Features

- **Compatible with an Embedded ARM7TDMI™ Processor**
- **Programmable Baud Rate Generator**
- **Parity, Framing and Overrun Error Detection**
- **Line Break Generation and Detection**
- **Automatic Echo, Local Loopback and Remote Loopback Channel Modes**
- **Multi-drop Mode: Address Detection and Generation**
- **Interrupt Generation**
- **Two Dedicated Peripheral Data Controller Channels Can be Easily Implemented**
- **5-, 6-, 7-, 8- and 9-bit Character Length**
- **Full Scan Testable (up to 98%)**
- **Can be Directly Connected to the Atmel Implementation of the AMBA™ Peripheral Bus (APB)**

Description

The two-channel, full-duplex USART features parity, framing and overrun error detection. A baud rate generator provides the bit period clock named the Baud Rate Clock to both the receiver and the transmitter. The USART can be programmed to operate in three different test modes: automatic echo, local loopback and remote loopback.

Two dedicated Peripheral Data Controller channels can be easily implemented. One is dedicated to the receiver. The other is dedicated to the transmitter.

The generation of interrupts is controlled in the status register by asserting the corresponding interrupt line.

The USART can be used with any 32-bit microcontroller core if the timing diagram shown on page 8 is respected. When using an ARM7TDMI as the core, the Atmel Bridge must be used to provide the correct bus interface to the peripheral.

32-bit Embedded ASIC Core Peripheral

USART

Rev. 1242E–12/01

Figure 1. USART Symbol

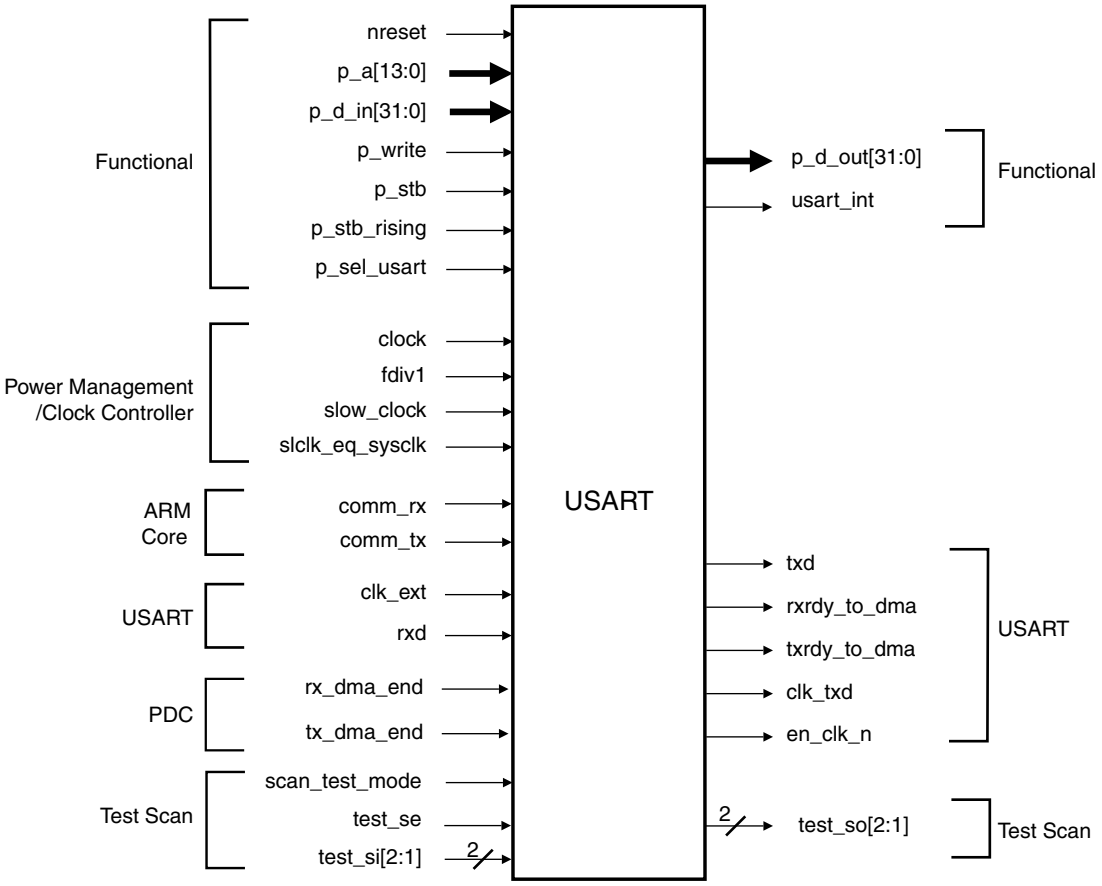


Table 1. USART Pin Description

Name	Function	Type	Active Level	Comments
Functional				
nreset	Reset System	Input	Low	Resets all the counters and signals
p_a[13:0]	Address Bus	Input	–	The address takes into account the 2 LSBs [1:0], but the macrocell does not take these bits into account (left unconnected).
p_d_in[31:0]	Input Data Bus	Input	–	From host (bridge)
p_d_out[31:0]	Output Data Bus	Output	–	To host (bridge)
p_write	Write Enable	Input	High	From host (bridge)
p_stb	Peripheral Strobe	Input	High	From host (bridge)
p_stp_rising	User Interface Clock Signal	Input	–	From host (bridge). Clock for all DFFs controlling the configuration registers.
p_sel_usart	Selection of the block	Input	High	From host (bridge)
usart_int	Interrupt signal to AIC	Output	High	
Power Management/Clock Controller				
clock	System Clock	Input	–	System clock for the USART output waveforms
fdiv1	USART Clock Enable	Input	–	System clock (clock) divided
slow_clock	ARM® Core Operation	Input		
slclk_eq_sysclk	ARM® Core Operation	Input		
ARM® Core				
comm_rx	ARM® Core Operation	Input	High	Must be connected to ARM core.
comm_tx	ARM® Core Operation	Input	High	Must be connected to ARM core.
USART				
clk_ext	Baud rate signal	Input	–	From SCK pad
rxd	Receive serial data pin	Input	–	
txd	Transmit serial data pin	Output	–	
rxrdy_to_dma	Output signal to DMA channel	Output	High	Byte available in the Receiver Holding Register (RHR). This signal connects to the PDC(1)
txrdy_to_dma	Output signal to the DMA channel	Output	High	There are no more characters in the Transmitter Holding Register (THR). This signal connects to the PDC(1)
clk_txd	Output of the baud rate generator	Output	–	To SCK pad
en_clk_n	Direction signal for SCK pad	Output	–	Active in synchronous mode
PDC				
rx_dma_end	End of receive DMA transfer	Input	High	Generated by PDC(1)
tx_dma_end	End of transmit DMA transfer	Input	High	Generated by PDC(1)

Table 1. USART Pin Description

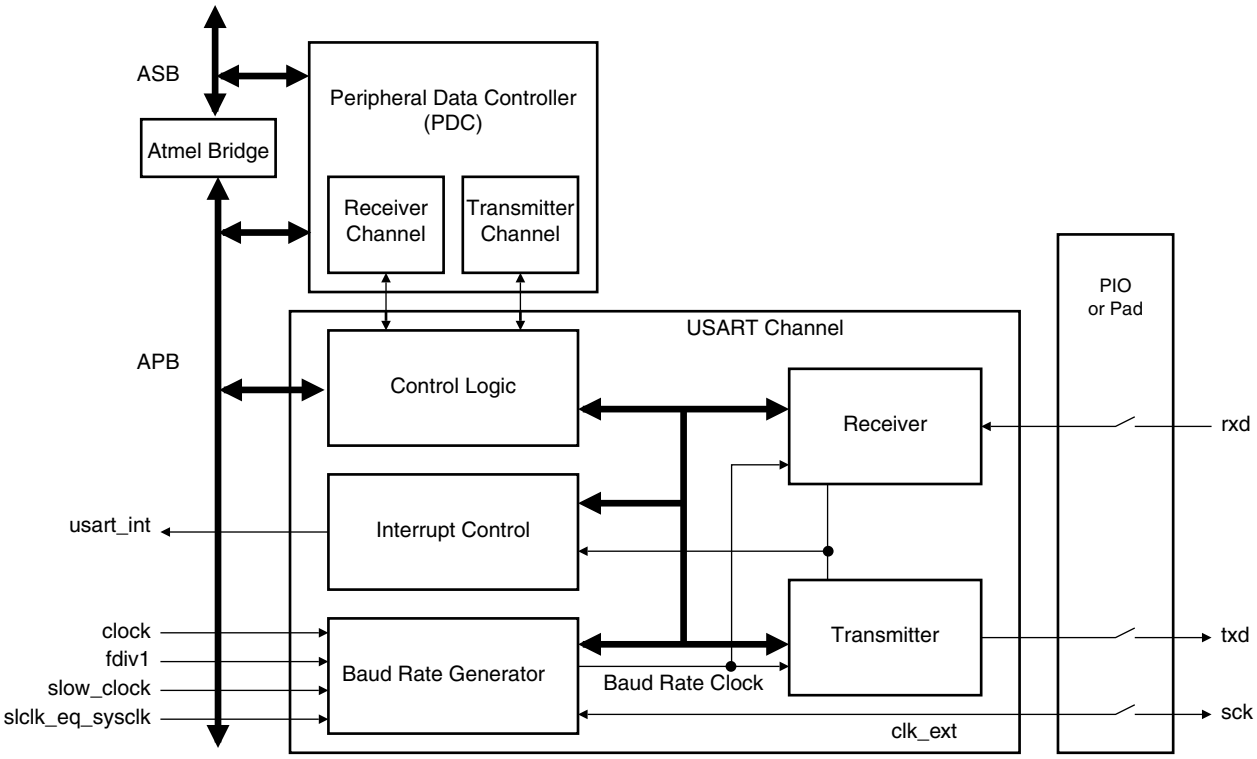
Name	Function	Type	Active Level	Comments
Test Scan				
scan_test_mode	Must be set when running the scan vectors	Input	High	
test_se	Scan test enable	Input	High/Low	Scan shift/scan capture
test_si[2:1]	Scan test input	Input	High	Entry of scan chain
test_so[2:1]	Scan test output	Output	–	Output of scan chain

Note: 1. The Peripheral Data Controller (PDC) is a separate block. Please refer to the corresponding datasheet.

Scan Test Configuration

The fault coverage is maximum if all non-scan inputs can be controlled and all non-scan outputs can be observed. In order to achieve this, the ATPG vectors must be generated on the entire circuit (top-level), which includes the USART, or all USART I/Os must have a top-level access and ATPG vectors must be applied to these pins.

Figure 2. USART Block Diagram

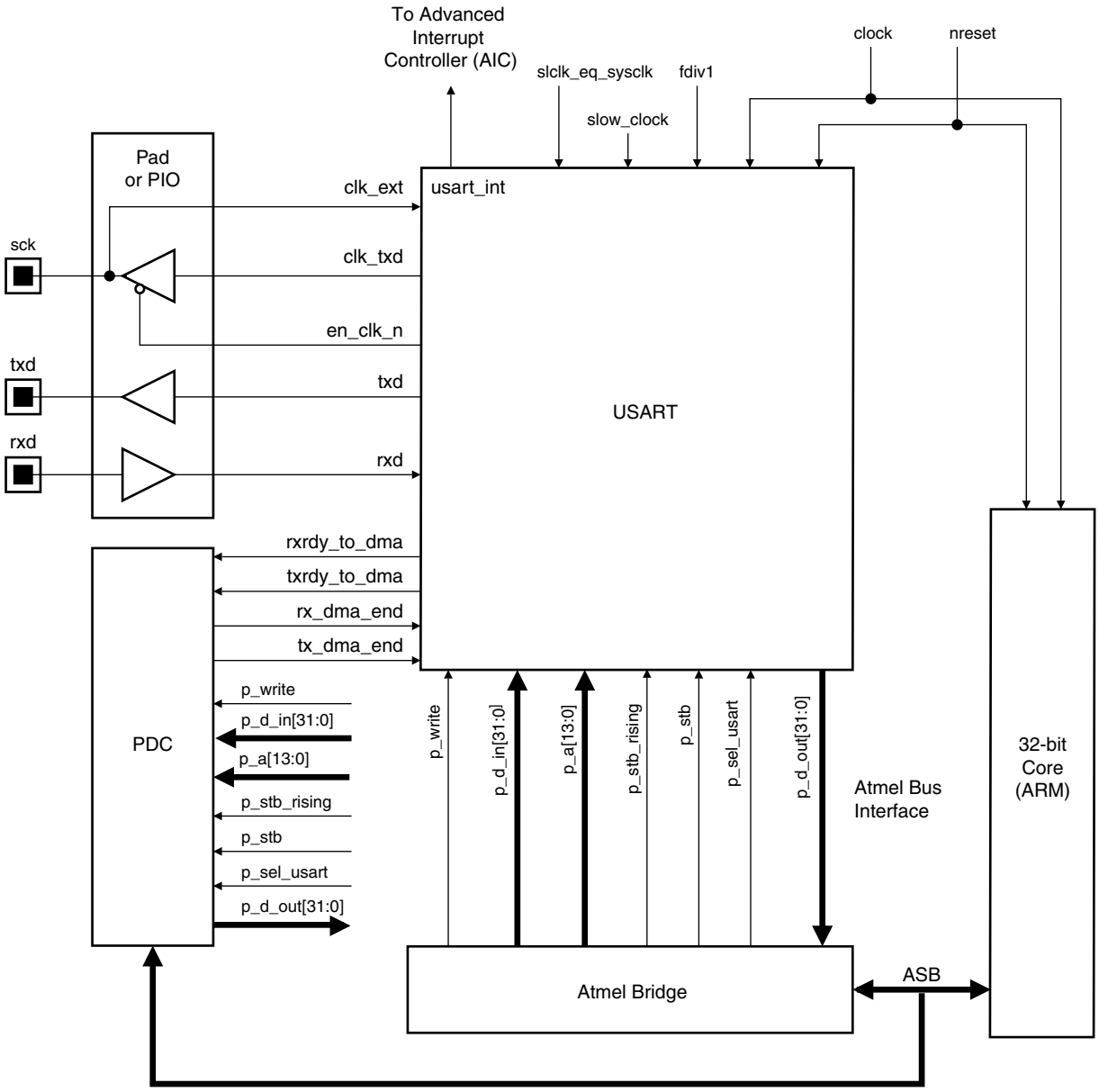


Peripheral Data Controller (PDC)

When the dedicated Atmel PDC is used, four additional registers are available in the USART (see page 16). These registers are physically located in the PDC and accessed when selecting the USART. For more details concerning these registers, please refer to the PDC datasheet.

The following pins are exclusively reserved for use with the PDC: rxrdy_to_dma, txrdy_to_dma, rx_dma_end, tx_dma_end. If the PDC is not used, rx_dma_end and tx_dma_end must be tied to zero.

Figure 3. Connecting the USART to an ARM®-based Microcontroller



Pin Description

Each USART channel has the following external signals:

Name	Description
sck	USART Serial clock can be configured as input or output: sck is configured as input if an external clock is selected (USCLKS = 11) sck is driven as output if the external clock is disabled (USCLKS[1] = 0) and clock output is enabled (CLKO = 1)
txd	Transmit Serial Data is an output
rxd	Receive Serial Data is an input

Timing Diagrams

Figure 4. USART Timing Diagram: Write/Read Cycle

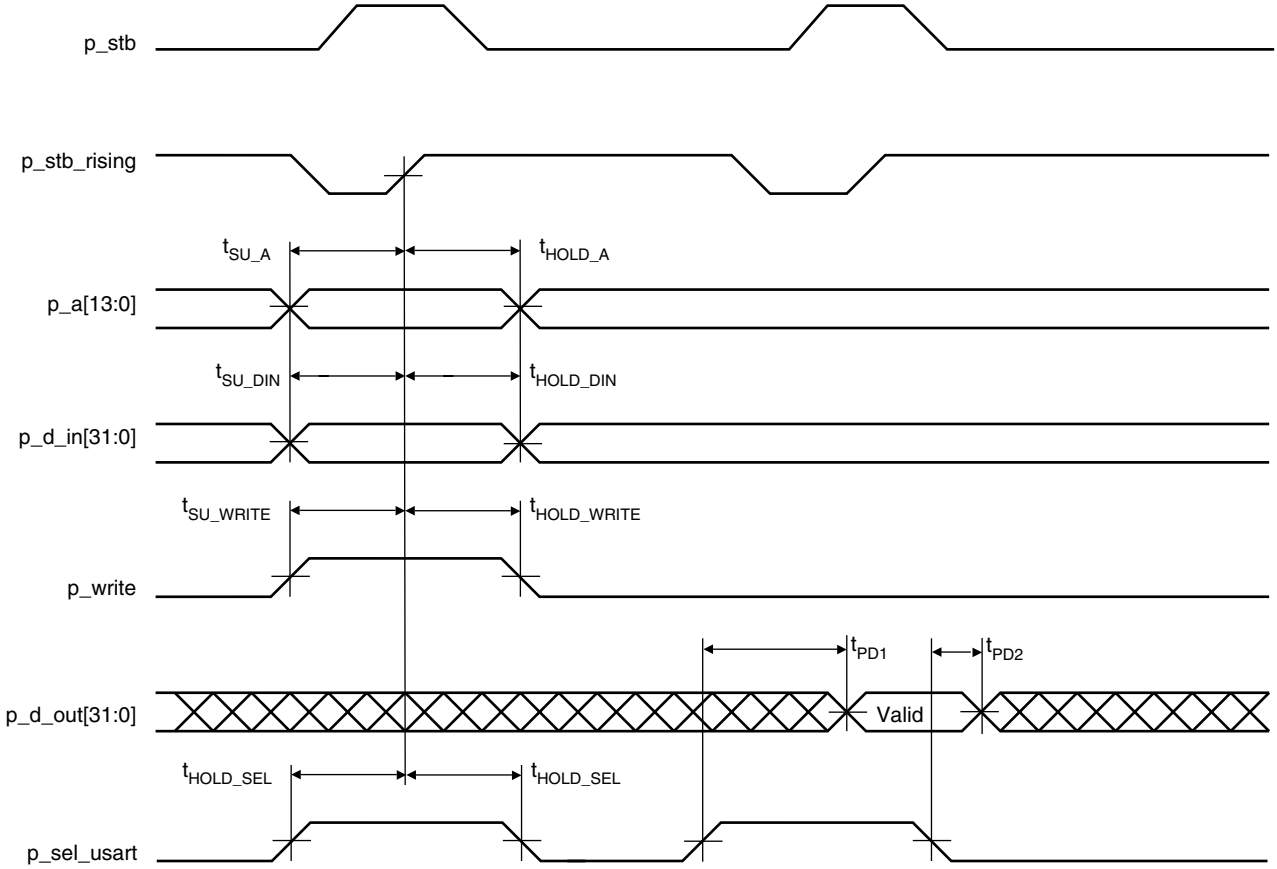
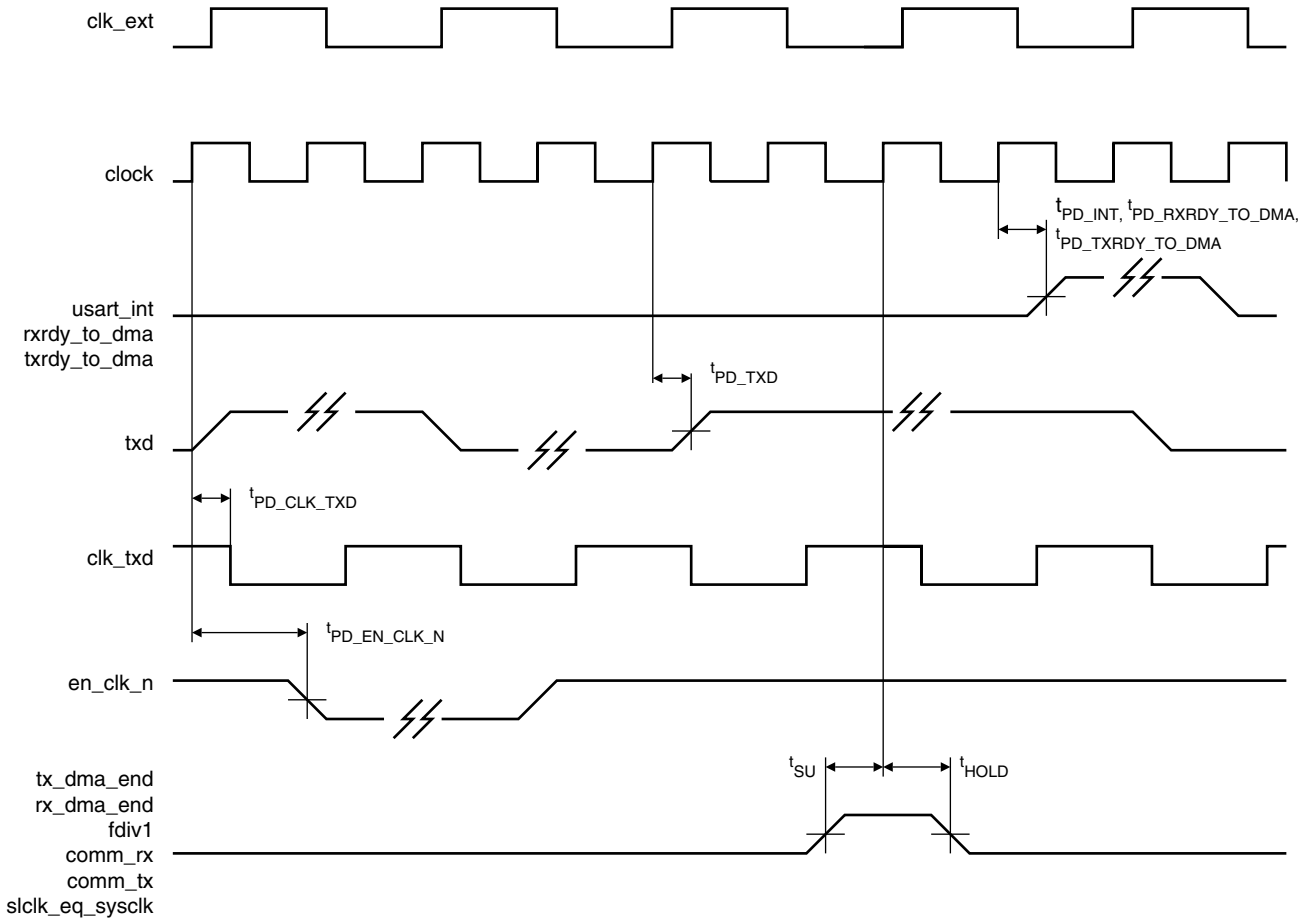


Figure 5. USART Timing Diagram: Propagation Delays, Control Signals



Baud Rate Generator

The Baud Rate Generator provides the bit period clock named the Baud Rate Clock to both the receiver and the transmitter.

The Baud Rate Generator can select between external and internal clock sources. The external clock source is SCK (clk_ext) or slow_clock. The internal clock sources can be either the master clock (clock) or the master clock divided (fdiv1).

Note: In all cases, if an external clock is used, the duration of each of its levels must be longer than the system clock (clock) period. The external clock frequency must be at least 4.5 times lower than the system clock.

When the USART is programmed to operate in asynchronous mode (SYNC = 0 in the Mode Register US_MR), the selected clock is divided by 16 times the value (CD) written in US_BRGR (Baud Rate Generator Register). If US_BRGR is set to 0, the Baud Rate Clock is disabled.

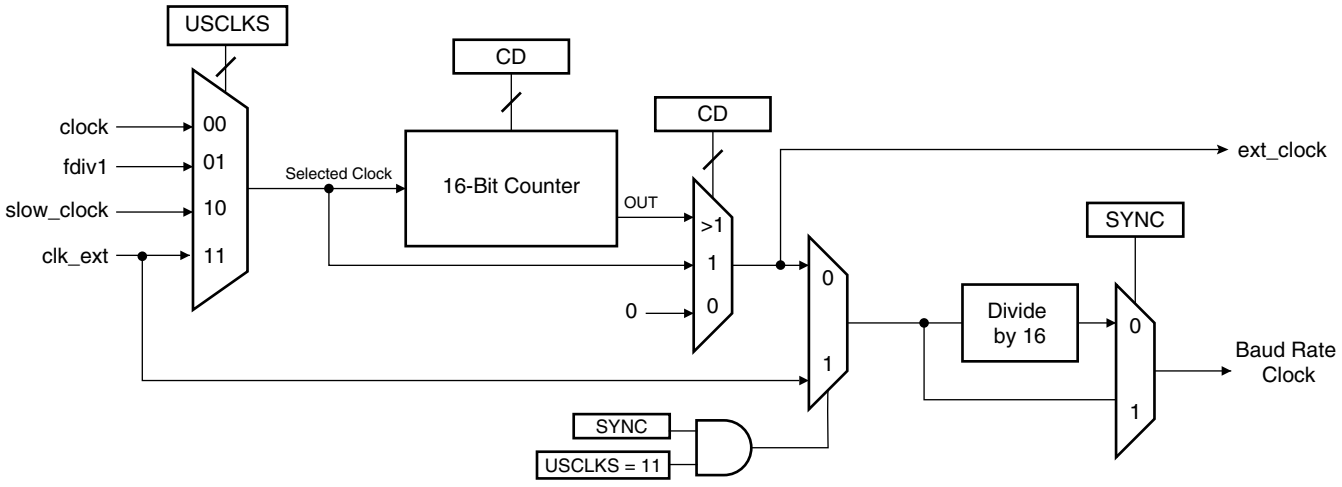
$$\text{Baud Rate} = \frac{\text{Selected Clock}}{16 \times \text{CD}}$$

When the USART is programmed to operate in synchronous mode (SYNC = 1) and the selected clock is internal (USCLKS[1] = 0 in the Mode Register US_MR), the Baud Rate Clock is the internal selected clock divided by the value written in US_BRGR. If US_BRGR is set to 0, the Baud Rate Clock is disabled.

$$\text{Baud Rate} = \frac{\text{Selected Clock}}{\text{CD}}$$

In synchronous mode with external clock selected (USCLKS = 11), the clock is provided directly by the signal on the SCK pin (clk_ext). No division is active. The value written in US_BRGR has no effect.

Figure 6. Baud Rate Generator



Receiver

Asynchronous Receiver

The USART is configured for asynchronous operation when SYNC = 0 (bit 7 of US_MR). In asynchronous mode, the USART detects the start of a received character by sampling the RXD signal until it detects a valid start bit. A low level (space) on RXD is interpreted as a valid start bit if it is detected for more than 7 cycles of the sampling clock, which is 16 times the baud rate. Hence, a space that is longer than 7/16 of the bit period is detected as a valid start bit. A space which is 7/16 of a bit period or shorter is ignored and the receiver continues to wait for a valid start bit.

When a valid start bit has been detected, the receiver samples the RXD at the theoretical mid-point of each bit. It is assumed that each bit lasts 16 cycles of the sampling clock (1-bit period) so the sampling point is eight cycles (0.5 bit period) after the start of the bit. The first sampling point is therefore 24 cycles (1.5 bit periods) after the falling edge of the start bit was detected. Each subsequent bit is sampled 16 cycles (1-bit period) after the previous one.

Figure 7. Asynchronous Mode: Start Bit Detection

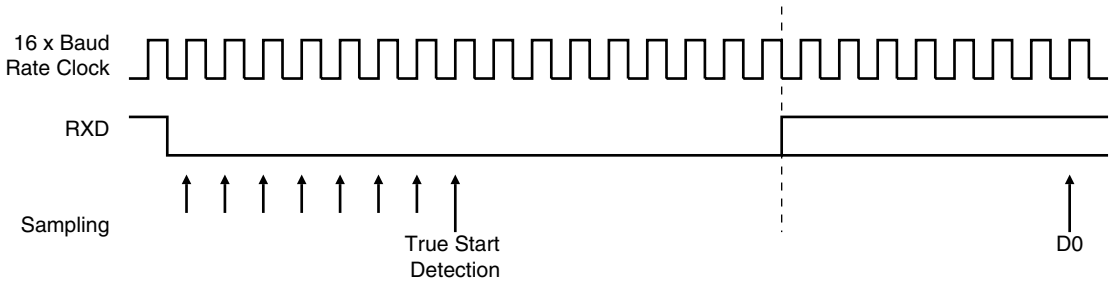
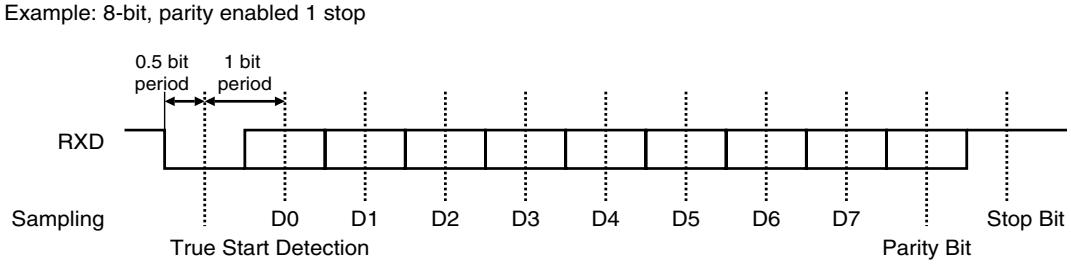


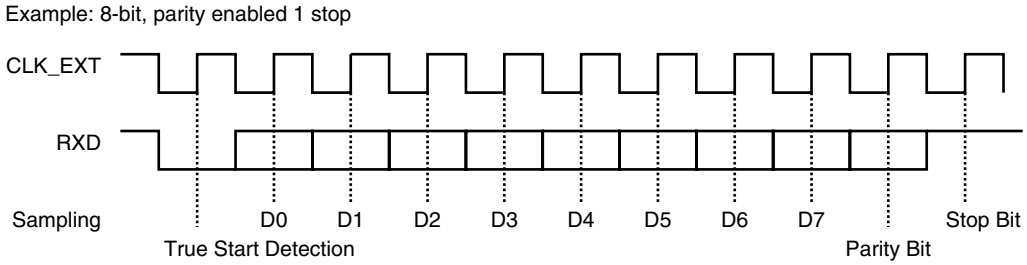
Figure 8. Asynchronous Mode: Character Reception



Synchronous Receiver

When configured for synchronous operation (SYNC = 1), the receiver samples the RXD signal on each rising edge of the Baud Rate Clock. If a low level is detected, it is considered as a start. Data bits, parity bit and stop bit are sampled and the receiver waits for the next start bit. See the example in Figure 9.

Figure 9. Synchronous Mode: Character Reception



Receiver Ready

When a complete character is received, it is transferred to the US_RHR and the RXRDY status bit in US_CSR is set. If US_RHR has not been read since the last transfer, the OVRE status bit in US_CSR is set.

Parity Error

Each time a character is received, the receiver calculates the parity of the received data bits, in accordance with the field PAR in US_MR. It then compares the result with the received parity bit. If different, the parity error bit PARE in US_CSR is set.

Framing Error

If a character is received with a stop bit at low level and with at least one data bit at high level, a framing error is generated. This sets FRAME in US_CSR.

Time-out

This function allows an idle condition on the RXD line to be detected. The maximum delay for which the USART should wait for a new character to arrive while the RXD line is inactive (high level) is programmed in US_RTOR (Receiver Time-out). When this register is set to 0, no time-out is detected. Otherwise, the receiver waits for a first character and then initializes a counter, which is decremented at each bit period and reloaded at each byte reception. When the counter reaches 0, the TIMEOUT bit in US_CSR is set. The user can restart the wait for a first character with the STTTO (Start Time-out) bit in US_CR.

Calculation of time-out duration:

$$\text{Duration} = \text{US\_RTOR Value} \times 4 \times \text{Bit Period}$$

Generating CLK_TXD

In synchronous mode, CLK_TXD is the clock as defined in Figure 9.

In asynchronous mode,

$$\text{CLK\_TXD} = 16 \times \text{Baud Rate Clock}$$

as defined in Figure 7.

Transmitter

The transmitter has the same behavior in both synchronous and asynchronous operating modes. Start bit, data bits, parity bit and stop bits are serially shifted, lowest significant bit first, on the falling edge of the serial clock. See the example in Figure 10.

The number of data bits is selected in the CHRL field in US_MR.

The parity bit is set according to the PAR field in US_MR.

The number of stop bits is selected in the NBSTOP field in US_MR.

When a character is written to US_THR (Transmit Holding), it is transferred to the Shift Register as soon as it is empty. When the transfer occurs, the TXRDY bit in US_CSR is set until a new character is written to US_THR. If Transmit Shift Register and US_THR are both empty, the TXEMPTY bit in US_CSR is set.

Time-guard

The time-guard function allows the transmitter to insert an idle state on the TXD line between two characters. The duration of the idle state is programmed in US_TTGR (Transmitter Time-guard). When this register is set to zero, no time-guard is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted byte during the number of bit periods programmed in US_TTGR:

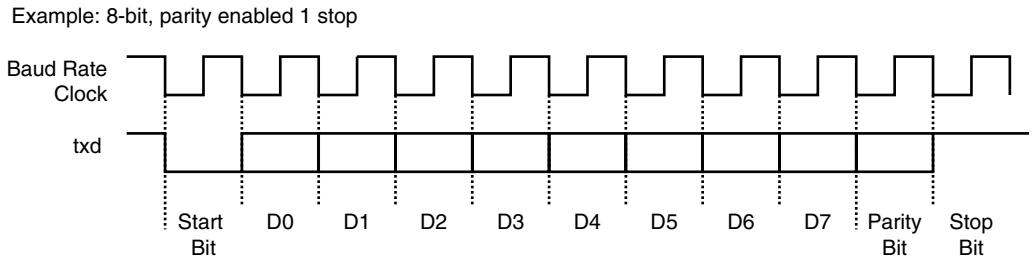
$$\text{Idle State Duration between Two Characters} = \text{Time-guard Value} \times \text{Bit Period}$$

Multi-drop Mode

When the field PAR in US_MR equals 11X (binary value), the USART is configured to run in multi-drop mode. In this case, the parity error bit PARE in US_CSR is set when data is detected with a parity bit set to identify an address byte. PARE is cleared with the Reset Status Bits command (RSTSTA) in US_CR. If the parity bit is detected low, identifying a data byte, PARE is not set.

The transmitter sends an address byte (parity bit set) when a Send Address command (SENDA) is written to US_CR. In this case, the next byte written to US_THR will be transmitted as an address. After this, any byte transmitted will have the parity bit cleared.

Figure 10. Synchronous and Asynchronous Modes: Character Transmission



Break

A break condition is a low signal level that has a duration of at least one character (including start/stop bits and parity).

Transmit Break

The transmitter generates a break condition on the TXD line when STTBRK is set in US_CR (Control Register). In this case, the character present in the Transmit Shift Register is completed before the line is held low.

To cancel a break condition on the TXD line, the STPBRK command in US_CR must be set. The USART completes a minimum break duration of one character length. The TXD line then returns to high level (idle state) for at least 12 bit periods, or the value of the Time-guard register if it is greater than 12, to ensure that the end of break is correctly detected. Then the transmitter resumes normal operation.

The BREAK is managed like a character:

- The STTBRK and the STPBRK commands are performed only if the transmitter is ready (bit TXRDY = 1 in US_CSR).
- The STTBRK command blocks the transmitter holding register (bit TXRDY is cleared in US_CSR) until the break has started.
- A break is started when the Shift Register is empty (any previous character is fully transmitted). US_CSR.TXEMPTY is cleared. The break blocks the transmitter shift register until it is completed (high level for at least 12 bit periods after the STPBRK command is requested).

In order to avoid unpredictable states:

- STTBRK and STPBRK commands must not be requested at the same time.
- Once an STTBRK command is requested, further STTBRK commands are ignored until the BREAK is ended (high level for at least 12 bit periods).
- All STPBRK commands requested without a previous STTBRK command are ignored.
- A byte written into the Transmit Holding Register while a break is pending but not started (bit TXRDY = 0 in US_CSR) is ignored.
- It is *not permitted* to write new data in the Transmit Holding Register while a break is in progress (STPBRK has not been requested), even though TXRDY = 1 in US_CSR.
- A new STTBRK command *must not* be issued until an existing break has ended (TXEMPTY=1 in US_CSR).

The standard break transmission sequence is:

1. Wait for the transmitter ready.
   (US_CSR.TXRDY = 1)
2. Send the STTBRK command.
   (Write 0x0200 to US_CR)
3. Wait for the transmitter ready.
   (bit TXRDY = 1 in US_CSR)
4. Send the STPBRK command.
   (Write 0x0400 to US_CR)

The next byte can then be sent:

5. Wait for the transmitter ready.
   (bit TXRDY = 1 in US_CSR)
6. Send the next byte.
   (Write byte to US_THR)

Each of these steps can be scheduled by using the interrupt if the bit TXRDY in US_IMR is set. For character transmission, the USART channel must be enabled before sending a break.

Receive Break

The receiver detects a break condition when all data, parity and stop bits are low. When the low stop bit is detected, the receiver asserts the RXBRK bit in US_CSR. An end of receive break is detected by a high level for at least 2/16 of a bit period in asynchronous operating mode or at least one sample in synchronous operating mode. RXBRK is also asserted when an end-of-break is detected.

Both the beginning and the end of a break can be detected by interrupt if the bit US_IMR.RXBRK is set.

Peripheral Data Controller Channels (PDC)

Each USART channel is closely connected to a corresponding Peripheral Data Controller channel. One is dedicated to the receiver. The other is dedicated to the transmitter.

The PDC channel is programmed using US_TPR (Transmit Pointer) and US_TCR (Transmit Counter) for the transmitter and US_RPR (Receive Pointer) and US_RCR (Receive Counter) for the receiver. The status of the PDC is given in US_CSR by the ENDTX bit for the transmitter and by the ENDRX bit for the receiver.

The pointer registers (US_TPR and US_RPR) are used to store the address of the transmit or receive buffers. The counter registers (US_TCR and US_RCR) are used to store the size of these buffers.

The receiver data transfer is triggered by the RXRDY bit and the transmitter data transfer is triggered by TXRDY. When a transfer is performed, the counter is decremented and the pointer is incremented. When the counter reaches 0, the status bit is set (ENDRX for the receiver, ENDTX for the transmitter in US_CSR) and can be programmed to generate an interrupt. While the counter is at zero, the status bit is asserted and transfers are disabled.

Interrupt Generation

Each status bit in US_CSR has a corresponding bit in US_IER (Interrupt Enable) and US_IDR (Interrupt Disable), which controls the generation of interrupts by asserting the USART interrupt line connected to the Advanced Interrupt Controller. US_IMR (Interrupt Mask Register) indicates the status of the corresponding bits.

When a bit is set in US_CSR and the same bit is set in US_IMR, the interrupt line is asserted.

Channel Test Configurations

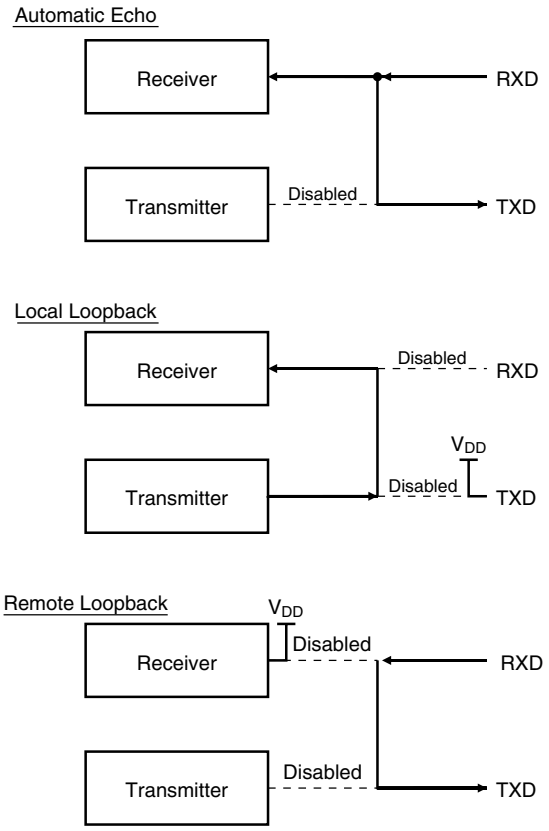
The USART can be programmed to operate in three different test modes, using the field CHMODE in US_MR.

Automatic echo mode allows bit-by-bit retransmission. When a bit is received on the RXD line, it is sent to the TXD line. Programming the transmitter has no effect.

Local loopback mode allows the transmitted characters to be received. TXD and RXD pins are not used and the output of the transmitter is internally connected to the input of the receiver. The RXD pin level has no effect and the TXD pin is held high, as in idle state.

Remote loopback mode directly connects the RXD pin to the TXD pin. The Transmitter and the Receiver are disabled and have no effect. This mode allows bit-by-bit retransmission.

Figure 11. Channel Modes



USART User Interface

Table 2. USART Memory Map

Offset	Register	Name	Access	Reset State
0x0000	Control Register	US_CR	Write-only	–
0x0004	Mode Register	US_MR	Read/Write	–
0x0008	Interrupt Enable Register	US_IER	Write-only	–
0x000C	Interrupt Disable Register	US_IDR	Write-only	–
0x0010	Interrupt Mask Register	US_IMR	Read-only	0
0x0014	Channel Status Register	US_CSR	Read-only	0x18
0x0018	Receiver Holding Register	US_RHR	Read-only	0
0x001C	Transmitter Holding Register	US_THR	Write-only	–
0x0020	Baud Rate Generator Register	US_BRGR	Read/Write	0
0x0024	Receiver Time-out Register	US_RTOR	Read/Write	0
0x0028	Transmitter Time-guard Register	US_TTGR	Read/Write	0
0x002C	Reserved	–	–	–
0x0030	Reserved for PDC connection	–	–	–
0x0034	Reserved for PDC connection	–	–	–
0x0038	Reserved for PDC connection	–	–	–
0x003C	Reserved for PDC connection	–	–	–

Notes:
1. The address takes into account the 2 LSBs [1:0], but the macrocell does not take these bits into account (left unconnected). Therefore loading 0x0001, 0x0002 or 0x0003 on P_A[13:0] addresses the Control Register.
2. In the following register description, all undefined bits (“–”) read “0”.
3. If the user selects an address that is not defined in the above table, the value of P_D_OUT[31:0] is 0x00000000.

USART Control Register

Name: US_CR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	SENDA	STTTO	STPBRK	STTBRK	RSTSTA
7	6	5	4	3	2	1	0
TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX	–	–

- **RSTRX: Reset Receiver**

0 = No effect.

1 = The receiver logic is reset, disabling the receive function (RXDIS is set internally).

- **RSTTX: Reset Transmitter**

0 = No effect.

1 = The transmitter logic is reset, disabling the transmit function (TXDIS and STPBRK are set internally).

- **RXEN: Receiver Enable**

0 = No effect.

1 = The receiver is enabled if RXDIS is 0.

- **RXDIS: Receiver Disable**

0 = No effect.

1 = The receiver is disabled.

- **TXEN: Transmitter Enable**

0 = No effect.

1 = The transmitter is enabled if TXDIS is 0.

- **TXDIS: Transmitter Disable**

0 = No effect.

1 = The transmitter is disabled.

- **RSTSTA: Reset Status Bits**

0 = No effect.

1 = Resets the status bits PARE, FRAME, OVRE and RXBRK in the US_CSR.

- **STTBRK: Start Break**

0 = No effect.

1 = If break is not being transmitted, start transmission of a break after the characters present in US_THR and the Transmit Shift Register have been transmitted.

- **STPBRK: Stop Break**

0 = No effect.

1 = If a break is being transmitted, stop transmission of the break after a minimum of one character length and transmit a high level during 12 bit periods.

- **STTTO: Start Time-out**

0 = No effect.

1 = Start waiting for a character before clocking the time-out counter.

- **SENDA: Send Address**

0 = No effect.

1 = In Multi-drop Mode only, the next character written to the US_THR is sent with the address bit set. USART Mode Register

USART Mode Register

Name: US_MR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	FILTER	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	CLKO	MODE9	–
15	14	13	12	11	10	9	8
CHMODE		NBSTOP		PAR			SYNC
7	6	5	4	3	2	1	0
CHRL		USCLKS		–	–	–	–

- **USCLKS: Clock Selection (Baud Rate Generator Input Clock)**

USCLKS		Selected Clock
0	0	clock
0	1	fdiv1
1	0	slow_clock (ARM)
1	1	External (SCK)

- **CHRL: Character Length**

Start, stop and parity bits are added to the character length.

CHRL		Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

- **SYNC: Synchronous Mode Select**

0 = USART operates in Asynchronous Mode.

1 = USART operates in Synchronous Mode.

- **PAR: Parity Type**

PAR			Parity Type
0	0	0	Even parity
0	0	1	Odd parity
0	1	0	Parity forced to 0 (Space)
0	1	1	Parity forced to 1 (Mark)
1	0	x	No parity
1	1	x	Multi-drop mode

- **NBSTOP: Number of Stop Bits**

The interpretation of the number of stop bits depends on SYNC.

NBSTOP		Asynchronous (SYNC = 0)	Synchronous (SYNC = 1)
0	0	1 stop bit	1 stop bit
0	1	1.5 stop bits	Reserved
1	0	2 stop bits	2 stop bits
1	1	Reserved	Reserved

Note: 1.5 or 2 stop bits are reserved for the TX function. The RX function uses only the 1 stop bit (there is no check on the 2 stop bit timeslot if NBSTOP = 10).

- **CHMODE: Channel Mode**

CHMODE		Mode Description
0	0	Normal Mode The USART Channel operates as an RX/TX USART.
0	1	Automatic Echo Receiver Data Input is connected to the TXD pin.
1	0	Local Loopback Transmitter Output Signal is connected to Receiver Input Signal.
1	1	Remote Loopback RXD pin is internally connected to TXD pin.

- **MODE9: 9-bit Character Length**

0 = CHRL defines character length.

1 = 9-bit character length.

MODE9 has priority on character length.

- **CKLO: Clock Output Select**

0 = The USART does not drive the SCK pin.

1 = The USART drives the SCK pin if USCLKS[1] is 0.

- **FILTER: Receive Line Filter**

0 = The USART does not filter receive line.

1 = The USART filters receive line using a three-sample filter (1/16 bit clock) (2 over 3 majority)

USART Interrupt Enable Register

Name: US_IER

Access Type: Write-only

31	30	29	28	27	26	25	24
COMM_RX	COMM_TX	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: Enable RXRDY Interrupt**

0 = No effect.

1 = Enables RXRDY Interrupt.

- **TXRDY: Enable TXRDY Interrupt**

0 = No effect.

1 = Enables TXRDY Interrupt.

- **RXBRK: Enable Receiver Break Interrupt**

0 = No effect.

1 = Enables Receiver Break Interrupt.

- **ENDRX: Enable End of Receive Transfer Interrupt**

0 = No effect.

1 = Enables End of Receive Transfer Interrupt.

- **ENDTX: Enable End of Transmit Interrupt**

0 = No effect.

1 = Enables End of Transmit Interrupt.

- **OVRE: Enable Overrun Error Interrupt**

0 = No effect.

1 = Enables Overrun Error Interrupt.

- **FRAME: Enable Framing Error Interrupt**

0 = No effect.

1 = Enables Framing Error Interrupt.

- **PARE: Enable Parity Error Interrupt**

0 = No effect.

1 = Enables Parity Error Interrupt.

- **TIMEOUT: Enable Time-out Interrupt**

0 = No effect.

1 = Enables Reception Time-out Interrupt.

- **TXEMPTY: Enable TXEMPTY Interrupt**

0 = No effect.

1 = Enables TXEMPTY Interrupt.

- **COMM_TX: Enable COMM_TX (from ARM) Interrupt**

0 = No effect.

1 = Enables COMM_TX interrupt.

- **COMM_RX: Enable COMM_RX (from ARM) Interrupt**

0 = No effect.

1 = Enables COMM_RX interrupt.

USART Interrupt Disable Register

Name: US_IDR

Access Type: Write-only

31	30	29	28	27	26	25	24
COMM_RX	COMM_TX	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: Disable RXRDY Interrupt**

0 = No effect.

1 = Disables RXRDY Interrupt.

- **TXRDY: Disable TXRDY Interrupt**

0 = No effect.

1 = Disables TXRDY Interrupt.

- **RXBRK: Disable Receiver Break Interrupt**

0 = No effect.

1 = Disables Receiver Break Interrupt.

- **ENDRX: Disable End of Receive Transfer Interrupt**

0 = No effect.

1 = Disables End of Receive Transfer Interrupt.

- **ENDTX: Disable End of Transmit Interrupt**

0 = No effect.

1 = Disables End of Transmit Interrupt.

- **OVRE: Disable Overrun Error Interrupt**

0 = No effect.

1 = Disables Overrun Error Interrupt.

- **FRAME: Disable Framing Error Interrupt**

0 = No effect.

1 = Disables Framing Error Interrupt.

- **PARE: Disable Parity Error Interrupt**

0 = No effect.

1 = Disables Parity Error Interrupt.

- **TIMEOUT: Disable Time-out Interrupt**

0 = No effect.

1 = Disables Receiver Time-out Interrupt.

- **TXEMPTY: Disable TXEMPTY Interrupt**

0 = No effect.

1 = Disables TXEMPTY Interrupt.

- **COMM_TX: Disable COMM_TX (from ARM) Interrupt**

0 = No effect.

1 = Disables COMM_TX interrupt.

- **COMM_RX: Disable COMM_RX (from ARM) Interrupt**

0 = No effect.

1 = Disables COMM_RX interrupt.

USART Interrupt Mask Register

Name: US_IMR

Access Type: Read-only

31	30	29	28	27	26	25	24
COMM_RX	COMM_TX	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: Mask RXRDY Interrupt**

0 = RXRDY Interrupt is disabled.

1 = RXRDY Interrupt is enabled.

- **TXRDY: Mask TXRDY Interrupt**

0 = TXRDY Interrupt is disabled.

1 = TXRDY Interrupt is enabled.

- **RXBRK: Mask Receiver Break Interrupt**

0 = Receiver Break Interrupt is disabled.

1 = Receiver Break Interrupt is enabled.

- **ENDRX: Mask End of Receive Transfer Interrupt**

0 = End of Receive Transfer Interrupt is disabled.

1 = End of Receive Transfer Interrupt is enabled.

- **ENDTX: Mask End of Transmit Interrupt**

0 = End of Transmit Interrupt is disabled.

1 = End of Transmit Interrupt is enabled.

- **OVRE: Mask Overrun Error Interrupt**

0 = Overrun Error Interrupt is disabled.

1 = Overrun Error Interrupt is enabled.

- **FRAME: Mask Framing Error Interrupt**

0 = Framing Error Interrupt is disabled.

1 = Framing Error Interrupt is enabled.

- **PARE: Mask Parity Error Interrupt**

0 = Parity Error Interrupt is disabled.

1 = Parity Error Interrupt is enabled.

- **TIMEOUT: Mask Time-out Interrupt**

0 = Receive Time-out Interrupt is disabled.

1 = Receive Time-out Interrupt is enabled.

- **TXEMPTY: Mask TXEMPTY Interrupt**

0 = TXEMPTY Interrupt is disabled.

1 = TXEMPTY Interrupt is enabled.

- **COMM_TX: Mask COMM_TX (from ARM) Interrupt**

0 = COMM_TX interrupt is disabled.

1 = COMM_TX interrupt is enabled.

- **COMM_RX: Mask COMM_RX (from ARM) Interrupt**

0 = COMM_RX interrupt is disabled.

1 = COMM_RX interrupt is enabled.

USART Channel Status Register

Name: US_CSR

Access Type: Read-only

31	30	29	28	27	26	25	24
COMM_RX	COMM_TX	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

- **RXRDY: Receiver Ready**

0 = No complete character has been received since the last read of the US_RHR or the receiver is disabled. If characters were being received when the receiver was disabled, RXRDY changes to 1 when the receiver is enabled.

1 = At least one complete character has been received and the US_RHR has not yet been read.

- **TXRDY: Transmitter Ready**

0 = A character is in the US_THR waiting to be transferred to the Transmit Shift Register, or an STTBRK command has been requested, or the transmitter is disabled. As soon as the transmitter is enabled, TXRDY becomes 1.

1 = There is no character in the US_THR.

Equal to zero when the USART is disabled or at reset. The Transmitter Enable command (in US_CR) sets this bit to one if the transmitter was previously disabled.

- **RXBRK: Break Received/End of Break**

0 = No Break Received or End of Break detected since the last Reset Status Bits command in the Control Register.

1 = Break Received or End of Break detected since the last Reset Status Bits command in the Control Register.

- **ENDRX: End of Receiver Transfer**

0 = The End of Transfer signal from the Peripheral Data Controller channel dedicated to the receiver is inactive.

1 = The End of Transfer signal from the Peripheral Data Controller channel dedicated to the receiver is active.

- **ENDTX: End of Transmitter Transfer**

0 = The End of Transfer signal from the Peripheral Data Controller channel dedicated to the transmitter is inactive.

1 = The End of Transfer signal from the Peripheral Data Controller channel dedicated to the transmitter is active.

- **OVRE: Overrun Error**

0 = No byte has been transferred from the Receive Shift Register to the US_RHR when RxRDY was asserted since the last Reset Status Bits command.

1 = At least one byte has been transferred from the Receive Shift Register to the US_RHR when RxRDY was asserted since the last Reset Status Bits command.

- **FRAME: Framing Error**

0 = No stop bit has been detected low since the last Reset Status Bits command.

1 = At least one stop bit has been detected low since the last Reset Status Bits command.

- **PARE: Parity Error**

1 = At least one parity bit has been detected false (or a parity bit high in multi-drop mode) since the last Reset Status Bits command.

0 = No parity bit has been detected false (or a parity bit high in multi-drop mode) since last Reset Status Bits command.

- **TIMEOUT: Receiver Time-out**

0 = There has not been a time-out since the last Start Time-out command or the Time-out Register is 0.

1 = There has been a time-out since the last Start Time-out command.

- **TXEMPTY: Transmitter Empty**

0 = There are characters in either US_THR or the Transmit Shift Register, or the transmitter is disabled.

1 = There are no characters in either US_THR or the Transmit Shift Register. TXEMPTY is 1 after Parity, Stop Bit and Time-guard have been transmitted. TXEMPTY is 1 after stop bit has been sent, or after Time-guard has been sent if US_TTGR is not 0.

Equal to zero when the USART is disabled or at reset. Transmitter Enable command (in US_CR) sets this bit to one if the transmitter is disabled.

- **COMM_TX: (from ARM)**

0 = COMM_TX is at 0.

1 = COMM_TX is at 1.

- **COMM_RX: (from ARM)**

0 = COMM_RX is at 0.

1 = COMM_RX is at 1.

USART Receiver Holding Register

Name: US_RHR

Access Type: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
RXCHR							

- **RXCHR: Received Character**

Last character received if RXRDY is set. When number of data bits is less than 8 bits, the bits are right-aligned. All non-significant bits read zero.

USART Transmitter Holding Register

Name: US_THR

Access Type: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TXCHR							

- **TXCHR: Character to be Transmitted**

Next character to be transmitted after the current character if TXRDY is not set. When number of data bits is less than 8 bits, the bits are right-aligned.

USART Baud Rate Generator Register

Name: US_BRGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
CD							
7	6	5	4	3	2	1	0
CD							

- **CD: Clock Divisor**

This register has no effect if Synchronous Mode is selected with an external clock.

CD	Description
0	Disables Clock
1	Clock Divisor Bypass
2 to 65535	Baud Rate (Asynchronous Mode) = Selected Clock / (16 x CD) Baud Rate (Synchronous Mode) = Selected Clock / CD

Notes:
1. In Synchronous Mode, when either external clock (clk_ext or fdiv1) is selected, the value programmed must be even to ensure a 50:50 mark:space ratio.
   In Synchronous Mode, when the internal clock (clock) is selected, the CD can be even and the duty clock is 50:50.
2. Clock divisor bypass (CD = 1) must not be used when the internal clock (clock) is selected (USCLKS = 0).

USART Receiver Time-out Register

Name: US_RTOR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TO							

- **TO: Time-out Value**

When a value is written to this register, a Start Time-out command is automatically performed.

Time-out duration = TO x 4 x Bit Period

TO	Description
0	Disables the RX Time-out function.
1 - 255	The Time-out counter is loaded with TO when the Start Time-out command is given or when each new data character is received (after reception has started).

USART Transmitter Time-guard Register

Name: US_TTGR

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
TG							

- **TG: Time-guard Value**

Time-guard duration = TG x Bit Period

TG	
0	Disables the TX Time-guard function.
1 - 255	TXD is inactive high after the transmission of each character for the time-guard duration.

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