GaAs IC AMPS/ETACS Power Amplifier

Alpha

AP110-79

Features

- Output Power Up to 31 dBm
- 4.8 V Operation
- Efficiency Greater Than 55%
- High Power SSOP-16 Package with Slug

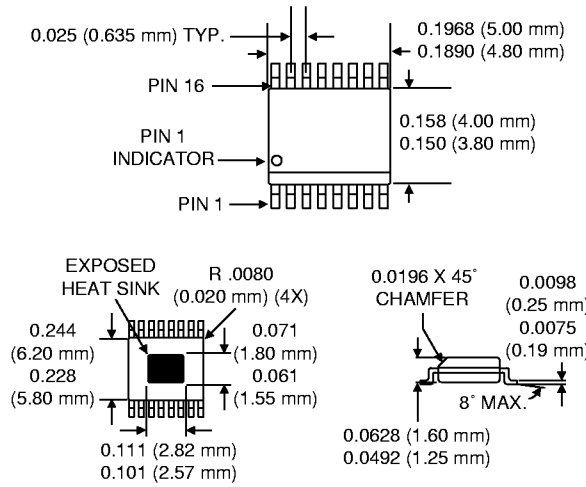
Description

The AP110-79 is a low cost IC power amplifier designed for the 824–849 MHz frequency band. It features 4 cell battery operation and high efficiency. The amplifier is designed to be stable over a temperature range of -30 to 100°C and over 7:1 VSWR loads.

Output Matching Circuit

The output match for the AP110-79 is provided externally in order to improve performance, reduce cost, and add flexibility. By making use of ceramic surface mount components with better Qs than GaAs matching elements, a lower loss matching network can be made. This lower loss results in higher power and efficiency for the amplifier. Also, by keeping these elements external the GaAs die size is reduced and the overall cost is less. This approach also permits the flexibility to tweak the amplifier for optimum performance at different powers, and/or frequencies.

SSOP-16 Slug



Electrical Specifications at 25°C

Characteristic	Condition	Frequency	Min.	Typ.	Max.	Unit
Output Power	$0<P_{IN}<7$	824–849 MHz		30.5		dBm
Efficiency	P_{OUT} = 30.5 dBm			55		%
Small Signal Gain	P_{IN} = -20 dBm			25		dB
Idle Current	P_{IN} = -60 dBm			75		mA
Noise in the Receive Band	P_{OUT} = 29.5 dBm R_X Band = 869–894 MHz R_X Bandwidth = 30 kHz			-100	-95	dBm
Input VSWR	P_{IN} = -30 to +7 dBm				2.5:1	
Harmonic Power	2fo 3fo			-25 -35		dBc
Input Impedance				50		Ω

Pin Out Assignments

Pin 1: V_{DD}
Bias controller supply voltage. The regulated +3.75 V supply must be connected to this pin. Disconnecting this voltage will turn the PA bias off. A switch at this pin can turn the PA on or off while leaving V_{SS} applied. A 6.8K resistor must be connected between this pin and Pin 2.

Pin 2: V_{REF}
Reference voltage for bias control circuitry. A 6.8K resistor between this pin and Pin 1 is needed to set nominal drain currents.

Pin 3: V_{GS2}
Second stage gate voltage tap.

Pin 4: V_{DS1}
First stage drain bias feed. Requires a matching inductor with good RF bypassing and the +4.8 V nominal supply voltage.

Pin 5: V_{GS1}
First stage gate voltage tap. Requires a 22K resistor to properly bias the first stage.

Pin 6: RF In
RF input with a 33 pF series input matching capacitor.

Pin 7-11: GND
Connect to ground.

Pin 12-13: RF Out/V_{DS2}
RF output and bias injection for the second stage drain. Output matching circuitry is required to transform the optimum load impedance to 50 Ω. The circuit must also provide a path for the +4.8 V DC bias and have good RF bypassing.

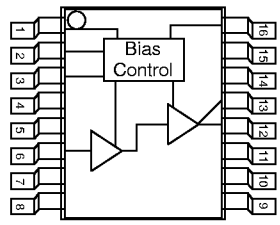
Pin 14-15: GND
Connect to ground.

Pin 16: V_{SS}
Negative bias supply voltage is -2.75 V. Two bypassing capacitors, a 100 nF and a 33 pF capacitor, are required.

Absolute Maximum Ratings

Characteristic	Symbol	Value
Drain Voltage	V_{DS}	10 V
Positive Bias Voltage	V_{DD}	6 V
Negative Bias Voltage	V_{SS}	-6 V
Power Input	P_{IN}	12 dBm
Operating Temperature	T_{OPT}	-30 to 100°C
Storage Temperature	T_{STG}	-35 to 120°C

Pin Out



Pin Configuration

Terminal	Symbol	Function
1	V_{DD}	Positive Bias Voltage In
2	V_{REF}	Reference Voltage
3	V_{GS2}	Gate Voltage 2
4	V_{DS1}	Drain Supply Voltage 1
5	V_{GS1}	Gate Voltage 1
6	RF In	RF Input
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	RF Out/V_{DS2}	RF Out/Drain Supply Voltage 2
13	RF Out/V_{DS2}	RF Out/Drain Supply Voltage 2
14	GND	Ground
15	GND	Ground
16	V_{SS}	Negative Bias Voltage In

Standby Mode

The power amplifier should be turned off whenever possible in order to reduce the overall power consumption. The AP110 can be turned off in several ways. The simplest is to switch the bias controller supply voltage (Pin 1) open. The gate bias voltages are in turn reduced from their nominal voltages to V_{SS}, resulting in a PA bias current of less than 1 mA. Additional PMOS switches in the drain lines drop the bias-off currents to <10 µA.

Bias Controller Circuit

An on-chip bias controller circuit eliminates the need to individually adjust the gate bias voltages. This circuit uses +3.75 V and the negative voltage (-2.75 V) to set the gate voltages on each stage for the proper bias current.