



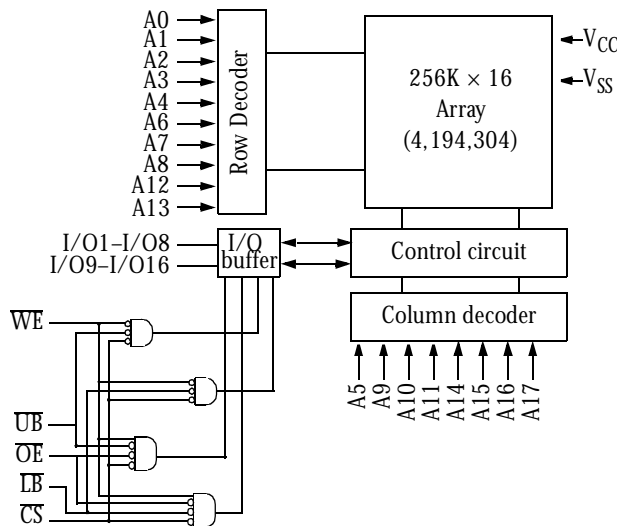
2.7V to 3.3V 256K × 16 Intelliwatt™ low-power CMOS SRAM with one chip enable

Features

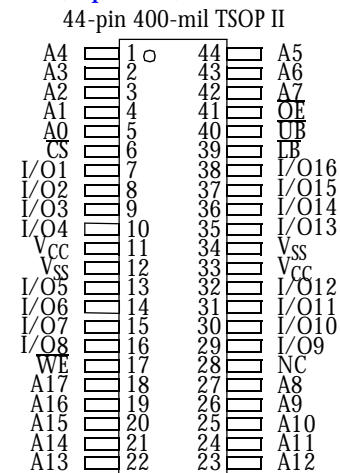
- AS6VA25616
- Intelliwatt™ active power circuitry
- Industrial and commercial temperature ranges available
- Organization: 262,144 words × 16 bits
- 2.7V to 3.3V at 55 ns
- Low power consumption: ACTIVE
 - 132 mW at 3.3V and 55 ns
- Low power consumption: STANDBY
 - 66 μ W max at 3.3V

- 1.2V data retention
- Equal access and cycle times
- Easy memory expansion with \overline{CS} , \overline{OE} inputs
- Smallest footprint packages
 - 48-ball FBGA
 - 400-mil 44-pin TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement (top view)



Note: A "MODE" pad is to be placed between pins 33 and 34 and 11 and 12, shorted. The bonding of this pad to V_{CC} or V_{SS} configures the device. There should only be 44+2+2 pads on the chip. Two extra V_{CC} to separate out Array from Peripheral and Two-Mode Pads.

48-CSP Ball-Grid-Array Package

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-------|-------|-----|-----|------|------|
| A | LB | OE | A0 | A1 | A2 | NC |
| B | I/O9 | UB | A3 | A4 | CS | I/O1 |
| C | I/O10 | I/O11 | A5 | A6 | I/O2 | I/O3 |
| D | VSS | I/O12 | A17 | A7 | I/O4 | VCC |
| E | VCC | I/O13 | NC | A16 | I/O5 | VSS |
| F | I/O15 | I/O14 | A14 | A15 | I/O6 | I/O7 |
| G | I/O16 | NC | A12 | A13 | WE | I/O8 |
| H | NC | A8 | A9 | A10 | A11 | NC |

Selection guide

| Product | V _{CC} Range | | | Speed (ns) | Power Dissipation | |
|------------|-----------------------|-------------------------|------------|---------------|-------------------------------|-----------------------------|
| | Min (V) | Typ ² (V) | Max (V) | | Operating (I _{CC1}) | Standby (I _{SB2}) |
| | | | | | Max (mA) | Max (μA) |
| AS6VA25616 | 2.7 | 3.0 | 3.3 | 55 | 2 | 20 |



Functional description

The AS6VA25616 is a low-power CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words \times 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 55 ns are ideal for low-power applications. Active high and low chip selects (\overline{CS}) permit easy memory expansion with multiple-bank memory systems.

When \overline{CS} is high, or \overline{UB} and \overline{LB} are high, the device enters standby mode: the AS6VA25616 is guaranteed not to exceed 66 μ W power consumption at 3.3V and 55ns. The device also returns data when V_{CC} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable (\overline{WE}) and chip select (\overline{CS}) low, and \overline{UB} and/or \overline{LB} low. Data on the input pins I/O1–O16 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CS} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting output enable (\overline{OE}), chip select (\overline{CS}), \overline{UB} and \overline{LB} low, with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip select or output enable is inactive, or write enable is active, or (\overline{UB}) and (\overline{LB}), output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. \overline{LB} controls the lower bits, I/O1–I/O8, and \overline{UB} controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are CMOS-compatible, and operation is from either a single 2.7V to 3.3V supply. Device is available in the JEDEC standard 400-mL, TSOP II, and 48-ball FBGA packages.

Absolute maximum ratings

| Parameter | Device | Symbol | Min | Max | Unit |
|--|--------|------------|------|----------------|------|
| Voltage on V_{CC} relative to V_{SS} | | V_{dIN} | –0.5 | $V_{CC} + 0.5$ | V |
| Voltage on any I/O pin relative to GND | | $V_{dI/O}$ | –0.5 | | V |
| Power dissipation | | P_D | – | 1.0 | W |
| Storage temperature (plastic) | | T_{stg} | –65 | +150 | °C |
| Temperature with V_{CC} applied | | T_{bias} | –55 | +125 | °C |
| DC output current (low) | | I_{OUT} | – | 20 | mA |

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

| \overline{CS} | \overline{WE} | \overline{OE} | \overline{LB} | \overline{UB} | Supply Current | I/O1–I/O8 | I/O9–I/O16 | Mode |
|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|-----------|------------|-----------------------------|
| H | X | X | X | X | I_{SB} | High Z | High Z | Standby (I_{SB}) |
| L | X | X | H | H | | | | |
| L | H | H | X | X | I_{CC} | High Z | High Z | Output disable (I_{CC}) |
| L | H | L | L | H | I_{CC} | D_{OUT} | High Z | Read (I_{CC}) |
| | | | H | L | | High Z | D_{OUT} | |
| | | | L | L | | D_{OUT} | D_{OUT} | |
| L | L | X | L | H | I_{CC} | D_{IN} | High Z | Write (I_{CC}) |
| | | | H | L | | High Z | D_{IN} | |
| | | | L | L | | D_{IN} | D_{IN} | |

Key: X = Don't care, L = Low, H = High.



Recommended operating condition (over the operating range)

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|-----------------------------|---|--|--------------------------------|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -2.1mA | V _{CC} = 2.7V | 2.4 | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 2.1mA | V _{CC} = 2.7V | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | V _{CC} = 2.7V | 2.2 | V _{CC} + 0.5 | V |
| V _{IL} | Input LOW Voltage | | V _{CC} = 2.7V | -0.5 | 0.8 | V |
| I _{IX} | Input Load Current | GND ≤ V _{IN} ≤ V _{CC} | | -1 | +1 | μA |
| I _{OZ} | Output Load Current | GND ≤ V _O ≤ V _{CC} ; Outputs High Z | | -1 | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | $\overline{CS} = V_{IL}, V_{IN} = V_{IL}$ or $V_{IH}, I_{OUT} = 0mA,$ $f = 0$ | V _{CC} = 3.3V | | 2 | mA |
| I _{CC1} @ 1 MHz | Average V _{CC} Operating Supply Current at 1 MHz | $\overline{CS} \leq 0.2V, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V,$ $f = 1\text{ mS}$ | V _{CC} = 3.3V | | 2 | mA |
| I _{CC2} | Average V _{CC} Operating Supply Current | $\overline{CS} \neq V_{IL}, V_{IN} = V_{IL}$ or $V_{IH}, f = f_{Max}$ | V _{CC} = 3.3V (55 ns) | | 40 | mA |
| I _{SB} | \overline{CS} Power Down Current; TTL Inputs | $\overline{CS} \geq V_{IH}$ or $\overline{UB} = \overline{LB}$ $\geq V_{IH}$, other inputs = V_{IL} or $V_{IH}, f = 0$ | V _{CC} = 3.3V | | 100 | μA |
| I _{SB1} | \overline{CS} Power Down Current; CMOS Inputs | $\overline{CS} \geq V_{CC} - 0.2V$ or $\overline{UB} = \overline{LB} \geq V_{CC} - 0.2V,$ other inputs = 0V - $V_{CC}, f = f_{Max}$ | V _{CC} = 3.3V | | 20 | μA |
| I _{SBDR} | Data Retention | $\overline{CS} \geq V_{CC} - 0.1V,$ $\overline{UB} = \overline{LB} = V_{CC} - 0.1V$ $f = 0$ | V _{CC} = 1.2V | | 2 | μA |

Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|-------------------|------------------|--|---|-----|------|
| Input capacitance | C _{IN} | A, \overline{CS} , WE, OE, \overline{LB} , \overline{UB} | V _{IN} = 0V | 5 | pF |
| I/O capacitance | C _{I/O} | I/O | V _{IN} = V _{OUT} = 0V | 7 | pF |



Read cycle (over the operating range)

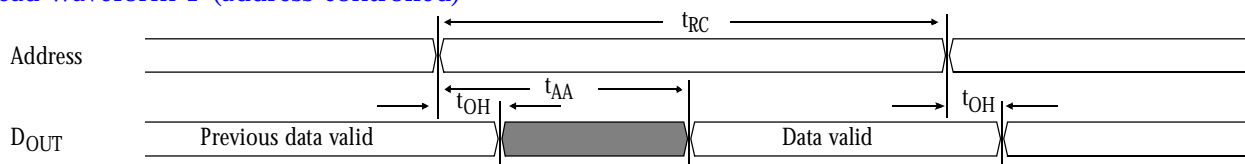
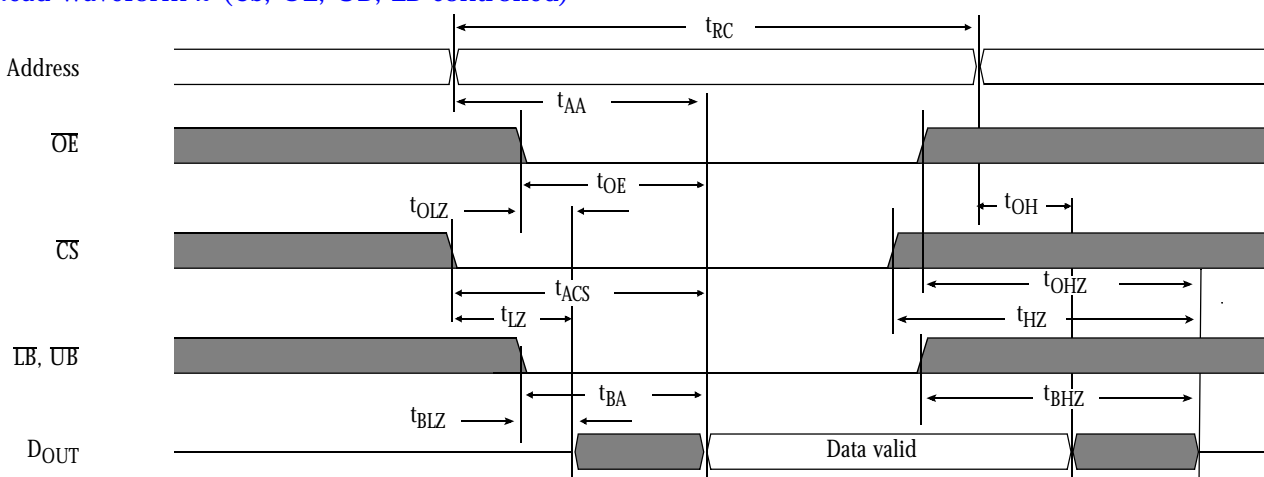
| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------|-----|-----|------|-------|
| Read cycle time | t_{RC} | 55 | – | ns | |
| Address access time | t_{AA} | – | 55 | ns | 3 |
| Chip select (\overline{CS}) access time | t_{ACS} | – | 55 | ns | 3 |
| Output enable (\overline{OE}) access time | t_{OE} | – | 25 | ns | |
| Output hold from address change | t_{OH} | 10 | – | ns | 5 |
| \overline{CS} to output in low Z | t_{CLZ} | 10 | – | ns | 4, 5 |
| \overline{CS} high to output in high Z | t_{CHZ} | 0 | 20 | ns | 4, 5 |
| \overline{OE} low to output in low Z | t_{OLZ} | 5 | – | ns | 4, 5 |
| $\overline{UB}/\overline{LB}$ access time | t_{BA} | – | 55 | ns | |
| $\overline{UB}/\overline{LB}$ low to low Z | t_{BLZ} | 10 | – | ns | 4, 5 |
| $\overline{UB}/\overline{LB}$ high to high Z | t_{BHZ} | 0 | 20 | ns | 4, 5 |
| \overline{OE} high to output in high Z | t_{OHZ} | 0 | 20 | ns | 4, 5 |
| Power up time | t_{PU} | 0 | – | ns | 4, 5 |
| Power down time | t_{PD} | – | 55 | ns | 4, 5 |

Shaded areas indicate preliminary information.

Key to switching waveforms

Rising input
 Falling input
 Undefined/don't care

Read waveform 1 (address controlled)

Read waveform 2 (\overline{CS} , \overline{OE} , \overline{UB} , \overline{LB} controlled)

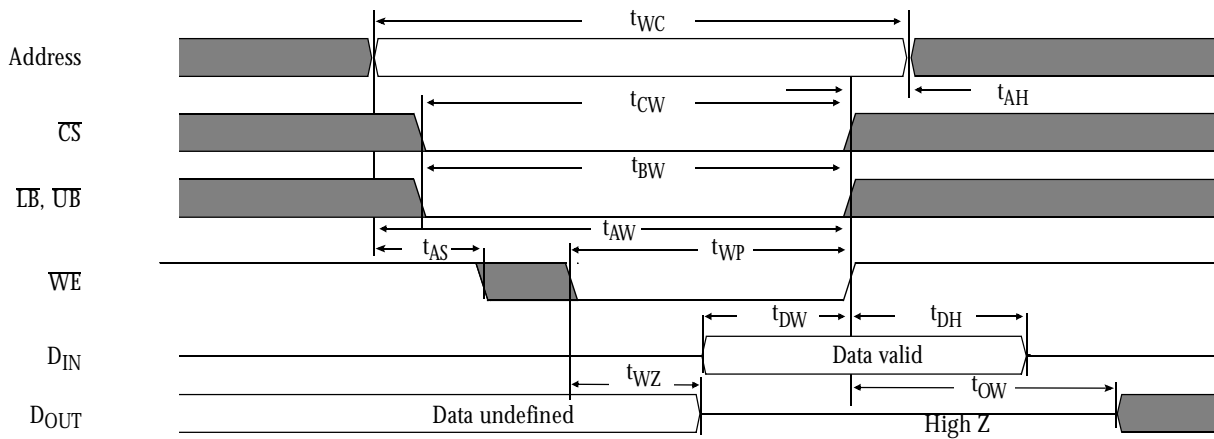


Write cycle (over the operating range)

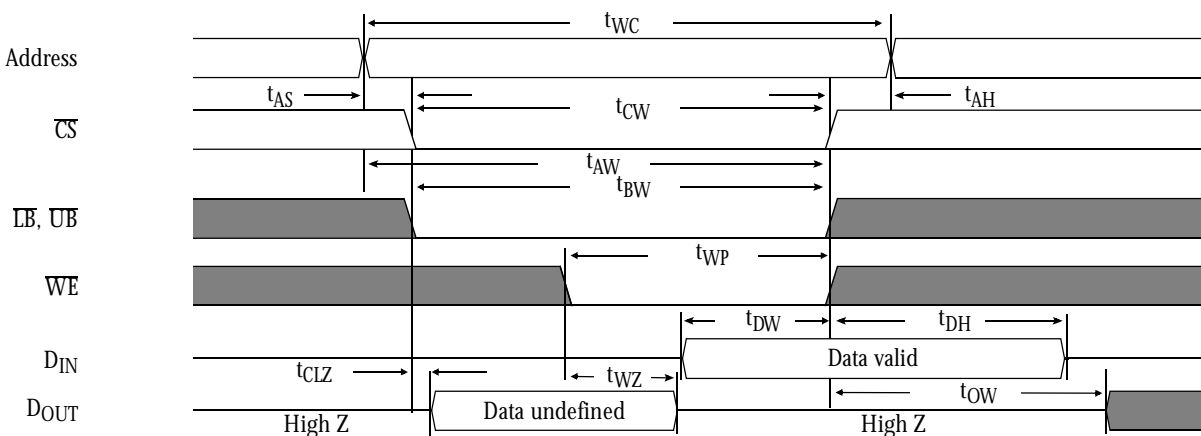
| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|-----|------|-------|
| Write cycle time | t_{WC} | 55 | – | ns | |
| Chip select to write end | t_{CW} | 40 | – | ns | 12 |
| Address setup to write end | t_{AW} | 40 | – | ns | |
| Address setup time | t_{AS} | 0 | – | ns | 12 |
| Write pulse width | t_{WP} | 35 | – | ns | |
| Address hold from end of write | t_{AH} | 0 | – | ns | |
| Data valid to write end | t_{DW} | 25 | – | ns | |
| Data hold time | t_{DH} | 0 | – | ns | 4, 5 |
| Write enable to output in high Z | t_{WZ} | 0 | 20 | ns | 4, 5 |
| Output active from write end | t_{OW} | 5 | – | ns | 4, 5 |
| $\overline{UB}/\overline{LB}$ low to end of write | t_{BW} | 35 | – | ns | |

Shaded areas indicate preliminary information.

Write waveform 1 (\overline{WE} controlled)



Write waveform 2 (\overline{CS} controlled)

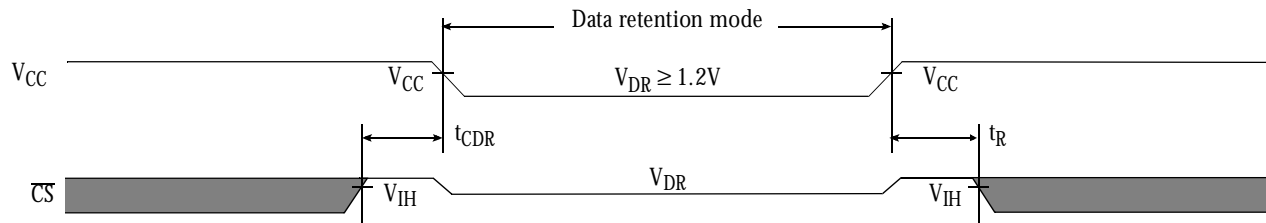




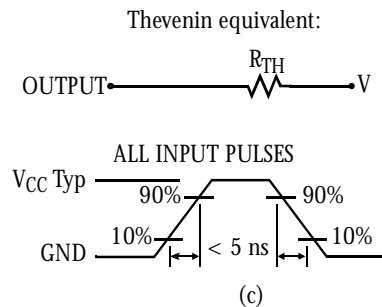
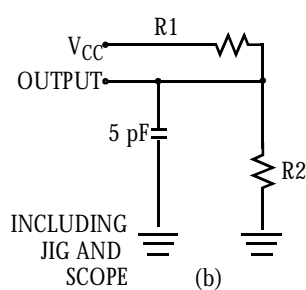
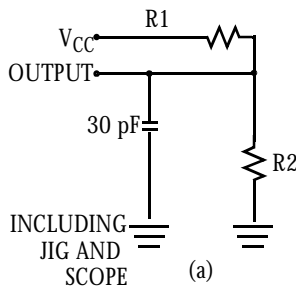
Data retention characteristics (over the operating range)

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|--------------------------------------|------------|--|----------|-----|------|
| V_{CC} for data retention | V_{DR} | $V_{CC} = 1.2V$ | 1.2V | 3.3 | V |
| Data retention current | I_{CCDR} | $\overline{CS} \geq V_{CC} - 0.1V$ or $\overline{UB} = \overline{LB} = > V_{CC} - 0.1V$ | – | 2 | mA |
| Chip deselect to data retention time | t_{CDR} | $V_{IN} \geq V_{CC} - 0.1V$ or $V_{IN} \leq 0.1V$ | 0 | – | ns |
| Operation recovery time | t_R | | t_{RC} | – | ns |

Data retention waveform



AC test loads and waveforms



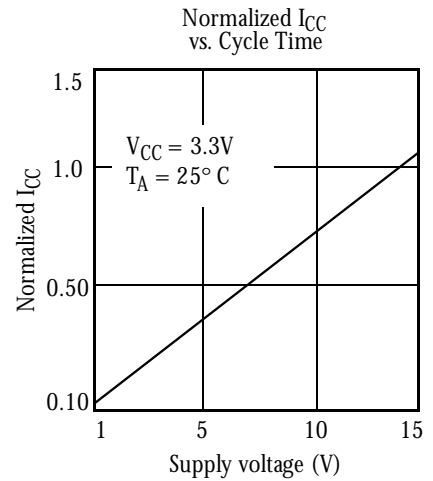
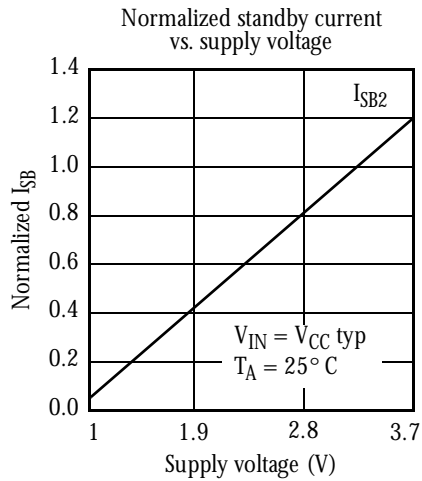
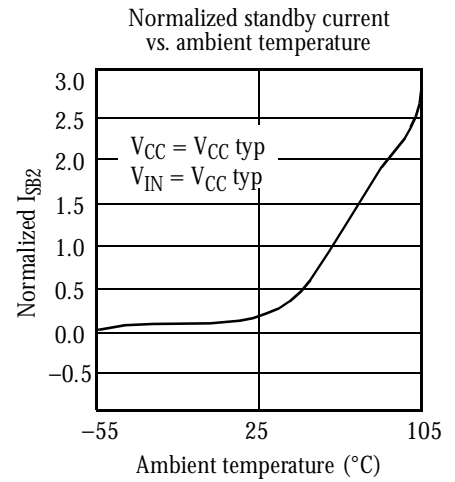
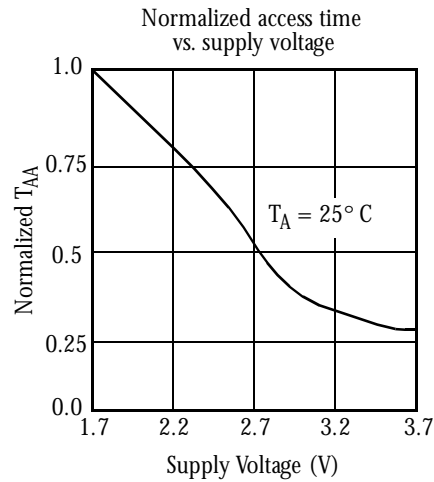
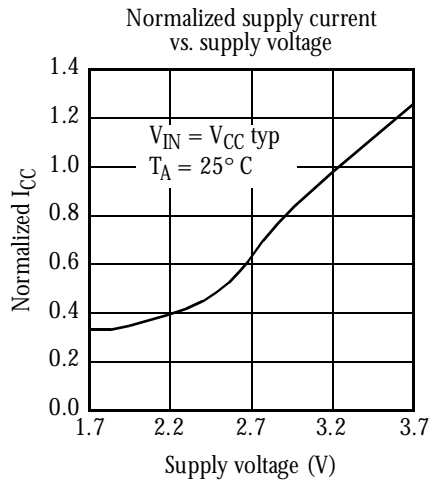
| Parameters | $V_{CC} = 3.0V$ | $V_{CC} = 2.5V$ | $V_{CC} = 2.0V$ | Unit |
|------------|-----------------|-----------------|-----------------|-------|
| R1 | 1105 | 16670 | 15294 | Ohms |
| R2 | 1550 | 15380 | 11300 | Ohms |
| R_{TH} | 645 | 8000 | 6500 | Ohms |
| V_{TH} | 1.75V | 1.2V | 0.85V | Volts |

Notes

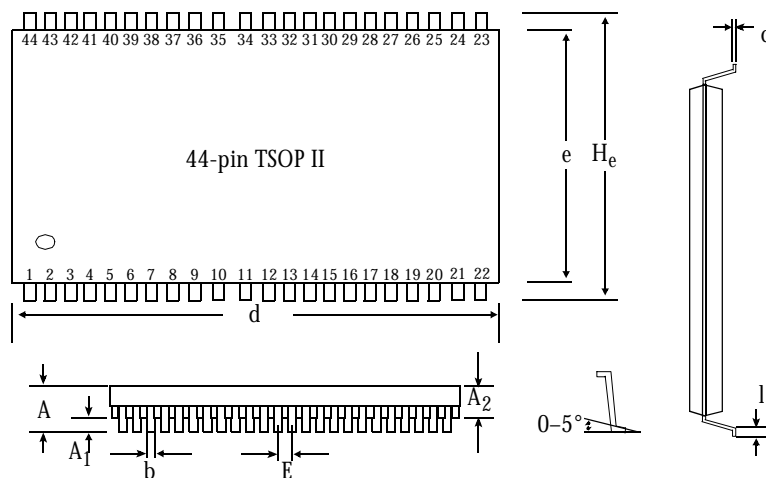
- During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CS} is required to meet I_{KB} specification.
- This parameter is sampled, but not 100% tested.
- For test conditions, see AC Test Conditions.
- t_{CLZ} and t_{CHZ} are specified with $C_L = 5pF$ as in Figure C. Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed, but not tested.
- \overline{WE} is HIGH for read cycle.
- \overline{CS} and \overline{OE} are LOW for read cycle.
- Address valid prior to or coincident with \overline{CS} transition LOW.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- \overline{CS} or \overline{WE} must be HIGH during address transitions. Either \overline{CS} or \overline{WE} asserting high terminates a write cycle.
- All write cycle timings are referenced from the last valid address to the first transitioning address.
- N/A.
- 1.2V data retention applies to commercial and industrial temperature range operations.
- $C = 30pF$, except at high Z and low Z parameters, where $C = 5pF$.



Typical DC and AC characteristics



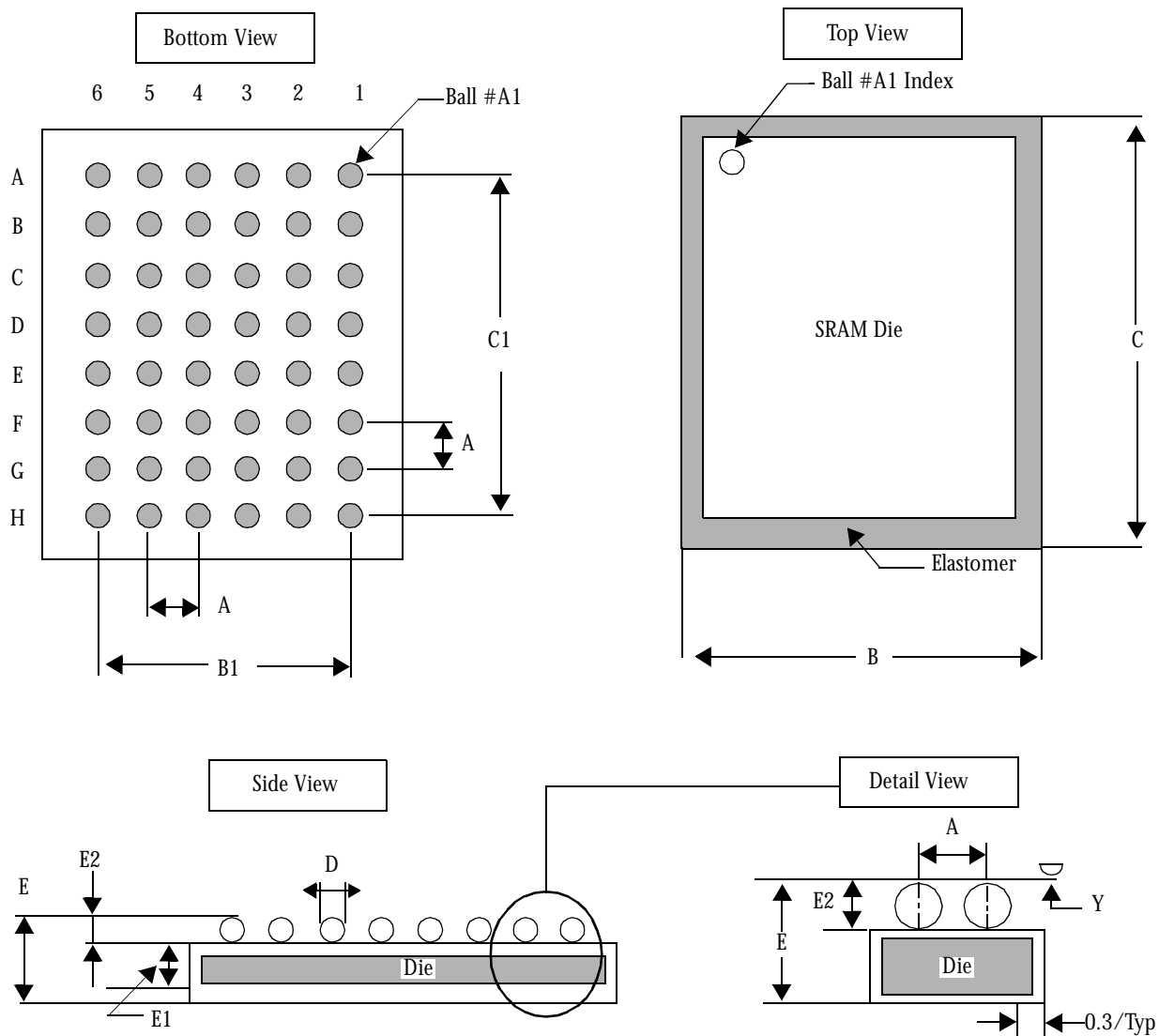
Package diagrams and dimensions



| | 44-pin TSOP II | |
|----------------|----------------|----------|
| | Min (mm) | Max (mm) |
| A | 1.2 | |
| A ₁ | 0.05 | |
| A ₂ | 0.95 | 1.05 |
| b | 0.25 | 0.45 |
| c | 0.15 (typical) | |
| d | 18.28 | 18.54 |
| e | 10.06 | 10.26 |
| He | 11.56 | 11.96 |
| E | 0.80 (typical) | |
| l | 0.40 | 0.60 |



48-ball FBGA



| | Minimum | Typical | Maximum |
|----|---------|---------|---------|
| A | – | 0.75 | – |
| B | 6.90 | 7.00 | 7.10 |
| B1 | – | 3.75 | – |
| C | 10.90 | 11 | 11.10 |
| C1 | – | 5.25 | – |
| D | 0.30 | 0.35 | 0.40 |
| E | – | – | 1.20 |
| E1 | – | 0.68 | – |
| E2 | 0.22 | 0.25 | 0.27 |
| Y | – | – | 0.08 |

Notes

1. Bump counts: 48 (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerance are ±0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.08 (max).



Ordering codes

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|------------|---------------|------------------------|-----------------|
| 55 | AS6VA25616-TC | 44-pin TSOP II | Commercial |
| | AS6VA25616-BC | 48-ball fine pitch BGA | |
| 55 | AS6VA25616-TI | 44-pin TSOP II | Industrial |
| | AS6VA25616-BI | 48-ball fine pitch BGA | |

Part numbering system

| AS6VA | 25616 | T, B | C, I |
|-------------------------|---------------|--------------------------------------|--|
| SRAM Inteliwatt™ prefix | Device number | Package: T: TSOP II B: CSP BGA | Temperature range: C: Commercial: 0° C to 70° C I: Industrial: -40° C to 85° C |