Product Brief

T-52-23-05

Bipolar Integrated Technology Inc.

HIPPI Interface Chip Set

(32- and/or 64-Bit)

B2022 - HIPPI Source Interface Chip
B2023 - HIPPI Destination Interface Chip

The B2022 and B2023 are BIT's implementation of the single chip Parallel HIPPI Source and Destination Interfaces. They provide the data path and control logic and the drivers and receivers required for a complete 32-bit Parallel HIPPI link. In addition, they provide a set of synchronization signals that allow cascading for 64-bit Parallel HIPPI operation.

Features:

- Functional compliance with ANSI X3T9.3 HIPPI-PH Specifications Rev. 8.0.
- Excellent timing characteristics allowing for ease of design.
- Efficient power and thermal characteristics.
- Control and error signal operation.
- 32-bit data channel, cascadable for 64-bit operation or 32/64-bit operation.
- Single channel (32-bit) data rate of 800 megabits per second, dual channel (64-bit) data rate of 1.6 gigabits per second.
- Data and control signal sequencing in accordance with the HIPPI Physical Framing Hierarchy.
- Automatic division of data into HIPPI bursts.
- Automatic LLRC and LLRC parity generation.
- Automatic LLRC and parity checking.
- Capable of handling up to 65,535 look-ahead ready pulses.
- Differential 10K ECL HIPPI link interface.
- Single-ended TTL host interface.
- Seamless interface to external FIFO's.
- Self-test diagnostic modes of operation.
- Maximum request/connection latency of 600 ns (not counting destination host response time).
- Maximum data latency of 400 ns.
- Full scan for board level observability.
- 225-lead pin-grid-array package.

General Description:

The B2022 and B2023 provide complete functionality for interfacing a source host device to a destination host device across a 32-bit Parallel HIPPI link.

The B2022 is designed to receive data and parity from a source FIFO and receive control information from the source FIFO and source host logic. It automatically controls the interconnect, request/connection, and data transmission sequences to operate within the HIPPI specifications. It blocks the received data and parity into HIPPI bursts, automatically generates the Length/Longitudinal Redundancy (LLRC) check word and the LLRC parity, and transmits the data, parity, and source-to-destination control signals across the HIPPI link. It receives and synchronizes the destination-to-source control signals and uses them for interconnect, connect, and source data flow control.

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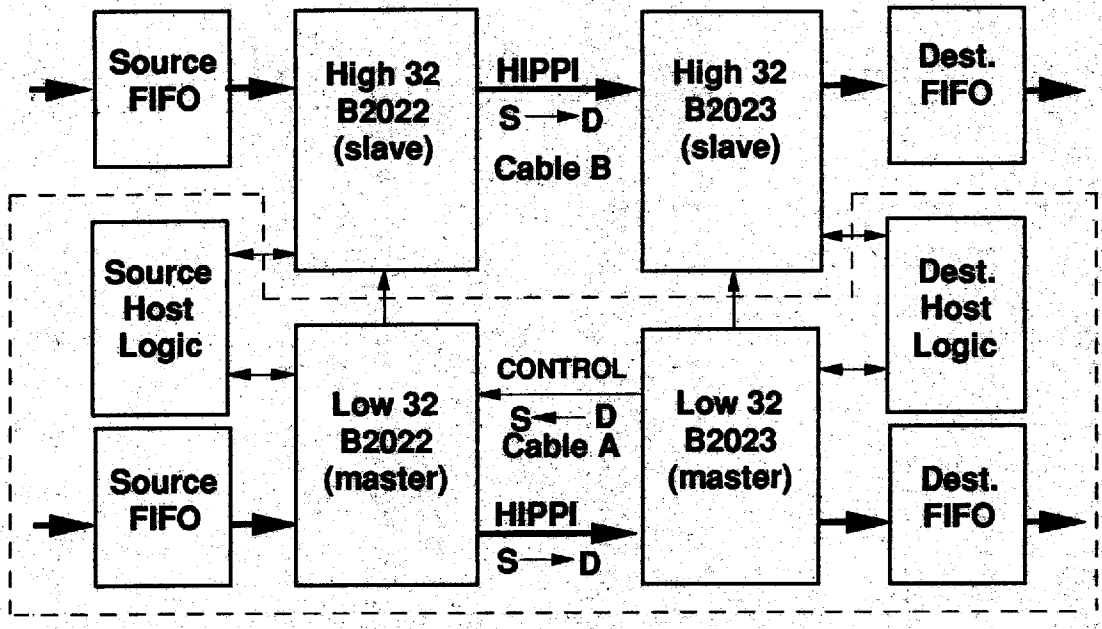
Functional Description:

The B2023 is designed to receive HIPPI data, parity, and source-to-destination control signals and synchronize them to the destination clock. It uses the control signals to determine how to treat the received data and parity and it automatically checks the parity of HIPPI I-Field, burst, and LLRC data and checks the LLRC word at the end of each burst. It also keeps track of the number of burst sized buffers available at the destination and generates the appropriate number of look-ahead ready pulses to the source for data flow control. It communicates with the destination host logic in performing the HIPPI request/connection sequences and in controlling the reception of data and parity into the destination FIFO. The destination synchronization circuit contains an elastic buffer that allows the received HIPPI signals to ship, jitter, or drift back and forth with relation to the destination clock without losing data or control information.

A 64-bit Parallel HIPPI Link can be constructed from two B2022 source chips, two B2023 destination chips, and two HIPPI cables.

The source chip that handles the low 32 bits of data acts as the master of the two-chip source interface. It receives the destination-to-source control signals, synchronizes them to the source clock, and presents them to both source chips for synchronous operation.

The destination chip that handles the low 32 bits of data acts as the master of the two-chip destination interface. It receives the source-to-destination interconnect signals and synchronizes them to the destination clock. It also generates a pair of synchronous signals that locate the HIPPI clock falling edge with respect to the destination clock. These signals are presented to both destination chips to ensure synchronous operation. The rest of the HIPPI control signals are also fed to both destination chips.



64-Bit Parallel HIPPI Link *(32-Bit Parallel Link [ ])*

In addition, the host-side input signals are synchronously fed to both chips in a source or destination. The simultaneous reception of all the control signals ensures both chips at each end of the link react to the outside stimulus in precise lock step.

These chips are fabricated with BIT's unique VLSI process that allows for a high level of density and integration while consuming power levels comparable to BiCMOS processes.

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