

TrenchMOS™ transistor

Logic level FET

BUK9515-100A

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology which features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

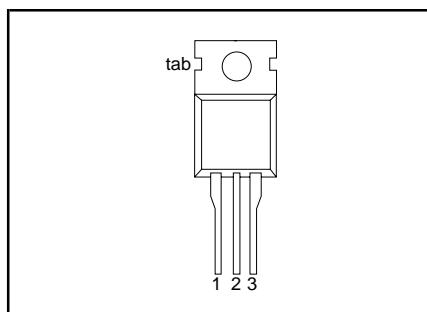
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	230	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	15	$m\Omega$
	$V_{GS} = 5 \text{ V}$	14.4	$m\Omega$
	$V_{GS} = 10 \text{ V}$		

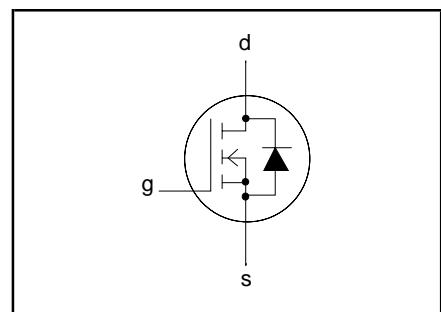
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50 \mu\text{s}$	-	15	V
I_D	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	75	A
I_D	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	53	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	240	A
P_{tot}	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	230	W
T_{stg}, T_j	Storage & operating temperature	-	-55	175	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th j-mb}$	Thermal resistance junction to mounting base	-	-	0.65	K/W
$R_{th j-a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

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STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$; $T_j = -55^\circ\text{C}$	100	-	-	V
$V_{GS(\text{TO})}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$; $T_j = 175^\circ\text{C}$	89	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}$; $T_j = -55^\circ\text{C}$	1	1.5	2.0	V
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10 \text{ V}; V_{DS} = 0 \text{ V}$; $T_j = 175^\circ\text{C}$	0.5	-	-	V
$R_{DS(\text{ON})}$	Drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}$; $T_j = 175^\circ\text{C}$	-	0.05	10	μA
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}$; $T_j = 175^\circ\text{C}$	-	-	500	μA
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}$; $T_j = 175^\circ\text{C}$	-	2	100	nA
			-	12.0	15.0	$\text{m}\Omega$
			-	-	40.5	$\text{m}\Omega$
			-	11.5	14.4	$\text{m}\Omega$
			-	-	16.0	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

$T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	6500	8600	pF
C_{oss}	Output capacitance		-	550	660	pF
C_{rss}	Feedback capacitance		-	325	400	pF
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30 \text{ V}; R_{\text{load}} = 1.2\Omega$	-	45	65	ns
t_r	Turn-on rise time	$V_{GS} = 5 \text{ V}; R_G = 10 \Omega$	-	130	195	ns
$t_{d\text{ off}}$	Turn-off delay time		-	400	560	ns
t_f	Turn-off fall time		-	130	190	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	$I_F = 25 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.85	1.2	V
		$I_F = 75 \text{ A}; V_{GS} = 0 \text{ V}$	-	1.1	-	V
t_{rr}	Reverse recovery time	$I_F = 75 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	80	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10 \text{ V}; V_R = 30 \text{ V}$	-	0.35	-	μC

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AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 35 \text{ A}$; $V_{DD} \leq 25 \text{ V}$; $V_{GS} = 5 \text{ V}$; $R_{GS} = 50 \Omega$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	120	mJ

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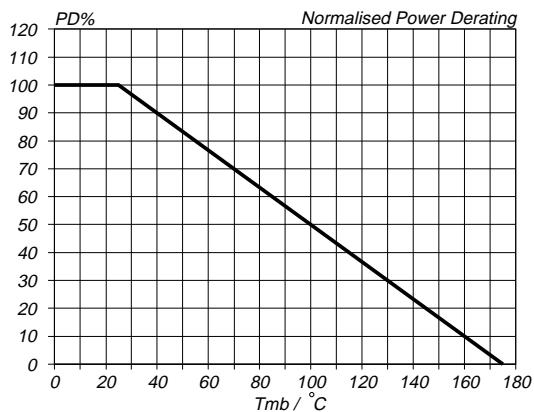


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D/P_{D,25^\circ C} = f(T_{mb})$

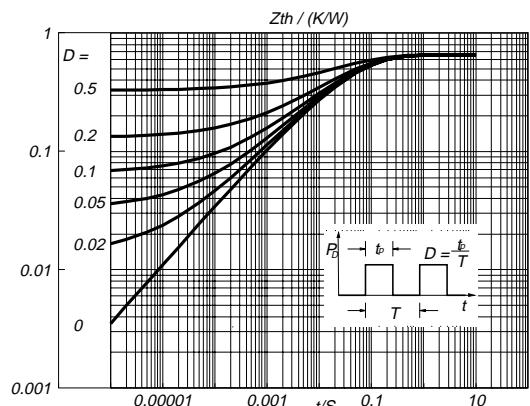


Fig.4. Transient thermal impedance.
 $Z_{th,j-mb} = f(t)$; parameter $D = t_p/T$

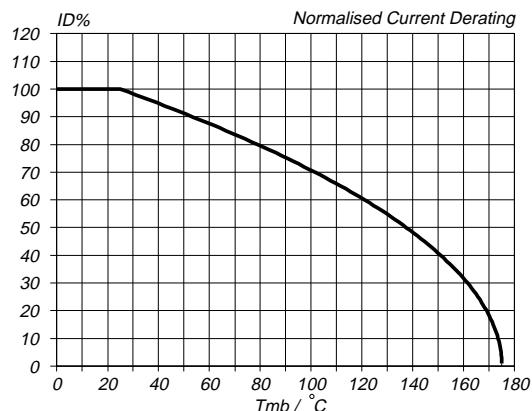


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D/I_{D,25^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 5 V$

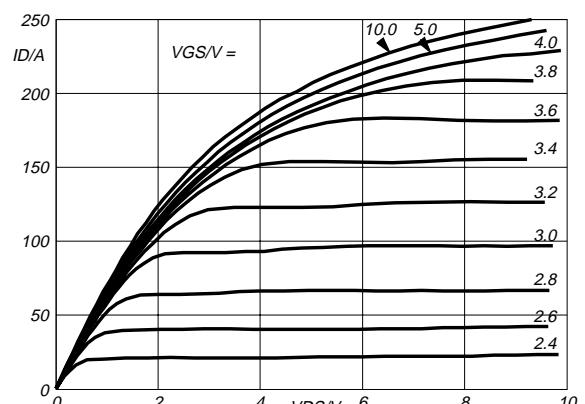


Fig.5. Typical output characteristics, $T_j = 25^\circ C$.
 $I_D = f(V_{DS})$; parameter V_{GS}

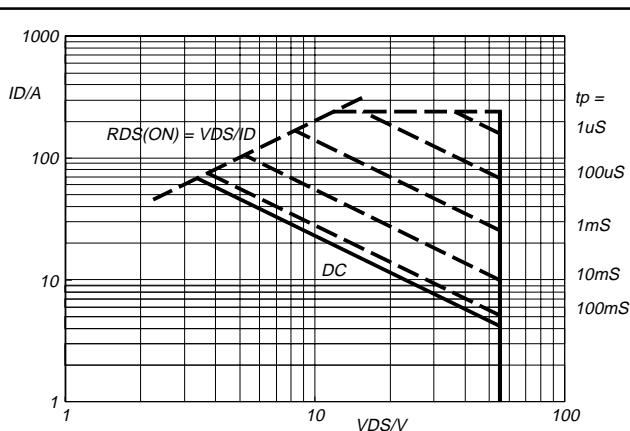


Fig.3. Safe operating area. $T_{mb} = 25^\circ C$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

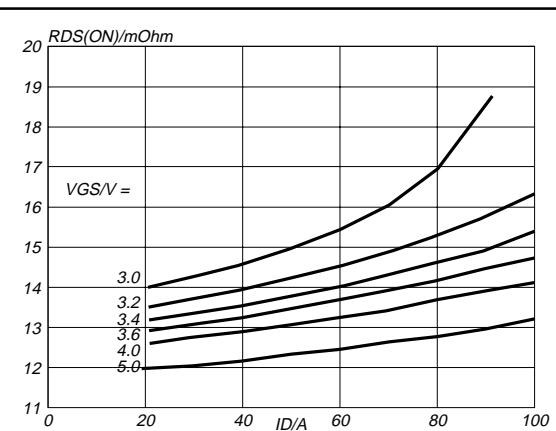


Fig.6. Typical on-state resistance, $T_j = 25^\circ C$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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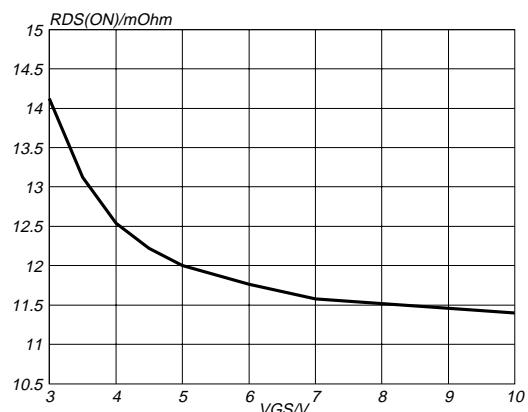


Fig.7. Typical on-state resistance, $T_j = 25^\circ C$.
 $R_{DS(ON)} = f(V_{GS})$; conditions: $I_D = 25 A$;

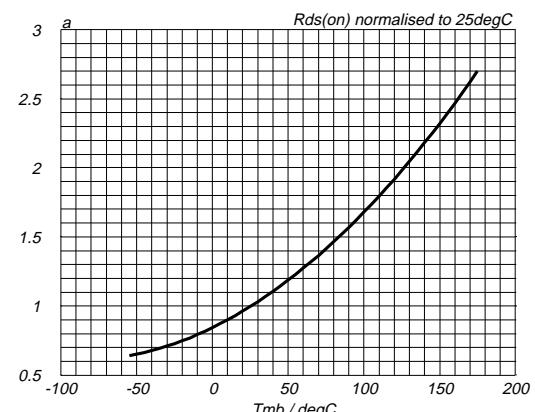


Fig.10. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ C} = f(T_j)$; $I_D = 25 A$; $V_{GS} = 5 V$

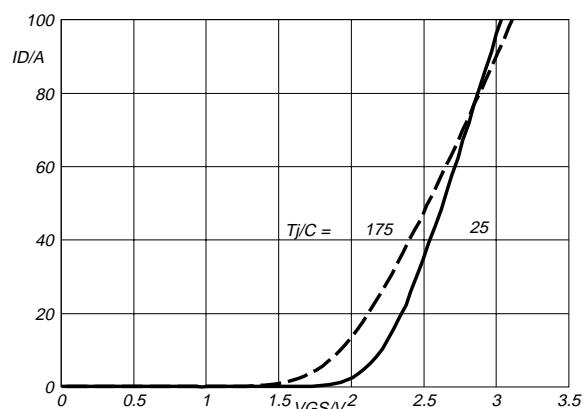


Fig.8. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25 V$; parameter T_j

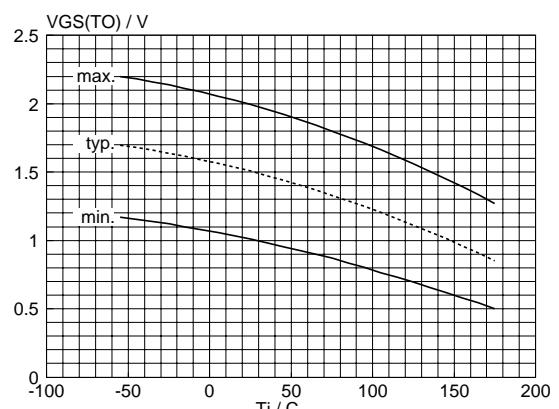


Fig.11. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1 mA$; $V_{DS} = V_{GS}$

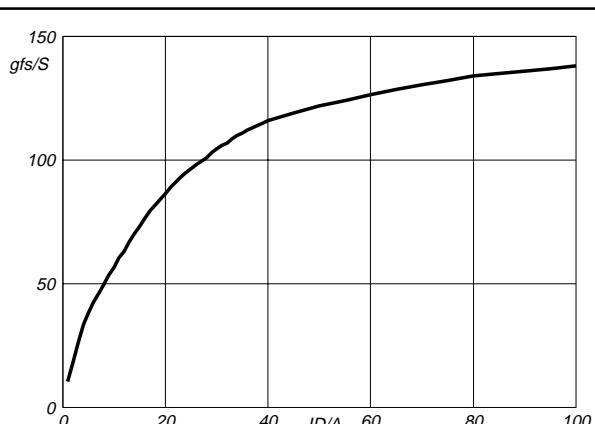


Fig.9. Typical transconductance, $T_j = 25^\circ C$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25 V$

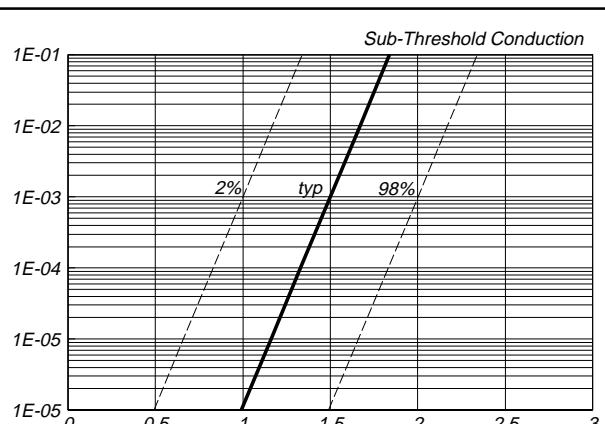


Fig.12. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ C$; $V_{DS} = V_{GS}$

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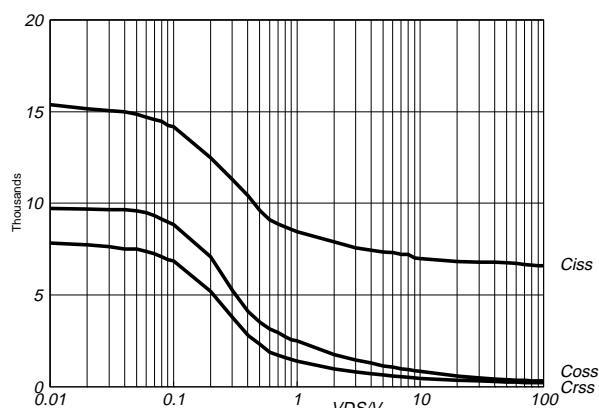


Fig.13. Typical capacitances, C_{iss} , C_{ooss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

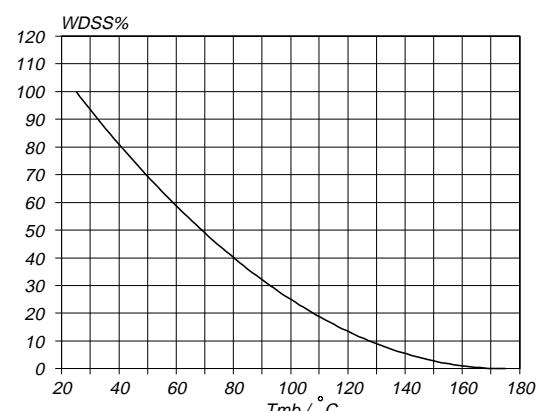


Fig.16. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

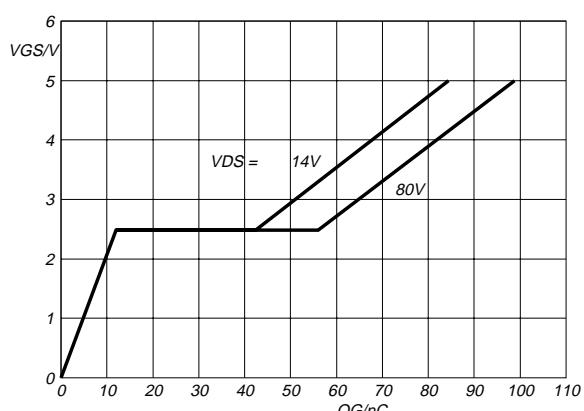


Fig.14. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 25$ A; parameter V_{DS}

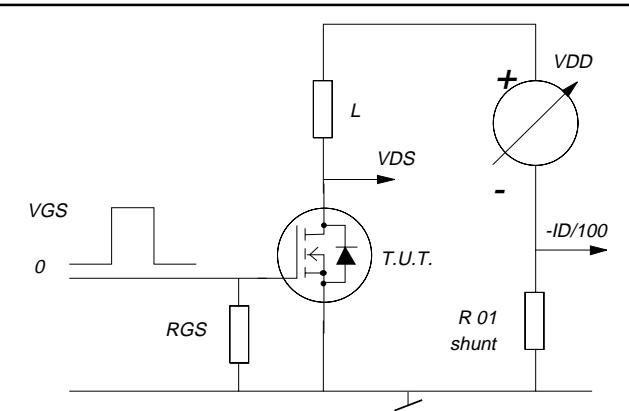


Fig.17. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

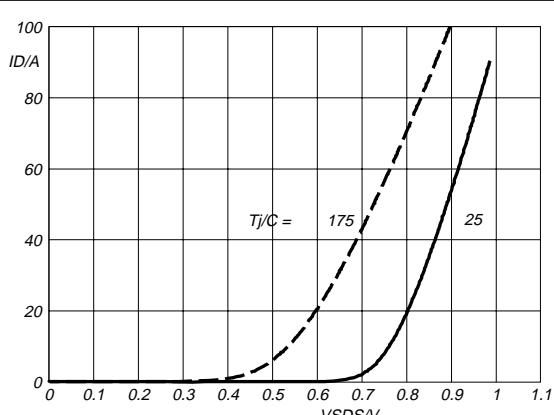


Fig.15. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

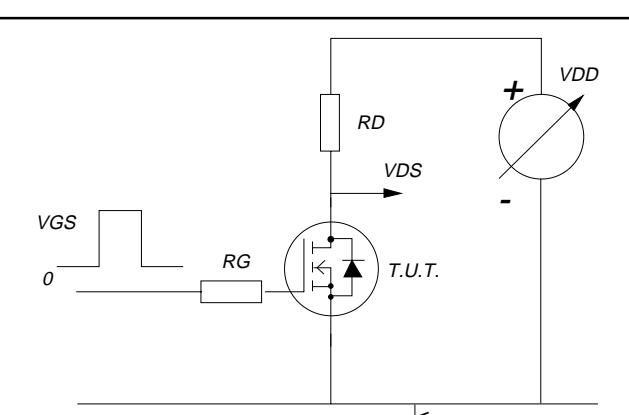


Fig.18. Switching test circuit.

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MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g



Fig.19. SOT78 (TO220AB); pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

**TrenchMOS™ transistor
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Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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