High Speed 512K x 8Bit CMOS Dynamic RAM with with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Access time (-4), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 512Kx8 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for microcomputer, personal computer and portable machines.

FEATURES

- **Part Identification**

  - KM48C512D/DL (5V, 1K Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	Active Power Dissipation
-4	770

- **Refresh Cycles**

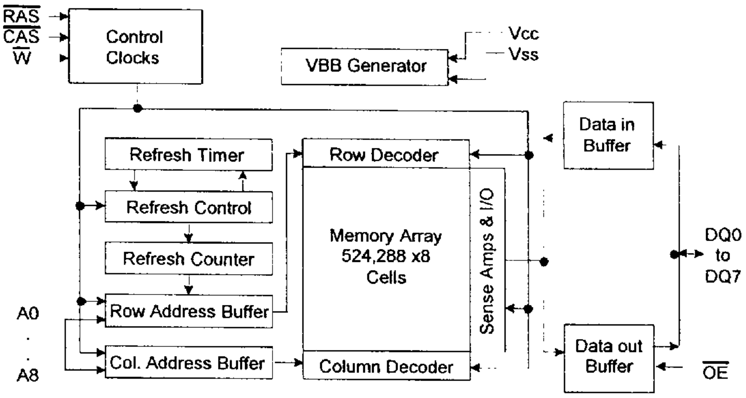
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C512D	5V	1K	16ms	128ms

- **Perfomance Range:**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-4	40ns	12ns	75ns	28ns

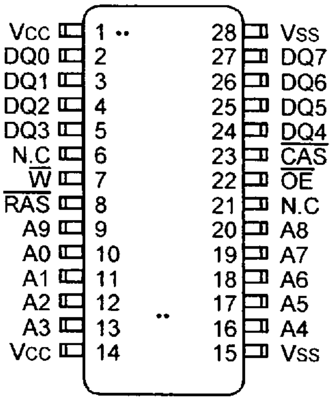
- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 28-pin SOJ 400mil & 28-pin TSOP(II) 400mil packages
- Dual +5V••10% power supply

FUNCTIONAL BLOCK DIAGRAM



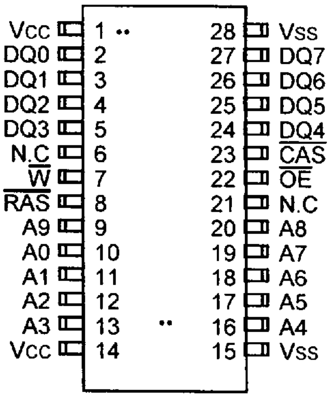
PIN CONFIGURATION (Top Views)

KM48C512DJ



(SOJ)

KM48C512DT



(TSOP-II)

Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 - 7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	••
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70••)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1.0[*1]	V
Input Low Voltage	V_{IL}	-1.0[*2]	-	0.8	V

[*1] : V_{CC}+2.0/20ns(5V), Pulse width is measured at V_{CC}

[*2] : -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0••V_{IN}••V_{IN}+0.5V, all other input pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V••V_{OUT}••V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Max	Units
I_{CC1}	Don't care	140	mA
I_{CC2}	Don't care	2	mA
I_{CC3}	Don't care	140	mA
I_{CC4}	Don't care	110	mA
I_{CC5}	Normal L	1 150	mA uA
I_{CC6}	Don't care	140	mA
I_{CC7}	L	300	uA
I_{CCS}	L	200	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V,
Din=Don't care, T_{RC}=31.25us, T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 =V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ7=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25••, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0••••T_A••70••, See note 1,2)

Test condition : V_{CC}=5.0V••10%, Vih/Vil=2.8/0.4V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-4		Units	Note
		Min	Max		
Random read or write cycle time	t_{RC}	75		ns	
Read-modify-write cycle time	t_{RWC}	111		ns	
Access time from $\overline{RAS}$	t_{RAC}		40	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		12	ns	3,4,5
Access time from column address	t_{AA}		20	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		ns	3
Output buffer turn-off dealy	t_{OFF}	0	9	ns	6
Transition time (rise and fall)	t_T	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	25		ns	
$\overline{RAS}$ pulse width	t_{RAS}	40	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	12		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	28	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		ns	
Row address set-up time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	8		ns	
Column address set-up time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	20		ns	
Read command set-up time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		ns	8
Write command set-up time	t_{WCS}	0		ns	7
Write command hold time	t_{WCH}	10		ns	
Write command pulse width	t_{WP}	10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	12		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	12		ns	

* 0••••T_A••60••, Output Loading(C_L) = 30pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-4		Units	Note
		Min	Max		
Data set-up time	t_{DS}	0		ns	9
Data hold time	t_{DH}	10		ns	9
Refresh period (Normal)	t_{REF}		16	ms	
Refresh period (L-ver)	t_{REF}		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t_{CWD}	31		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t_{RWD}	59		ns	7
Column address $\overline{\text{W}}$ delay time	t_{AWD}	39		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t_{CPWD}	44			7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before-$\overline{\text{RAS}}$ refresh)	t_{CSR}	10		ns	
$\overline{\text{CAS}}$ hlod time ($\overline{\text{CAS}}$ -before-$\overline{\text{RAS}}$ refresh)	t_{CHR}	10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	5		ns	
$\overline{\text{CAS}}$ precharge time (CBR counter test cycle)	t_{CPT}	20		ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}		25	ns	3
Fast Page mode cycle time	t_{PC}	28		ns	
Fast Page read-modify-write cycle time	t_{PRWC}	67		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	t_{CP}	6		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t_{RASP}	40	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	23		ns	
$\overline{\text{OE}}$ access time	t_{OEA}		12	ns	
$\overline{\text{OE}}$ to data delay	t_{OED}	9		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	9	ns	6
$\overline{\text{OE}}$ command hold time	t_{OEH}	12		ns	
$\overline{\text{RAS}}$ pulse width (C-B-R self refresh)	t_{RASS}	100		us	11
$\overline{\text{RAS}}$ precharge time (C-B-R self refresh)	t_{RPS}	74		ns	11
$\overline{\text{CAS}}$ hold time (C-B-R self refresh)	t_{CHS}	-50		ns	11

* 0••••T_A••60••, Output Loading(C_L) = 30pF

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or $\overline{CBR}$ cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 30pF. Dout reference level : Voh/Vol=2.0V/0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD}••t_{RCD}(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}••t_{WCS}(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{CWD}••t_{CWD}(min), t_{RWD}••t_{RWD}(min), t_{AWD}••t_{AWD}(min) and t_{CPWD}••t_{CPWD}(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. This parameters are referenced to the $\overline{CAS}$ falling edge in ealy write cycles and to the $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. 1024cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).