Document Title

256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	October 2, 1996	Advance
0.1	Revise - Remove sTSOP1 from product - Rename high power product to low power. I_{SB1}=10.0mA(Max) - Add super low power version with special handling I_{SB1}=1.0mA(Max) - Remove 70ns and add 85ns part on KM68FS2000 Family	December 1, 1996	Preliminary
1.0	Finalize	April 11, 1997	Final
2.0	Revise - Change datasheet format - Remove reverse type package from product - Remove reseved speed bin(100ns)	March 5, 1998	Final

256Kx8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 256Kx8
- Power Supply Voltage
  - KM68FV2000 Family : 3.0 ~ 3.6V
  - KM68FS2000 Family : 2.3 ~ 3.3V
  - KM68FR2000 Family : 1.8 ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 32-TSOP1-0820F

GENERAL DESCRIPTION

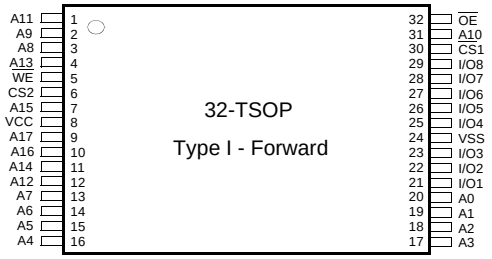
The KM68FV2000, KM68FS2000 and KM68FR2000 families are fabricated by SAMSUNG′s advanced Full CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM68FV2000	Commercial(0~70°C)	3.0~3.6V	70[1]/85@V_{CC}=3.3±0.3V	10mA[2]	60mA	32-TSOP1-F
KM68FS2000		2.3~3.3V	85@V_{CC}=3.0±0.3V		55mA	
			120[1]/150@V_{CC}=2.5±0.2V		30mA	
KM68FR2000		1.8~2.7V	300[1]@V_{CC}=2.0±0.2V		15mA	
KM68FV2000I	Industrial(-40~85°C)	3.0~3.6V	70[1]/85@V_{CC}=3.3±0.3V		60mA	
KM68FS2000I		2.3~3.3V	85@V_{CC}=3.0±0.3V		55mA	
			120[1]/150@V_{CC}=2.5±0.2V		30mA	
KM68FR2000I		1.8~2.7V	300[1]@V_{CC}=2.0±0.2V		15mA	

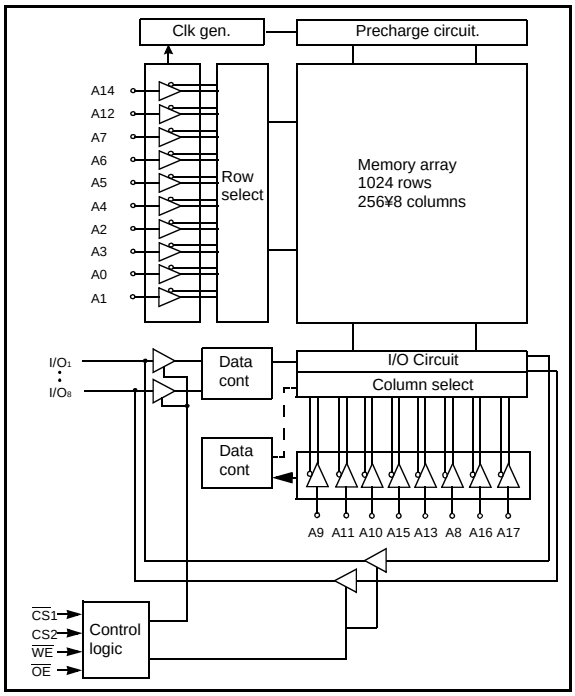
1. The parameter is measured with 30pF test load.
2. 2mA for super low power version with special handling.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS_1}$,CS_2	Chip Select Input	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A_0~A_{17}	Address Inputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM68FV2000T-7	32-TSOP F, 70ns, 3.3V, LL	KM68FV2000TI-7	32-TSOP F, 70ns, 3.3V, LL
KM68FV2000T-8	32-TSOP F, 85ns, 3.3V, LL	KM68FV2000TI-8	32-TSOP F, 85ns, 3.3V, LL
KM68FS2000T-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL	KM68FS2000TI-12	32-TSOP F, 120/85ns, 2.5/3.0V, LL
KM68FS2000T-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL	KM68FS2000TI-15	32-TSOP F, 150/85ns, 2.5/3.0V, LL
KM68FR2000T-30	32-TSOP F, 300ns, 2.0/2.5V, LL	KM68FR2000TI-30	32-TSOP F, 300ns, 2.0/2.5V, LL

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	X[1)]	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disable	Active
L	H	L	H	Dout	Read	Active
L	H	X[1)]	L	Din	Write	Active

1. X means don't care (Must be high or low states)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V[2)]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[3)]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM68FV2000, KM68FS2000, KM68FR2000
		-40 to 85	°C	KM68FV2000I, KM68FS2000I, KM68FR2000I
Soldering temperature and time	T_{SOLDER}	260°C, 5sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN}/V_{OUT}=-0.2 to 3.9V for KM68FV2000 Family.
3. Maximum V_{CC}=-0.2 to 4.6V for KM68FV2000 Family.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product		Min	Typ[2)]	Max	Unit
Supply voltage	Vcc	KM68FV2000 Family KM68FS2000 Family KM68FR2000 Family		3.0 2.3 1.8	3.3 2.5/3.0 2.0/2.5	3.6 3.3 2.7	V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM68FV2000 Family	Vcc=3.3±0.3V	2.2	-	Vcc+0.2[2)]	V
		KM68FS2000 Family	Vcc=3.0±0.3V	2.2			
			Vcc=2.5±0.2V	2.0			
		KM68FR2000 Family	Vcc=2.5±0.2V	2.0			
			Vcc=2.0±0.2V	1.6			
Input low voltage	V_{IL}	All Family		-0.2[3)]	-	0.4	V

Note
1. Commercial Product : T_A=0 to 70°C, unless otherwise specified
   Industrial Product : T_A=-40 to 85°C, unless otherwise specified
2. Overshoot : Vcc + 1.0V in case of pulse width≤20ns
3. Undershoot : -1.0V in case of pulse width≤20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

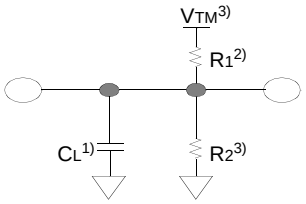
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	mA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	mA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	10	mA
Average operating current	I_{CC1}	Cycle time=1μs, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	Read	-	-	10	mA
			Write	-	-	15	
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	Vcc=3.3V@70ns	-	-	55[1)]	mA
			Vcc=2.7V@120ns	-	-	30	
			Vcc=2.2V@300ns	-	-	15	
Output low voltage	V_{OL}	I_{OL}	2.1mA at Vcc=3.0/3.3V	-	-	0.4	V
			0.5mA at Vcc=2.5V	-	-	0.4	
			0.33mA at Vcc=2.0V	-	-	0.4	
Output high voltage	V_{OH}	I_{OH}	-1.0mA at Vcc=3.0/3.3V	2.4	-	-	V
			-0.5mA at Vcc=2.5V	2.0	-	-	
			-0.44mA at Vcc=2.0V	1.6	-	-	
Standby Current(TTL)	I_{SB}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, Other inputs=V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V, CS2≥Vcc-0.2V or CS_2≤0.2V, Other inputs=0~Vcc		-	-	10[2)]	mA

1.The value is measured at Vcc=3.0±0.3V
   - ICC2=60mA with 70ns at Vcc=3.3±0.3V, but this value is not 100% tested but obtained statistically.
2. Super low power product = 2mA with special handling.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V
0.4 to 1.8V for Vcc=2.0V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V
1.1V for Vcc=2.5V
0.9V for Vcc=2.0V
Output load (See right) : C_L=100pF+1TTL
C_L=30pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070W, R_2=3150W
3. V_{TM} =2.8V for V_{CC}=3.0/3.3V
=2.3V for V_{CC}=2.5V
=1.8V for V_{CC}=2.0V

AC CHARACTERISTICS

(Commercial product : T_A=0 to 70°C, Industrial product : T_A=-40 to 85°C
KM68FV2000 Family : Vcc=3.0~3.6V, KM68FS2000 Family : Vcc=2.3~3.3V,
KM68FR2000 Family : Vcc=1.8~2.7V)

Parameter List		Symbol	Speed Bins										Units
			70ns		85ns		120ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	70	-	85	-	120	-	150	-	300	-	ns
	Address access time	t_{AA}	-	70	-	85	-	120	-	150	-	300	ns
	Chip select to output	t_{CO1}, t_{CO2}	-	70	-	85	-	120	-	150	-	300	ns
	Output enable to valid output	t_{OE}	-	35	-	45	-	60	-	75	-	150	ns
	Chip select to low-Z output	t_{LZ1}, t_{LZ2}	10	-	10	-	10	-	20	-	50	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	10	-	30	-	ns
	Chip disable to high-Z output	t_{HZ1}, t_{HZ2}	0	25	0	25	0	35	0	40	0	60	ns
	Output disable to high-Z output	t_{OHZ}	0	25	0	25	0	35	0	40	0	60	ns
	Output hold from address change	t_{OH}	10	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	t_{WC}	70	-	85	-	120	-	150	-	300	-	ns
	Chip select to end of write	t_{CW}	65	-	70	-	100	-	120	-	300	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	65	-	70	-	100	-	120	-	300	-	ns
	Write pulse width	t_{WP}	55	-	60	-	80	-	100	-	200	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	25	0	35	0	40	0	60	ns
	Data to write time overlap	t_{DW}	30	-	35	-	50	-	60	-	120	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	5	-	5	-	20	-	ns

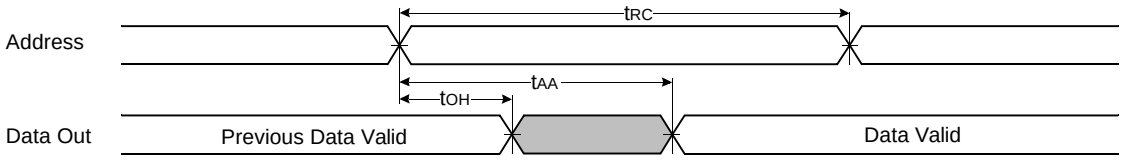
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1}$≥Vcc-0.2V[1)]	1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS_1}$≥Vcc-0.2V[1)]	-	-	10[2)]	mA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t_{RDR}		t_{RC}	-	-	

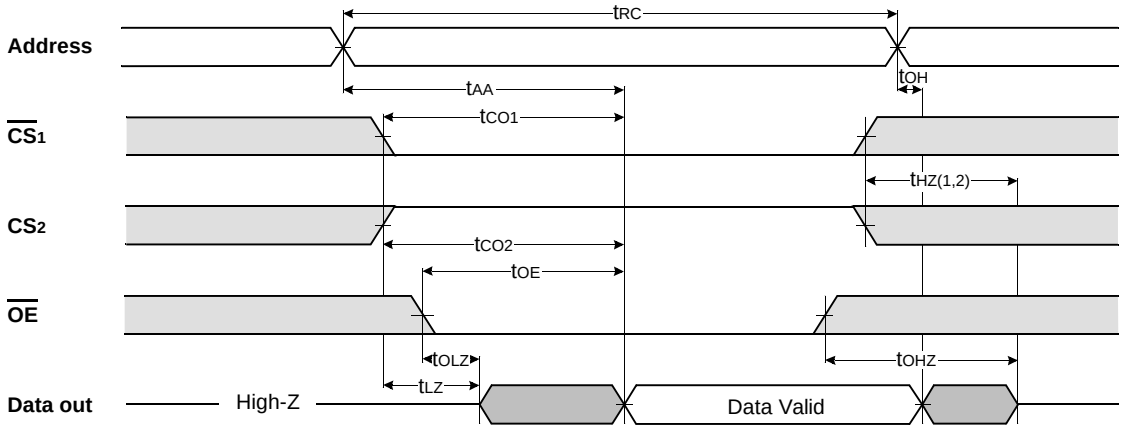
1. $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V($\overline{CS_1}$ controlled) or CS_2≤0.2V(CS_2 controlled)
2. Super low power product = 2mA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}1=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



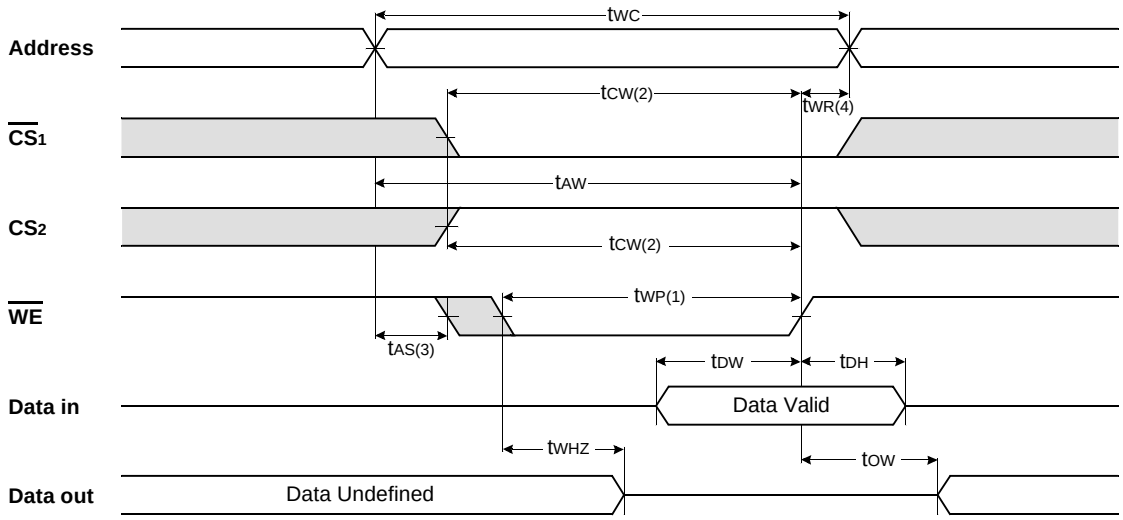
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



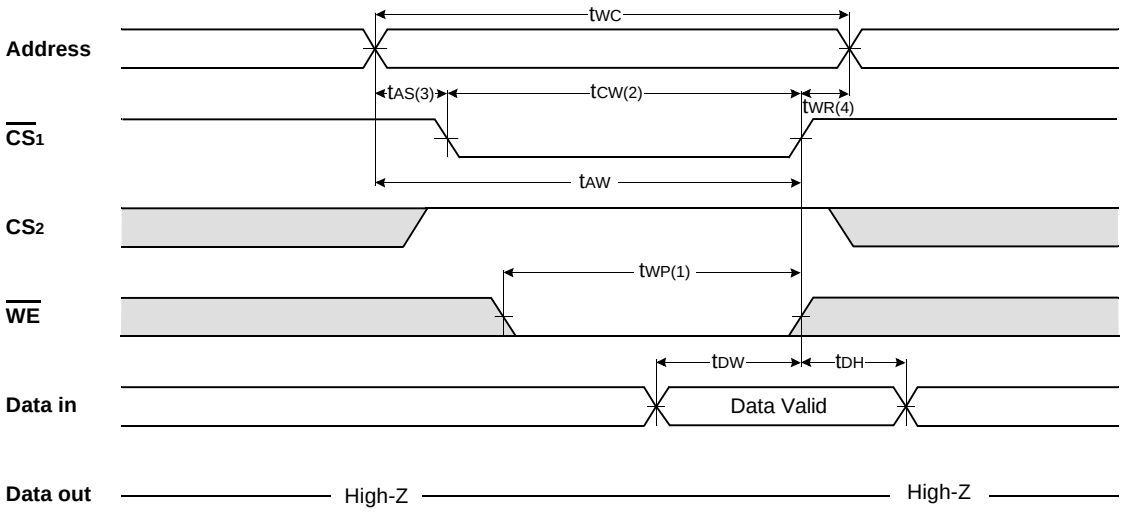
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

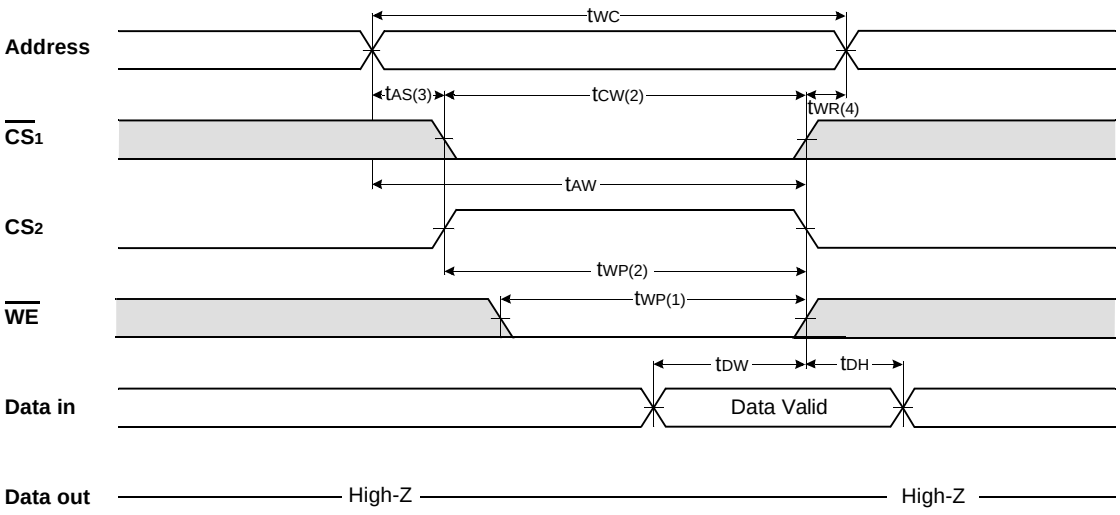
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS_1}$ Controlled)

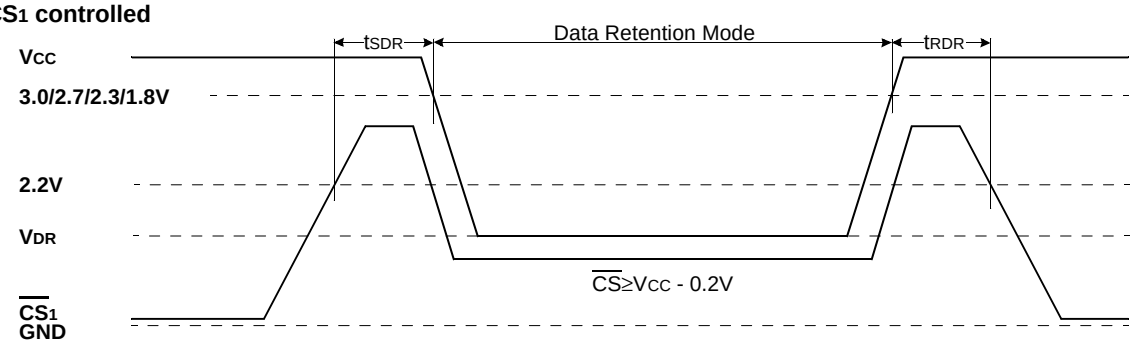


NOTES (WRITE CYCLE)

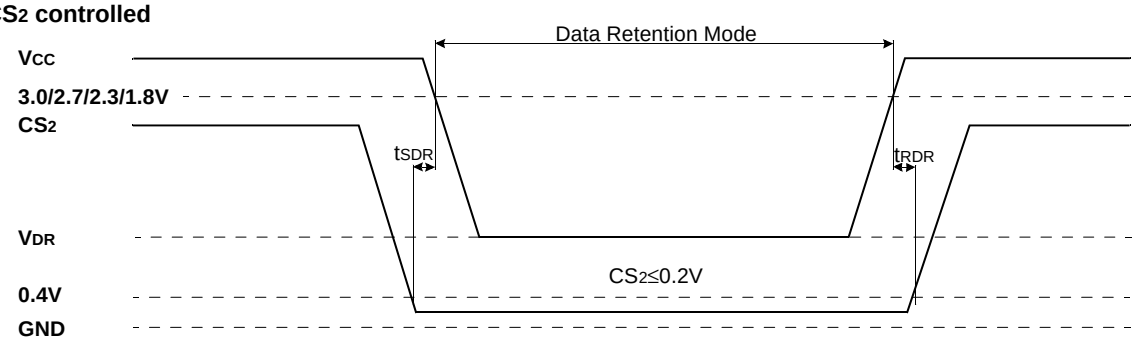
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS_2 controlled



PACKAGE DIMENSIONS

Units : millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)