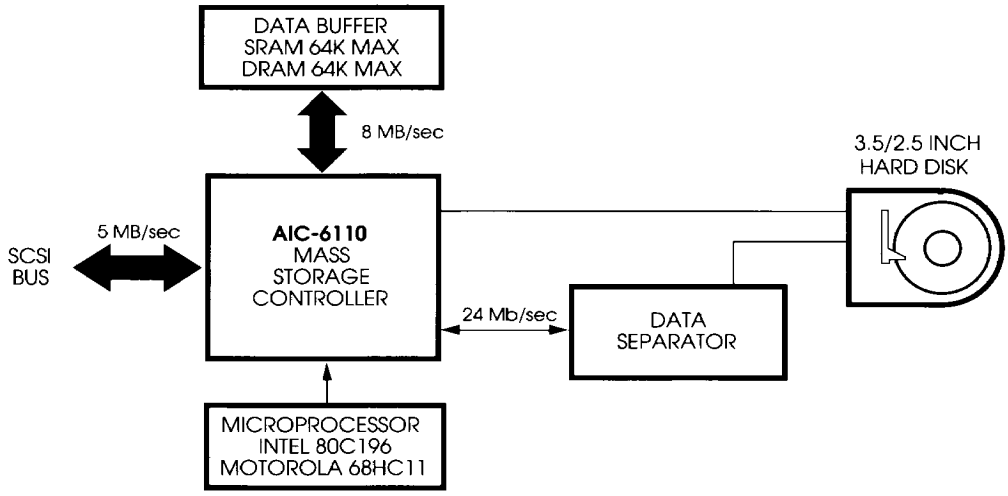
# AIC-6110

## Single-Chip SCSI Mass Storage Controller




**AIC-6110 Typical Application**

### FEATURES

#### SCSI Interface

- Synchronous transfers up to 5 MBytes/sec with an 8-byte offset
- Asynchronous transfer up to 5 MBytes/sec
- Multiple initiator and target modes
- Automatic arbitration, selection and reselection
- On-board 48 mA drivers

#### Peripheral Interface

- Transfer rate up to 24 Mbits/sec
- Controls embedded disk, hard disk, floppy, and tape drives
- Built-in 2,7 RLL ENDEC with programmable precompensation and 2 VFO sync patterns
- Optional NRZ interface
- 31-word RAM-based sequencer map allows track and format flexibility

#### Buffer Interface

- Supports DRAMs and SRAMs
- 8 MBytes/sec bandwidth at 32 MHz buffer clock
- Auto DRAM refresh
- 16-bit addressing capability
- Buffer bandwidth independent of disk rate
- 8-byte FIFO for speed matching

#### Microprocessor Interface

- High-speed multiplexed processor interface
- 16 fully maskable interrupts
- Open drain interrupt line

#### Technologies

- Power-down option
- High-speed CMOS
- Software compatible to Adaptec AIC-010/AIC-300
- 68-pin PLCC package or 80-pin QFP package

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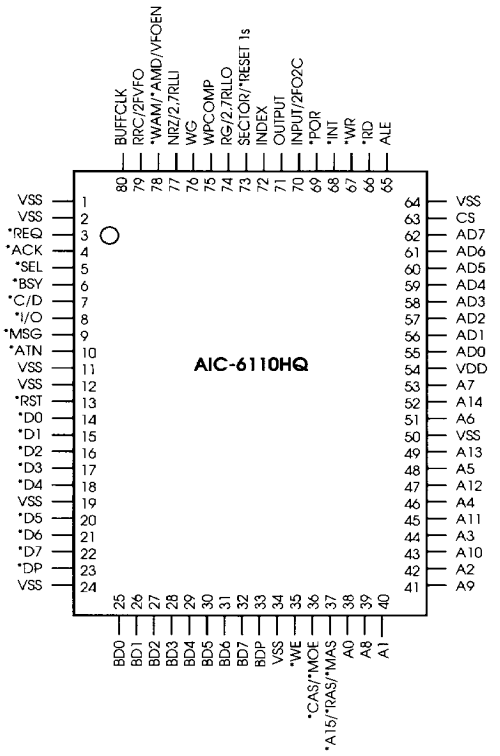


**AIC-6110 80-Pin QFP Package**

## Overview

AIC-6110 is a software-configurable VLSI device which provides the buffer management, SCSI bus control, encode/decode, and disk control functions for an intelligent disk, floppy, optical or tape drive controller. The AIC-6110 chip simplifies the design and increases the throughput of block-oriented high-performance peripheral controllers. Adaptec's AIC-6110 is intended for use in intelligent controllers utilizing a low-cost microprocessor for supervision.

The AIC-6110 is an advanced VLSI device fabricated in CMOS technology that allows for operations with data rates up to 24 Mbits/second NRZ or 18 Mbits/second in the 2,7 RLL mode. The AIC-6110's CMOS technology and the power-down feature lower power consumption, helping to meet the power requirements of smaller form factor drives and portable systems.

Other features of the AIC-6110 include the support of DRAM for lower system cost, or SRAM for higher performance. The AIC-6110 supports DRAM with internal refresh counters and does not require additional logic to support refresh. AIC-6110 also supports programmable precompensation allowing for a greater choice of media capability. The integrated 48 mA drivers in the AIC-6110 connect the chip directly to the SCSI bus. The AIC-6110 incorporates an 8-byte FIFO buffer that maximizes synchronous and asynchronous SCSI performance.

The AIC-6110 is software compatible with products that use the popular Adaptec architecture. The fully programmable RAM-based sequencer controls the various disk operations for formatting, reading and writing. The disk controller section also provides for a 32-bit or 48-bit programmable ECC polynomial for error detection and correction and also a fixed 16-bit CRC-CCITT polynomial for error detection purposes.

In order to effectively support SCSI bus transfer rates of up to 5 MBytes/second in the synchronous mode and multiple initiator, multiple target applications, the AIC-6110 incorporates a high-performance SCSI protocol chip, the AIC-6250. In addition, the AIC-6110 contains a high-performance buffer controller with a 7.5 MByte/second buffer bandwidth.