AKM

=PRELIMINARY= AK2396

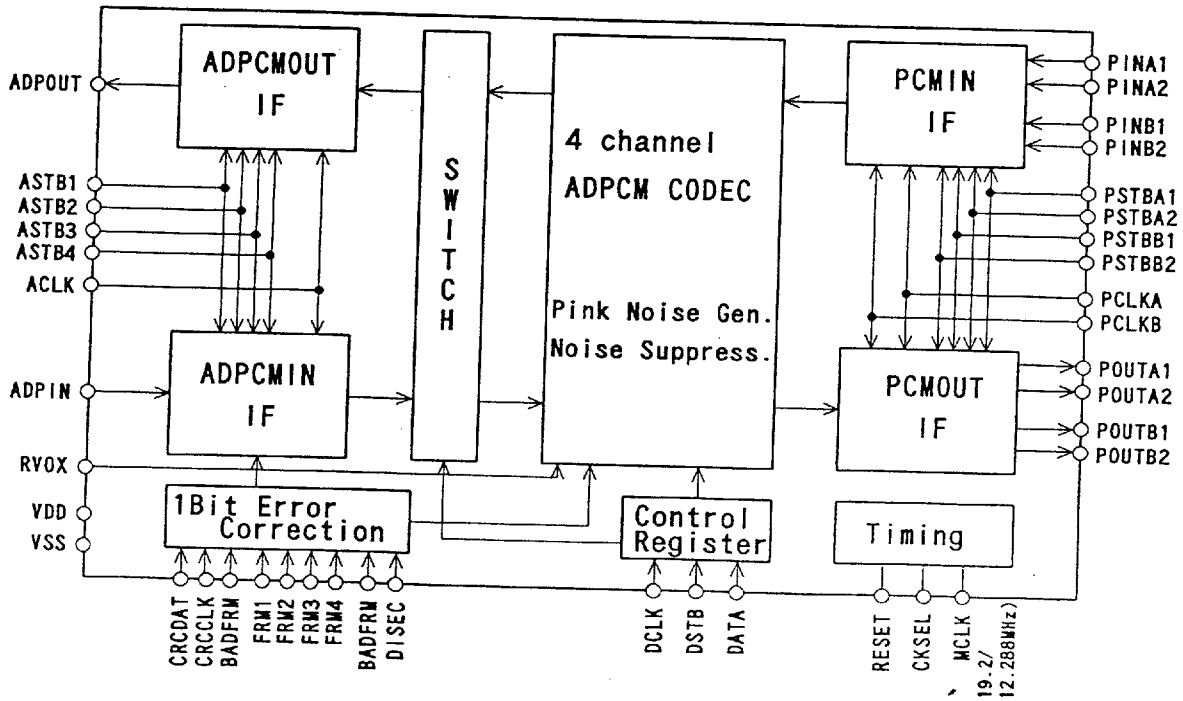
4 Channel ADPCM CODEC for Digital Cordless Telephone

Features

- ☐ ADPCM (Full Duplex, Synchronous operation) which conforms to ITU-T recommendation G.721, published in 1988.
- ☐ 1-bit error recovery circuit*/noise suppression*
- ☐ Noise generator function (each channel)
- ☐ ADPCM data through function (each channel)
- ☐ Mute function (each channel)
- ☐ Channel exchange function
- ☐ System Clock: 19.2MHz / 12.288MHz
- ☐ Operating voltage: 3-5 V single power supply
- ☐ Current consumption: 6 mA typ. (3V power supply)
- ☐ 44 pin QFP

* Patent pending (Japan)

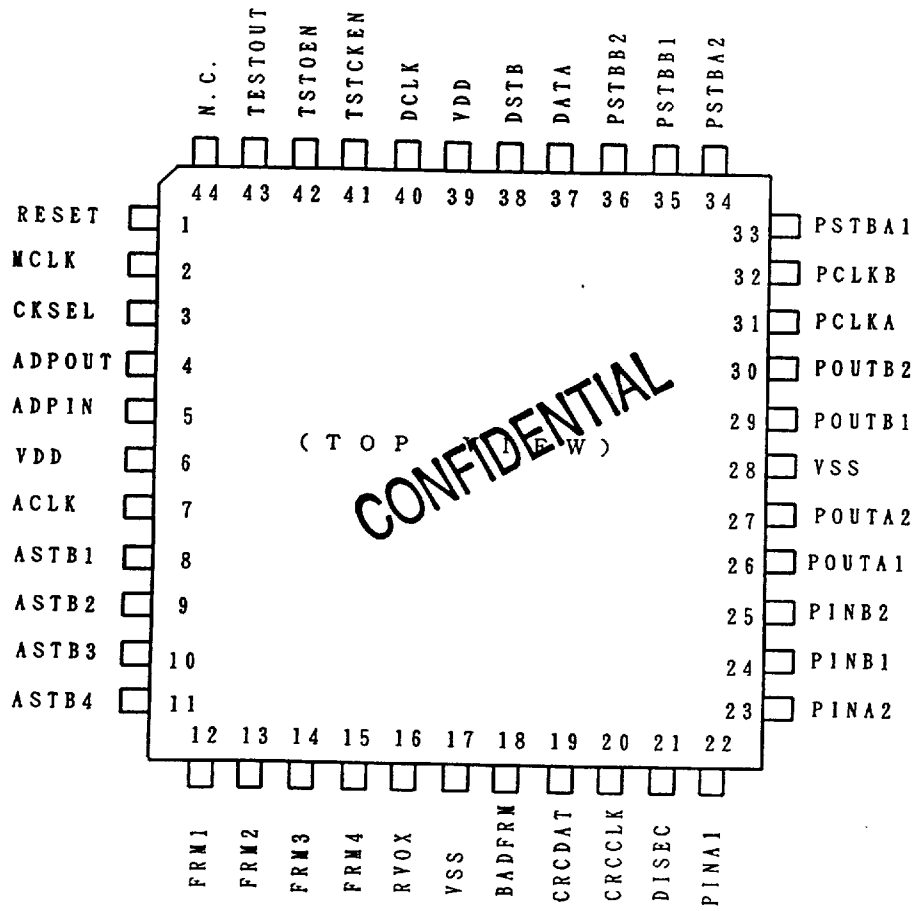
Block Diagram



Description

The AK2396 is a 4 channel, full-duplex ADPCM codec LSI developed for cell station of digital cordless telephones. This device includes our unique noise suppression function, and is capable of suppressing noise caused by transmission errors in the wireless line.

■ Pin arrangement



Pin Functions

No.	Name	I/O	Function	Remark
			Power Supply Pins	
6, 39	VDD	PWR	Voltage power supply input pins. (3 - 5V typ)	
17, 28	VSS	PWR	Ground pins.	
			System Clock / Reset Pins	
1	RESET	I	Reset input pin. It initializes the control register and timing. "1" : Reset "0" : Normal operation	Note-1
2	MCLK	I	19.2 MHz or 12.288 MHz master clock input pin.	
3	CKSEL	I	MCLK select pin. "1" : 19.2 MHz "0" : 12.288 MHz	
			ADPCM I/O pins	
4	ADPOUT	O (3 st)	ADPCM signal output pin. This signal is output from the MSB synchronous with the rising edge of ACLK and timing of ASTB of each channel. The data of 4 channels are time division multiplied.	
5	ADPIN	I	Time division multiplied ADPCM signal input pin. Signals are input from the MSB synchronous with the falling edge of ACLK and the timing of ASTB of each channel.	
7	ACLK	I	Shift clock input pin for ADPCM signal. 128KHz~2.048MHz.	
8, 9 10, 11	ASTB1-4	I	8 kHz synchronization signal input pin for the ADPCM signal.	
12, 13 14, 15	FRM1-4	I	Signal which shows the heading of the TDMA frame (5 ms) for the receiving ADPCM signal. Suppression of transmitting error noise and silent interval processing are executed in frame unites. "1" : Head of frame "0" : Rest of frame	
16	RVOX	I	Signal which shows the silent interval of receiving ADPCM signals. Depending on the control register setting, muting is carried out or pink noise is generated. "1" : Silence detected (VOX operation) "0" : Voice detected (Normal operation)	

No.	Name	I/O	Function	Remark
ADPCM I/O (continued)				
18	BADFRM	I	Signal show the error information of receiving frame. Normally, CRC error information is input. If the noise suppression function is not used, set it on "0". "1" : Frame error exist "0" : Frame error doesn't exist	
19	CRCDAT	I	CRC check result data input pin for correcting 1-bit errors. 16-bit data are input synchronous with the rising edge of the CRCCLK signal and latched with the rising edge of the next ASTB.	
20	CRCCLK	I	Shift clock input pin for CRCDAT input.	
21	DISEC	I	1-bit error correction function selection pin. "1" : 1-bit error correction function disable. "0" : 1-bit error correction function enable.	
PCM I/O pins				
22, 23	PINA1-2	I	64kbps PCM data input pins of A group. This signal is the reference of 4 channel synchronous operation. The timing of data input is given by PSTBAn pins and the data are input from the MSB synchronous with the falling edge of PCLKA.	
24, 25	PINB1-2	I	64kbps PCM data input pins of B group. The timing of data input is given by PSTBBn pins and the data are input from the MSB synchronous with the falling edge of PCLKB.	
26, 27	POUTA1-2	O (3st)	64kbps PCM data output pins of A group. The timing of data input is given by PSTBAn pins and the data are output from the MSB synchronous with the rising edge of PCLKA.	
29, 30	POUTB1-2	O (3st)	64kbps PCM data output pins of B group. The timing of data input is given by PSTBBn pins and the data are output from the MSB synchronous with the rising edge of PCLKB.	
31	PCLKA	I	Shift clock input pin for A group PCM data. 64KHz ~ 2.048MHz.	
32	PCLKB	I	Shift clock input pin for B group PCM data. 64KHz ~ 2.048MHz	
33, 34	PSTBA1-2	I	PCM data strobe signal input pin of A group. On 4 channel synchronous operation, the order of processing is channel 1 of A group, channel 2 of A group, channel 1 of B group and channel 2 of B group.	
35, 36	PSTBB1-2	I	PCM data strobe signal input pin of B group.	

No.	Name	I/O	Function	Remark
			CPU Interface Pins	
37	DATA	I	Serial data input pin to the control register. Data include the address + data, and are 12 bits in length. They are input synchronous with the rising edge of DCLK and are latched with the rising edge of DSTB.	
38	DSTB	I	Control register data strobe input pin.	
40	DCLK	I	Control register data shift clock input pin.	
			Others	
41	TSTCKEN	I	Test input pin. During normal use, set to "0".	
42	TSTOEN	I	Test input pin. During normal use, set to "0".	
43	TESTO	O	Test output pin. During normal use, set to open.	
44	N.C.	NC	No connect pin.	

Note-1) Please do reset operation when power is on.

Absolute Maximum Ratings

Parameters	Signal	min	max	Units
Power Supply Voltage	VD	-0.3	7	V
Voltage Applied to Pins	V_{TD}	-0.3	VD + 0.3	V
Storage Temperature	T_{stg}	-55	125	℃

Note) Voltages are all given with the ground pin as reference. VSS = 0V
Caution: If this device is used under conditions which exceed these values, the device may be destroyed. Also, normal operation cannot be guaranteed.

Recommended Operating Conditions

Parameter	Signal	min	typ	max	Units
Operating Temperature Range	T_a	-30		85	℃
Power Supply Voltage	VD	2.7	3.0/5.0	5.5	V

Caution: Voltages are all given with the ground pin as reference. VSS = 0V

Electrical Characteristics

■ DC Characteristics

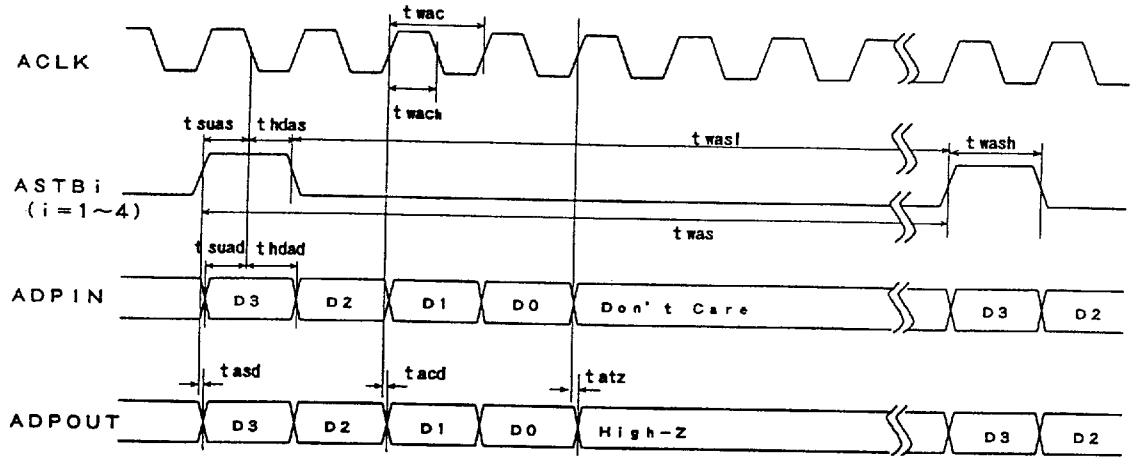
Parameter	Pin Name	Symbol	min	typ	max	Units	Remarks
Power Supply Current	VDD	I DD		6		mA	
High Level Input Voltage	I	V IH	0.7VDD			V	
Low Level Input Voltage	I	V IL			0.3VDD	V	
High Level Output Voltage	O	V OH	VDD-1.0			V	I_{OH}=-1.5mA
Low Level Output Voltage	O	V OL			0.5	V	I_{OL}= 1.5mA
High Level Input Leakage Current	I	I IH			10	μA	
Low Level Input Leakage Current	I	I IL	10			μA	

■ AC Characteristics

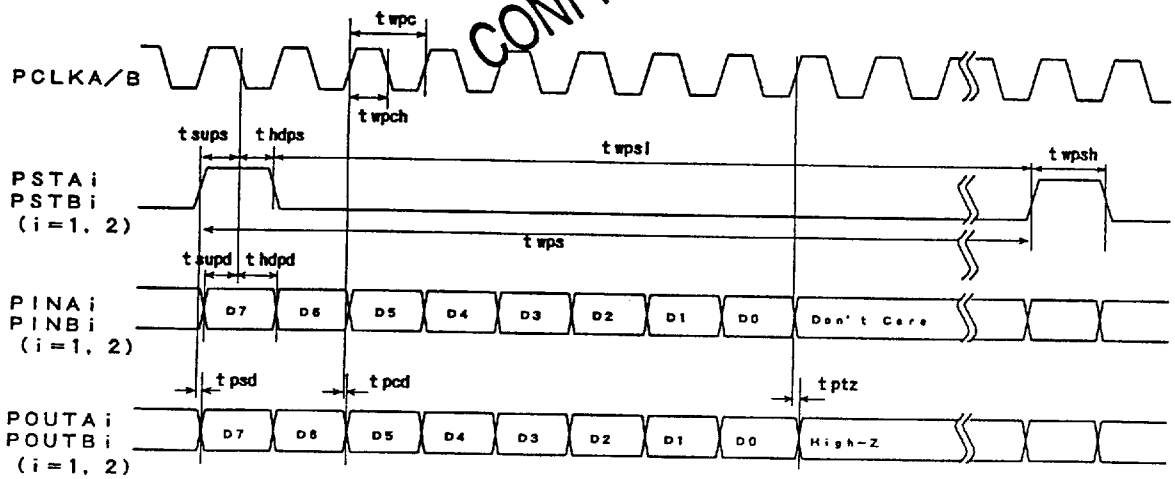
Parameters	Symbol	min	typ	max	Unit
Master clock frequency (Note 1)	f mck		19.2		MHz
〃 (Note 2)	f mck		12.288		MHz
Master clock duty		40	50	60	%
ADPCM Interface					
ACLK Cycle Time	t wac	1/256		1/16	t was
ACLK Pulse High Level Width	t wach		1/2		t wac
ASTB Cycle Time	t was		125		μs
ASTB Setup Time	t suas	100			ns
ASTB Hold Time	t hdas	100			ns
ASTB Pulse High Level Width	t wash	200			ns
ASTB Pulse Low Level Width	t wasl	1			t wac
ADPIN Setup Time	t suad	100			ns
ADPIN Hold Time	t hdad	100			ns
ADPOUT Delay Time (to ASTB) (Note 3)	t asd			55	ns
ADPOUT Delay Time (to ACLK) (Note 3)	t acd			55	ns
ACLK rising edge to High-Z Time	t atz			50	ns
PCM Interface					
PCLKA/B Cycle Time	t wpc	1/256		1/8	t ps
PCLKA/B Pulse High Level Width	t wpch		1/2		t wpc
PSTBA/B Cycle Time	tps		125		μs
PSTBA/B Setup Time	t supS	100			ns
PSTBA/B Hold Time	t hdps	100			ns
PSTBA/B Pulse High Level Width	t wpsh	200			ns
PSTBA/B Pulse Low Level Width	t wpsl	1			t wpc
PINA/B Setup Time	t supd	100			ns
PINA/B Hold Time	t hdpd	100			ns
POUTA/B Delay Time (to PSTB)(Note 3)	t psd			55	ns
POUTA/B Delay Time (to PCLK)(Note 3)	t pcd			55	ns
PCLKA/B Rising edge to High-Z time	t ptz			50	ns
CRCDAT, RVOX, BADFRM Interface					
CRCCLK Cycle Time	t wcc	1/1024twas		1/4 twac	
CRCCLK Pulse High Level width	t wcch		1/2		t wcc
CRCDAT Setup Time	t sucd	50			ns
CRCDAT Hold Time	t hdcd	50			ns
RVOX/BADFRM Setup Time	t surb	100			ns
RVOX/BADFRM Hold Time	t hdrb	100			ns
FRM Cycle Time	t wf		5		ns
FRM Setup Time (to CRCCLK)	t suf	50			ns
FRM Hold Time (to CRCCLK)	t hdf	50			ns
FRM Setup Time (to ACLK)	t sufa	100			ns
FRM Hold Time (to ACLK)	t hdfa	100			ns
FRM Pulse High Level Width	t wfh	200			ns
FRM Pulse Low Level Width	t wfl	1			t wac
CPU Interface					
DCLK Cycle Time	t wd	333			ns
DCLK Pulse High Level Width	t wdh		1/2		t wd
DATA Setup Time	t sud	100			ns
DATA Hold Time	t hdd	100			ns
DSTB Pulse High Level Width	t wds	1			t wd
DSTB Delay Time	t ds	333			ns
DSTB Pulse Low Level Setup Time	t sudl	100			ns
Reset Pulse Width	t wrsh	500			ns

(Note 1) When CKSEL=1.
(Note 2) When CKSEL=0.
(Note 3) When capacitance lord = 50pF.

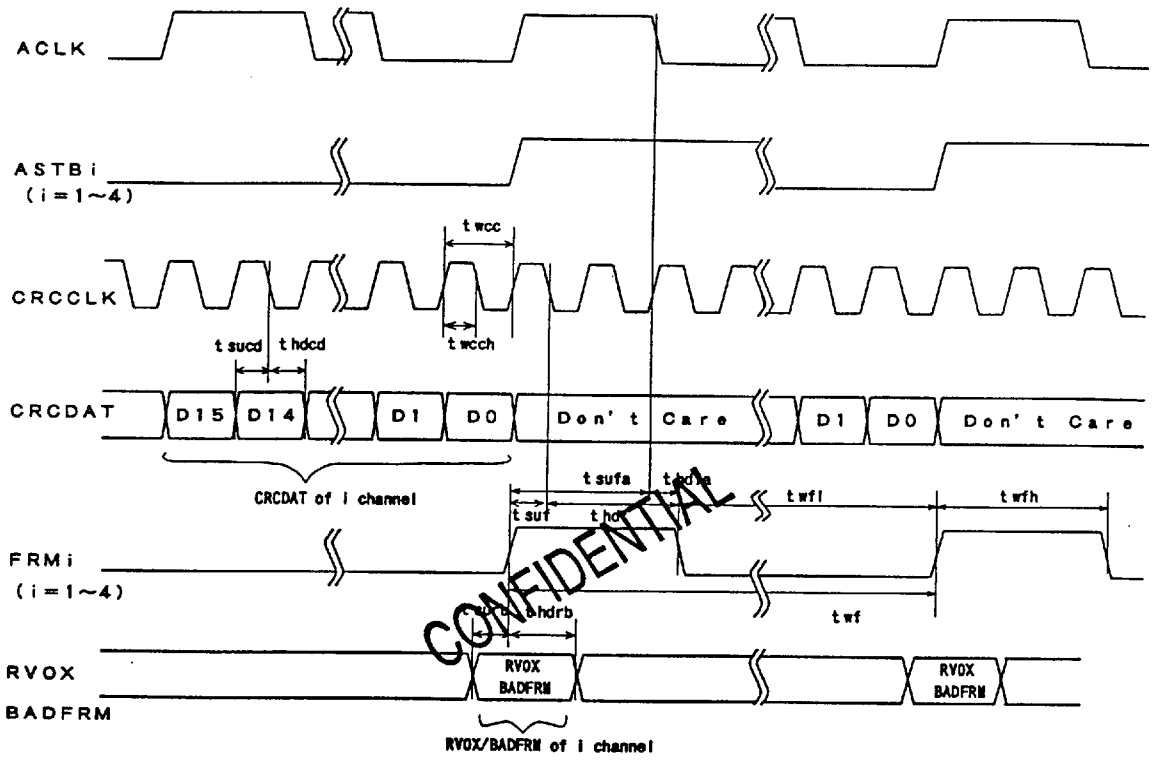
■ ADPCM Interface Timing Diagrams



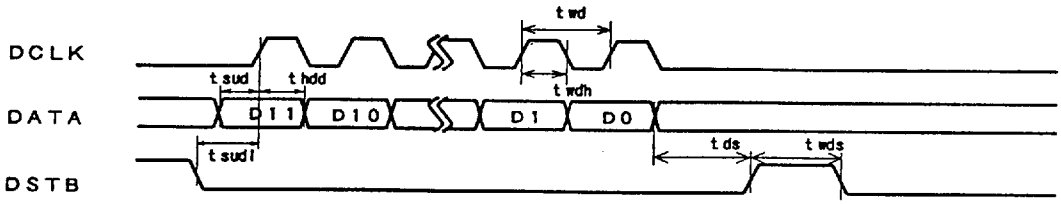
■ PCM Interface Timing Diagrams



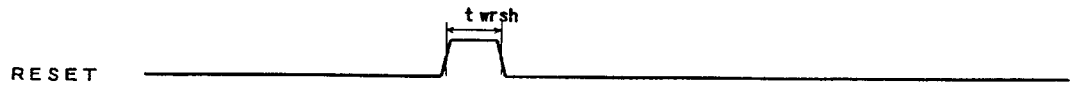
■ CRCDAT, RVOX, BADFRM Interface Timing Diagrams



■ CPU Interface Timing Diagrams



■ Reset Pulse



Explanation of Operation

■ Register Map

ADDRESS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	W	TXMUTE B2	TXMUTE B1	TXMUTE A2	TXMUTE A1	RXMUTE B2	RXMUTE B1	RXMUTE A2	RXMUTE A1
1	W	×	×	×	MT/NS	NOISE LEVEL			
2	W	THRU4 B2	THRU3 B1	THRU2 A2	THRU1 A1	NOUT4 B2	NOUT3 B1	NOUT2 A2	NOUT1 A1
3	W	CCB2		CCB1		CCA2		CCA1	
4	W	ATT VAL 1				STATE WIDTH 1			
5	W	2				2			
6	W	3				3			
7	W	4				4			
8	W	5				5			
9	W	6				6			
A	W	×	LIMIT VAL 2			×	LIMIT VAL 1		
B	W	×	LIMIT VAL 4			×	LIMIT VAL 3		
C	W	×	LIMIT VAL 6			×	LIMIT VAL 5		

×: Don't care

■ Control Data Format

ADDRESS				DATA							
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1)Mute Control [R0]

This register controls mute mode of each channel. After reset is done, normal operation is selected.

1: Mute
0: Normal operation

1. RXMUTE(D3～D0)

When mute is selected, +0 PCM code is output to POUTAn/Bn.

2. TXMUTE(D7～D4)

When mute is selected, PCM data of PINAn/Bn is replaced with +0 PCM code and input to ADPCM encoder.

(2)Noise Generation Parameters [R1]

This register controls the noise generation parameter for generating colored noise for silent intervals during uplink VOX control and executing noise generation during long term error frame reception. After reset is done, noise level is set to -24dBm0 and noise/mute select is selected to mute.

1. Noise Level(D3～D0)

Noise Level = -24- set value(NOISE LEVEL)*3 (dbm0)

Note) 3dB step width is approximate value.

2. Noise/Mute Select(D4)

Sets whether or not colored noise is generated or mute when silent interval signal to RVOX pin is received.

1:Noise Output
0:Mute

(3)PCM Output Control [R2]

This register controls the output data to POUTAn/Bn. The priorities of registers are RXMUTE of R0 register, data through of R2 register, Forced noise generate setting of R2 register. After reset is done, normal operation is selected.

1. Forced Noise Generation(D3~D0)

Sets whether or not colored noise will be output to POUTAn/Bn regardless of the RVOX pin input and the noise suppression state.

1: Noise output
0: Normal processing

2. Data through(D7~D4)

The upper 4 bit of PINAn/Bn and POUTAn/Bn are exchanged for the 4 bit data of ADPOUT and ADPIN as ADPCM data.
The lower 4 bit of PINAn/Bn and POUTAn/Bn are set "1".
In this mode, noise suppression is validated only ADPCM data limit and 1 bit error recovery.

1: data through
0: normal operation

(4)Channel exchange [R3]

This register controls the connection of each PCM channels to each ADPCM channels. Same ADPCM channel can not connect to the plural PCM channels.

1. PCM channel A1(D1~D0) After reset is done, A1 is connected with ADPCM 1ch.
2. PCM channel A2(D3~D2) After reset is done, A2 is connected with ADPCM 2ch.
3. PCM channel B1(D5~D4) After reset is done, B1 is connected with ADPCM 3ch.
4. PCM channel B2(D7~D6) After reset is done, B2 is connected with ADPCM 4ch.

Set Value(Dn+1、Dn)	ADPCM channel
0 0	1
0 1	2
1 0	3
0 0	4

(5)Noise Suppression Parameter [R4~RC]

These registers control the noise suppression parameters. When reset is done, parameters are set to our recommend value. If another values are needed, please set the new value after the reset.

1. Noise Suppression Parameter 1[R4~R9]

Set the state width (= number of frames) and the attenuation value at each state when the noise suppression is executed. The decoded ADPCM data is attenuated by setting value when the noise suppression is executed.

1.1 State Width(D3~D0)

State Width = set value (STATE WIDTH n) + 1

1.2 Attenuation Value(D7~D4)

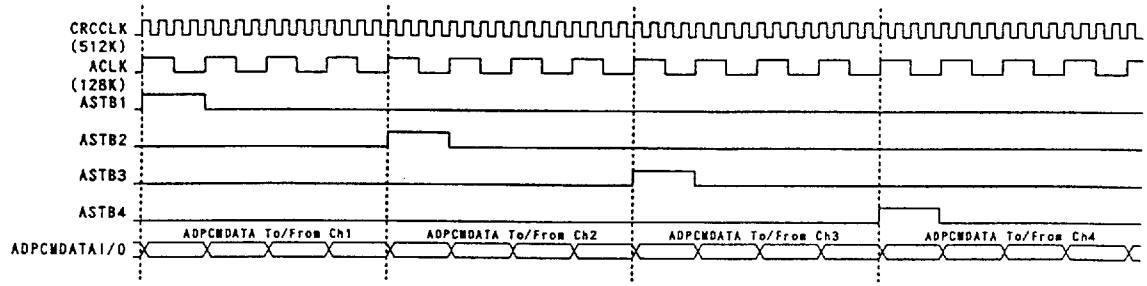
Attenuation Value = set value (ATT VAL n) * 3 (dB)

Note) 3dB step width is approximate value.

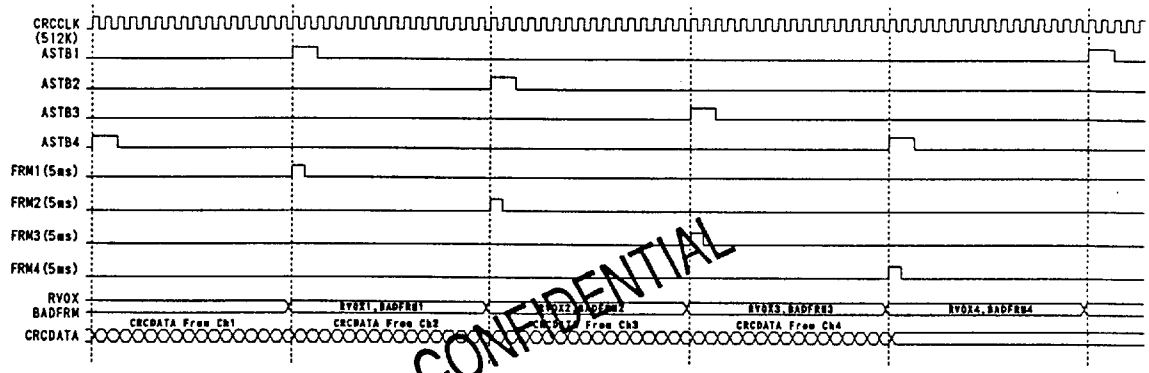
2. Noise Suppression Parameter 2[RA~RC]

Set the limit value of the ADPCM data at each state when the noise suppression executed. The set value is the absolute value. When the noise suppression is executed, if received ADPCM data is under the limit value then it is input to the ADPCM decoder, and if received ADPCM data is over the limit value then it is changed to positive or negative limit value and is input to the ADPCM decoder.

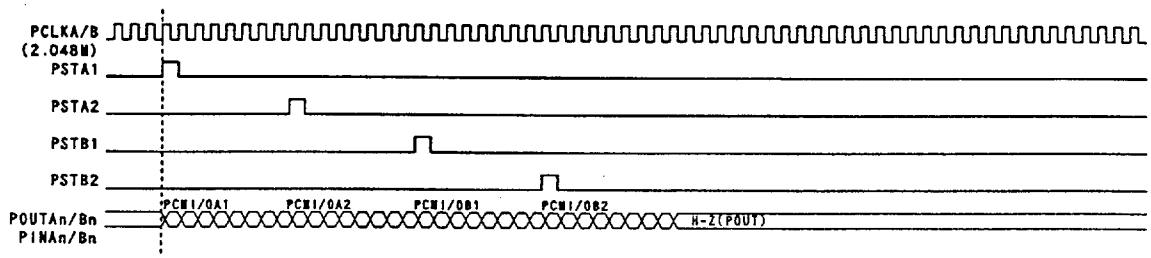
■ ADPCM I/O Timing Sample



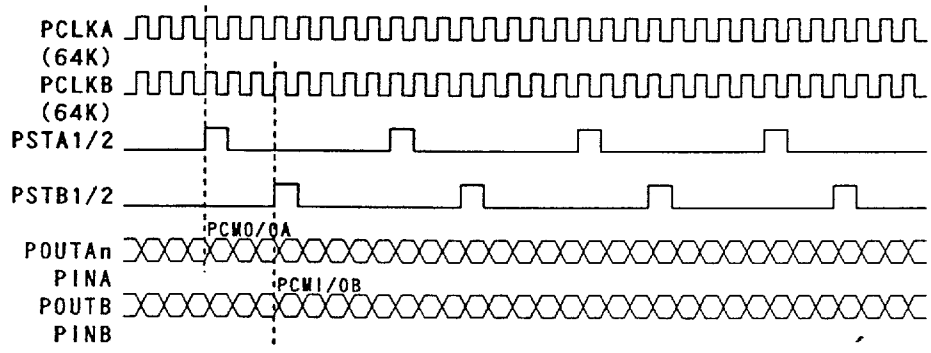
■ CRCDATA, BADFRM, RVOX Timing Sample



■ PCM I/O Timing Sample (1)



■ PCM I/O Timing Sample (2)



■ 1-bit Error Correction Circuit and Noise Suppression Function

The 32 k bps ADPCM defined by ITU-T Rec. G.721 has been a wired transmission system standard, and does not envision applications with high error rate wireless channels, so there are cases of voice quality deterioration occurring as a result of transmission errors by radio.

As the countermeasure, the AK2396 have a noise suppression function (Patent pending in Japan) for burst errors and 1 bit error correction (Patent pending in Japan) for random errors. These functions needs CRC error check results and CRC error check result data (16 bit) at receive side, so it is not required especial operation at transmit side.

(1) Noise suppression

The AK2396 reduce the voice quality deterioration that is caused by burst errors. Only transmission error information (CRC error check results etc.) is required. Overview of processing is shown below.

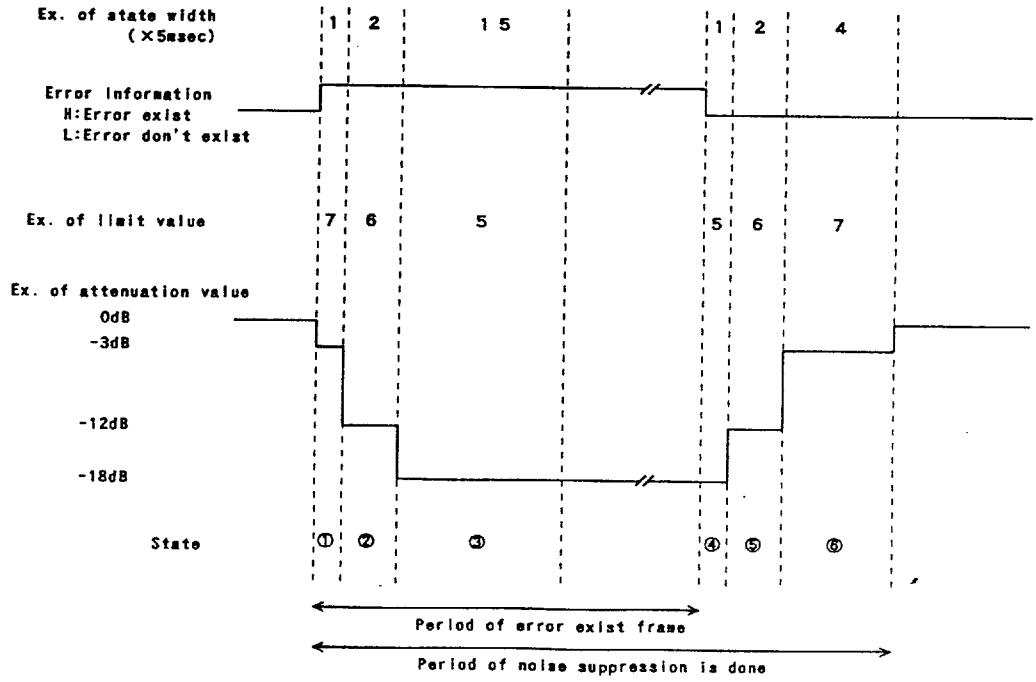
① Limitation of ADPCM code

If absolute value of received ADPCM code is under the limit value then it is input to the ADPCM decoder, and if absolute value of received ADPCM code is over the limit value then it is changed to positive or negative limit value and is input to the ADPCM decoder.

② Attenuation of linear PCM code

Attenuation is done to decoded linear PCM code.

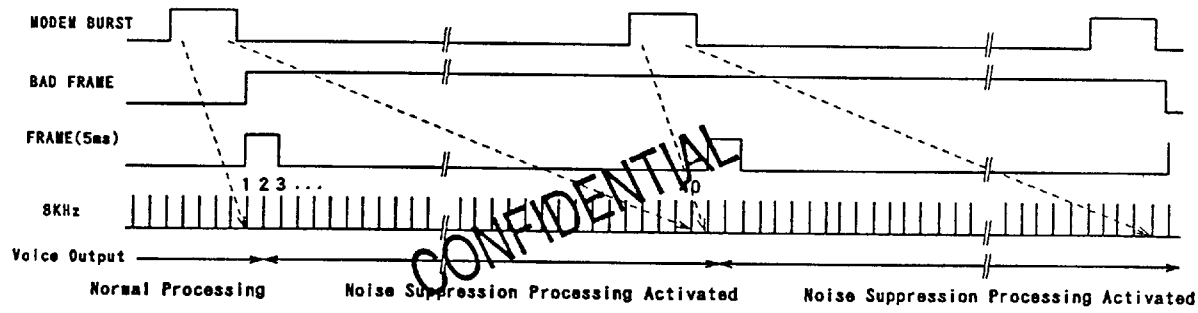
Limitation value and attenuation value can be set to control registers. These values are independent at each state (=times after error occurred), so, smooth attenuation and limitation can be executed. Also, state width can be set to control registers.



(2) 1 bit error correction

1 bit error correction reduce the noise that is caused by random errors in low BER condition. This function needs CRC check result data (16 bit) and CRC error check results. CRC check result data is input synchronous with CRCCLK and FRM. The AK2396 detect 1 bit error position by CRC check result data and reverse it. This function can be disabled by DISEC pin.

■ Timing of Noise Suppression Processing during Generation of Transmission Errors

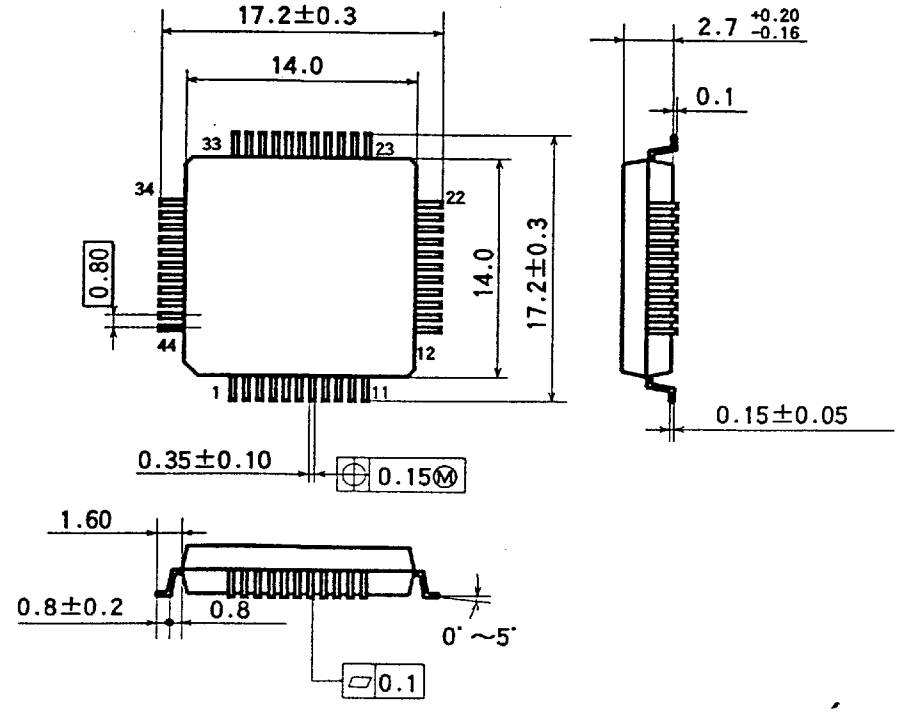


Package

■ Marking

(1) Pin 1 indicated (The chamfered corner indicates pin number 1.)
(2) Date Code: XXXXXXX (7 digits)
Higher order four digits: week code
Lower order three digits: In-house control code
(3) Marketing code: AK2396
(4) Manufacturing Country Name Indication : Japan
(5) Asahi Kasei Logo

■ Package External Dimensions



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