

Features

- 16 Mbit SRAM Multi Chip Module
- Allows 32-, 16- or 8-bit access configuration
- Operating Voltage: 3.3V \pm 0.3V, 5V Tolerant
- Access Time:
 - 25 ns, 20 ns
 - 18 ns (preliminary information)
- Very Low Power Consumption
 - Active: 595 mW per byte (Max) @ 20 ns⁽¹⁾, 415mW per byte (Max) @ 50ns⁽²⁾
 - Standby: 15 mW (Typ)
- Military Temperature Range: -55 to +125°C
- TTL-Compatible Inputs and Outputs
- Asynchronous
- Die manufactured on Atmel 0.25 μ m Radiation Hardened Process
- No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm²
- Tested up to a Total Dose of 300 krad (Si) according to MIL-STD-883 Method 1019
- ESD Better than 2000V
- Quality Grades:
 - QML-Q or V with SMD 5962-06229
 - ESCC
- 950 Mils Wide MQFP 68 Package
- Mass : 8.5 grams

Notes: 1. For AT68166FT-20 only. 540mW for AT68166FT-25.
2. For AT68166FT-20 only. 450mW for AT68166FT-25.

Description

The AT68166FT is a 16Mbit SRAM packaged in a hermetic Multi Chip Module (MCM) for space applications.

The AT68166FT MCM incorporates four 4Mbit AT60142FT SRAM dice. It can be organized as either one bank of 512Kx8, two banks of 512Kx16 or four banks of 512Kx8. It combines rad-hard capabilities, a latch-up threshold of 80MeV.cm²/mg, a Multiple Bit Upset immunity and a total dose tolerance of 300Krad, with a fast access time.

The MCM packaging technology allows a reduction of the PCB area by 50% with a weight savings of 75% compared to four 4Mbit packages.

Thanks to the small size of the 4Mbit SRAM die, Atmel has been able to accommodate the assembly of the four dice on one side of the package which facilitates the power dissipation.

The compatibility with other products allows designers to easily migrate to the Atmel AT68166FT memory.

The AT68166FT is powered at 3.3V and is 5V tolerant.

The AT68166FT is processed according to the test methods of the latest revision of the MIL-PRF-38535 or the ESCC 9000.



Rad Hard 16 MegaBit 3.3V 5V Tolerant SRAM Multi- Chip Module

AT68166FT

7531G-AERO-07/07



Block Diagram **Figure 1.** AT68166FT Block Diagram

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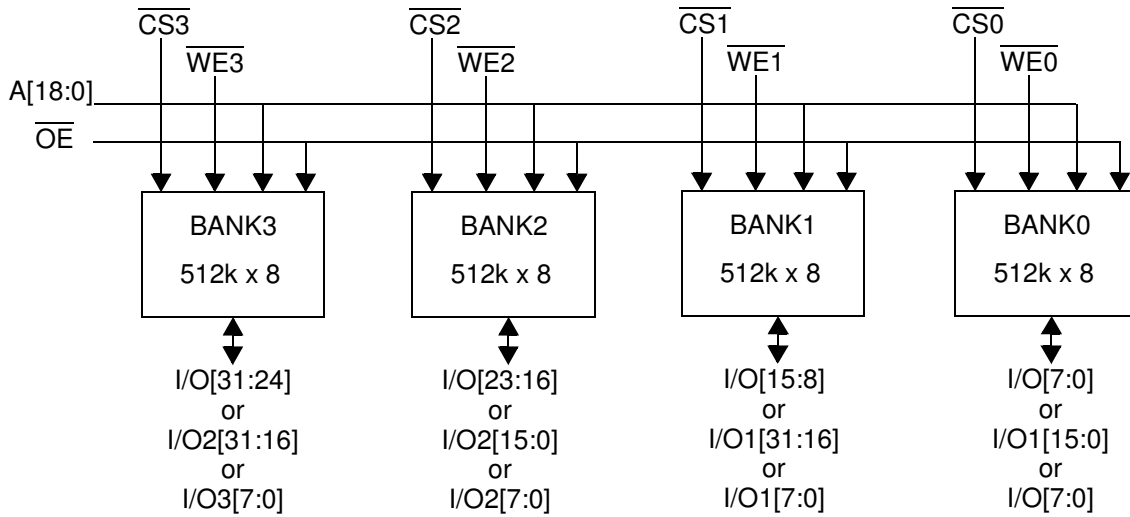
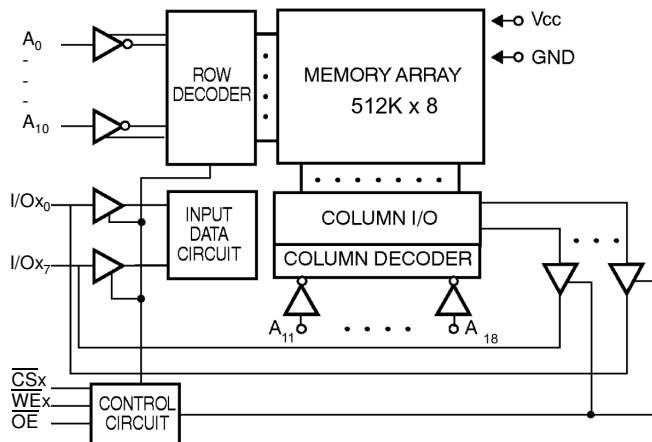


Figure 2. 512K x 8 Banks Block Diagram (AT60142FT)



Packages

AT68166FT is packed in MQFP68.

| | Access Times | | |
|-----------|--------------|-------|-------|
| | 25 ns | 20 ns | 18 ns |
| AT68166FT | YM | YS | YS |

The pin assignment depends on the access time. There are 2 versions:

- YM package where 3 pins are not connected.
- YS package where the 3 above pins are connected to GND or V_{CC}.

Pin Configuration

Table 1. AT68166FT pin assignment in YS package

| Lead | Signal | Lead | Signal | Lead | Signal | Lead | Signal |
|------|---------|------|--------|------|---------|------|--------|
| 1 | I/O0[0] | 18 | VCC | 35 | I/O3[7] | 52 | VCC |
| 2 | I/O0[1] | 19 | A11 | 36 | I/O3[6] | 53 | A10 |
| 3 | I/O0[2] | 20 | A12 | 37 | I/O3[5] | 54 | A9 |
| 4 | I/O0[3] | 21 | A13 | 38 | I/O3[4] | 55 | A8 |
| 5 | I/O0[4] | 22 | A14 | 39 | I/O3[3] | 56 | A7 |
| 6 | I/O0[5] | 23 | A15 | 40 | I/O3[2] | 57 | A6 |
| 7 | I/O0[6] | 24 | A16 | 41 | I/O3[1] | 58 | WE0 |
| 8 | I/O0[7] | 25 | CS0 | 42 | I/O3[0] | 59 | CS3 |
| 9 | GND | 26 | OE | 43 | GND | 60 | GND |
| 10 | I/O1[0] | 27 | CS1 | 44 | I/O2[7] | 61 | CS2 |
| 11 | I/O1[1] | 28 | A17 | 45 | I/O2[6] | 62 | A5 |
| 12 | I/O1[2] | 29 | WE1 | 46 | I/O2[5] | 63 | A4 |
| 13 | I/O1[3] | 30 | WE2 | 47 | I/O2[4] | 64 | A3 |
| 14 | I/O1[4] | 31 | WE3 | 48 | I/O2[3] | 65 | A2 |
| 15 | I/O1[5] | 32 | A18 | 49 | I/O2[2] | 66 | A1 |
| 16 | I/O1[6] | 33 | GND | 50 | I/O2[1] | 67 | A0 |
| 17 | I/O1[7] | 34 | VCC | 51 | I/O2[0] | 68 | VCC |

Note: In YM package leads 33, 34 and 68 are not connected.

Figure 3. AT68166FT pin assignment in YM package

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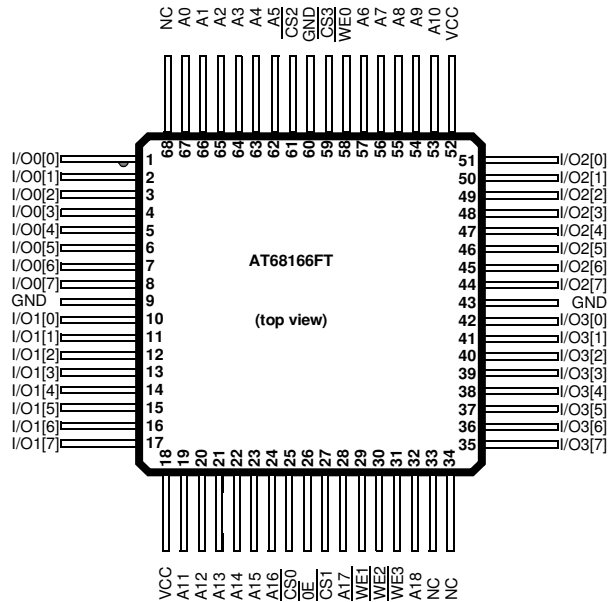
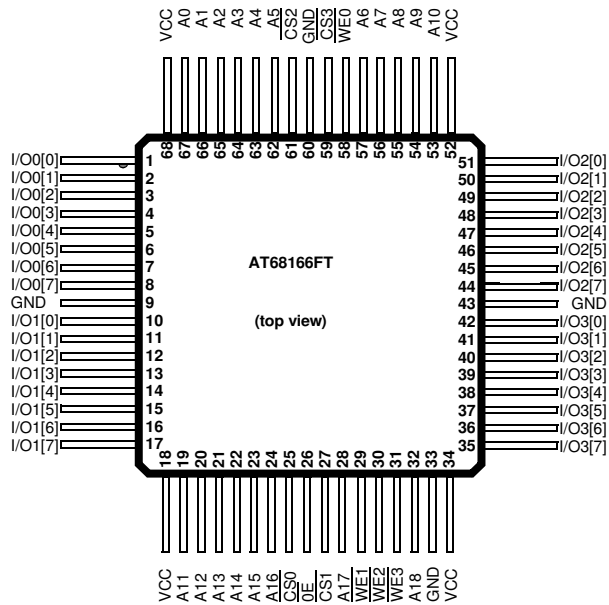


Figure 4. AT68166FT pin assignment in YS package



Pin Description

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Table 2. Pin Names

| Name | Description |
|-------------------------------------|-------------------|
| A0 - A18 | Address Inputs |
| I/O0 - I/O31 | Data Input/Output |
| $\overline{CS0}$ - $\overline{CS3}$ | Chip Select |
| $\overline{WE0}$ - $\overline{WE3}$ | Write Enable |
| \overline{OE} | Output Enable |
| VCC | Power Supply |
| GND ⁽¹⁾ | Ground |

Note: 1. The package lid is connected to GND

Table 3. Truth Table⁽¹⁾

| \overline{CSx} | \overline{WEx} | \overline{OE} | Inputs/Outputs | Mode |
|------------------|------------------|-----------------|----------------|----------------|
| H | X | X | Z | Standby |
| L | H | L | Data Out | Read |
| L | L | X | Data In | Write |
| L | H | H | Z | Output Disable |

Note: 1. L=low, H=high, X= H or L, Z=high impedance.



Electrical Characteristics

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Absolute Maximum Ratings*

| | |
|--|--------------------------------------|
| Supply Voltage to GND Potential:..... | -0.5V to +7V |
| DC Input Voltage:..... | GND -0.5V to 4.6V |
| DC Output Voltage High Z State:..... | GND -0.5V to 4.6V |
| Storage Temperature:..... | -65°C to +150°C |
| Output Current Into Outputs (Low): | 20 mA |
| Electro Statics Discharge Voltage:..... | > 2000V (MIL STD 883D Method 3015.3) |

*NOTE:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Military Operating Range

| Operating Voltage | Operating Temperature |
|-------------------|-----------------------|
| 3.3 ± 0.3V | -55°C to + 125°C |

Recommended DC Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|-----------------|--------------------|-----------|-----|---------------------|------|
| V _{CC} | Supply voltage | 3 | 3.3 | 3.6 | V |
| GND | Ground | 0.0 | 0.0 | 0.0 | V |
| V _{IL} | Input low voltage | GND - 0.3 | 0.0 | 0.8 | V |
| V _{IH} | Input high voltage | 2.2 | – | 5.5V ⁽¹⁾ | V |

Note: 1. 5.8V in transient conditions.

Capacitance

| Parameter | Description | Min | Typ | Max | Unit |
|--|-------------------|-----|-----|-----|------|
| C _{in} ⁽¹⁾ (OE and Ax) | Input capacitance | – | – | 48 | pF |
| C _{in} ⁽¹⁾ (CSx and WEx) | Input capacitance | – | – | 12 | pF |
| C _{io} ⁽¹⁾ | I/O capacitance | – | – | 12 | pF |

Note: 1. Guaranteed but not tested.

DC Parameters

| Parameter | Description | Minimum | Typical | Maximum | | | Unit |
|-----------------------------|----------------------------------|---------|---------|--------------|--------------|--------------|------|
| | | | | AT68166FT-25 | AT68166FT-20 | AT68166FT-18 | |
| IIX ⁽¹⁾ | Input leakage current | -1 | – | 1 | 1 | 1 | μA |
| IOZ ⁽¹⁾ | Output leakage current | -1 | – | 1 | 1 | 1 | μA |
| IIH ⁽²⁾ at 5.5V | Input Leakage Current (OE & Axx) | – | – | 10 | 6 | 6 | μA |
| | Input Leakage Current (WE & CS) | – | – | 5 | 2 | 2 | μA |
| IOZH ⁽²⁾ at 5.5V | Output Leakage Current | – | – | 5 | 1.5 | 1.5 | μA |
| VOL ⁽³⁾ | Output low voltage | – | – | 0.4 | 0.4 | 0.4 | V |
| VOH ⁽⁴⁾ | Output high voltage | 2.4 | – | – | – | – | V |

- Notes:
1. $GND < V_{IN} < V_{CC}$, $GND < V_{OUT} < V_{CC}$ Output Disabled.
 2. $V_{IN} = 5.5V$, $V_{OUT} = 5.5V$, Output Disabled.
 3. V_{CC} min. - $I_{OL} = 6$ mA
 4. V_{CC} min. $I_{OH} = -4$ mA

Consumption

| Symbol | Description | TAVAV/TAVAW Test Condition | AT68166FT-25 | AT68166FT-20 | AT68166FT-18 (preliminary) | Unit | Value |
|------------------------------------|---------------------------|----------------------------|--------------|--------------|----------------------------|------|-------|
| $I_{CCSB}^{(1)}$ | Standby Supply Current | – | 10 | 7 | 7.5 | mA | max |
| $I_{CCSB1}^{(2)}$ | Standby Supply Current | – | 8 | 6 | 7 | mA | max |
| $I_{CCOP}^{(3)}$ Read per byte | Dynamic Operating Current | 18 ns | – | – | 170 | mA | max |
| | | 20 ns | – | 165 | 165 | | |
| | | 25 ns | 150 | 145 | 145 | | |
| | | 50 ns | 85 | 80 | 80 | | |
| | | 1 μ s | 15 | 12 | 12 | | |
| $I_{CCOP}^{(4)}$ Write per byte | Dynamic Operating Current | 18 ns | – | – | 145 | mA | max |
| | | 20 ns | – | 140 | 140 | | |
| | | 25 ns | 150 | 135 | 135 | | |
| | | 50 ns | 125 | 115 | 115 | | |
| | | 1 μ s | 110 | 105 | 105 | | |

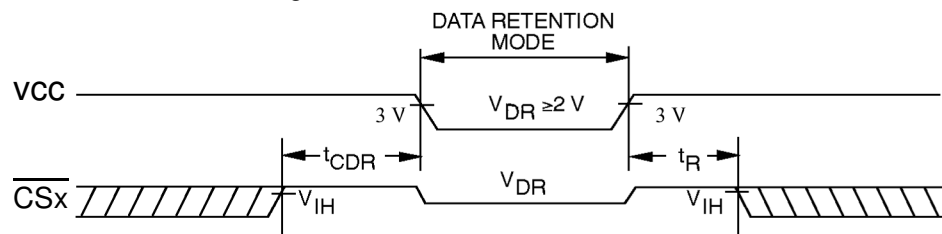
- Notes:
1. All $\overline{CSx} \geq V_{IH}$
 2. All $\overline{CSx} \geq V_{CC} - 0.3V$
 3. $F = 1/T_{TAVAV}$, $I_{out} = 0$ mA, $\overline{WEx} = \overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.
 4. $F = 1/T_{TAVAW}$, $I_{out} = 0$ mA, $\overline{WEx} = V_{IL}$, $\overline{OE} = V_{IH}$, $V_{IN} = GND/V_{CC}$, V_{CC} max.

Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select \overline{CSx} must be held high within V_{CC} to $V_{CC} - 0.2V$.
2. Output Enable (\overline{OE}) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions \overline{CSx} and \overline{OE} must be kept between $V_{CC} + 0.3V$ and 70% of V_{CC} .
4. The RAM can begin operation $> t_R$ ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 5. Data Retention Timing



Data Retention Characteristics

| Parameter | Description | Min | Typ $T_A = 25^\circ\text{C}$ | Max | Unit |
|-------------------------|--------------------------------------|-------------------------|------------------------------|--------------------|------|
| V_{CCDR} | V_{CC} for data retention | 2.0 | – | – | V |
| t_{CDR} | Chip deselect to data retention time | 0.0 | – | – | ns |
| t_{R} | Operation recovery time | $t_{\text{AVAV}}^{(1)}$ | – | – | ns |
| $I_{\text{CCDR}}^{(2)}$ | Data retention current | – | 3 | 6 (AT68166FT-25) | mA |
| | | | | 4.5 (AT68166FT-20) | |
| | | | | 5 (AT68166FT-18) | |

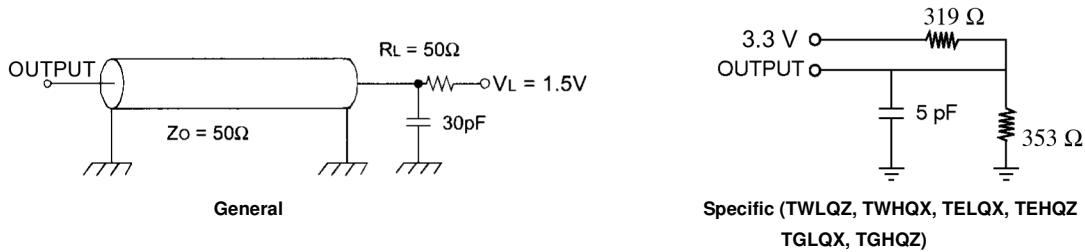
- T_{AVAV} = Read cycle time.
- All $\text{CS}_X = V_{\text{CC}}$, $V_{\text{IN}} = \text{GND}/V_{\text{CC}}$.

AC Characteristics

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Temperature Range:..... -55 +125°C
 Supply Voltage: 3.3 ±0.3V
 Input Pulse Levels: GND to 3.0V
 Input Rise and Fall Times:..... 3ns (10 - 90%)
 Input and Output Timing Reference Levels:..... 1.5V
 Output Loading I_{OL}/I_{OH} :..... See Figure 3

Figure 6. AC Test Loads Waveforms



Write Cycle

Table 4. Write cycle timings⁽¹⁾

| Symbol | Parameter | AT68166FT-25 | | AT68166FT-20 | | AT68166FT-18 (preliminary) | | Unit |
|--------|----------------------------------|--------------|-----|--------------|-----|-------------------------------|-----|------|
| | | min | max | min | max | min | max | |
| TAVAW | Write cycle time | 20 | - | 20 | - | 18 | - | ns |
| TAVWL | Address set-up time | 2 | - | 2 | - | 2 | - | ns |
| TAVWH | Address valid to end of write | 14 | - | 11 | - | 10 | - | ns |
| TDVWH | Data set-up time | 9 | - | 8 | - | 7 | - | ns |
| TELWH | \overline{CS} low to write end | 12 | - | 12 | - | 11 | - | ns |
| TWLQZ | Write low to high $Z^{(2)}$ | - | 10 | - | 10 | - | 9 | ns |
| TWLWH | Write pulse width | 12 | - | 9 | - | 9 | - | ns |
| TWHAX | Address hold from end of write | 0 | - | 0 | - | 0 | - | ns |
| TWHDX | Data hold time | 2 | - | 1 | - | 1 | - | ns |
| TWHQX | Write high to low $Z^{(2)}$ | 5 | - | 5 | - | 5 | - | ns |

- Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.
 2. Parameters guaranteed, not tested, with output loading 5 pF. (See "AC Test Loads Waveforms" on page 10.)

Figure 7. Write Cycle 1. \overline{WE} Controlled, \overline{OE} High During Write

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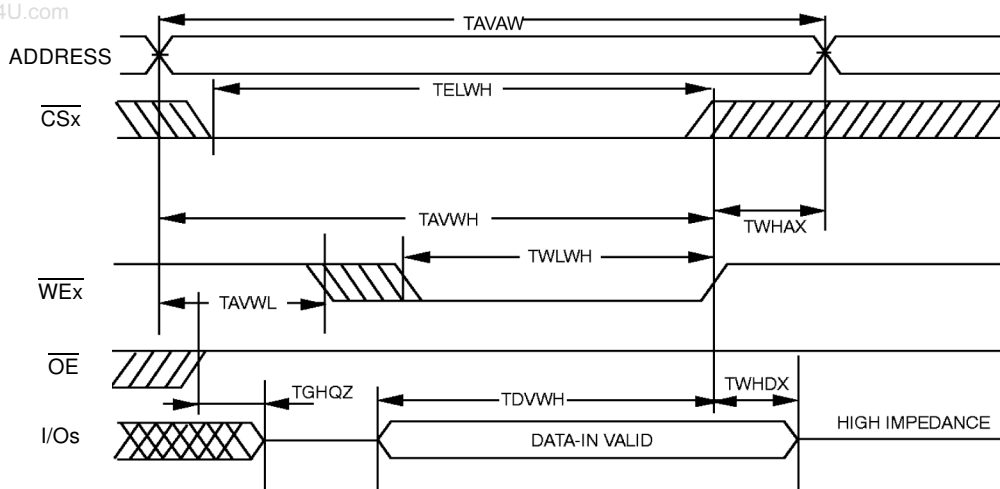


Figure 8. Write Cycle 2. \overline{WE} Controlled, \overline{OE} Low

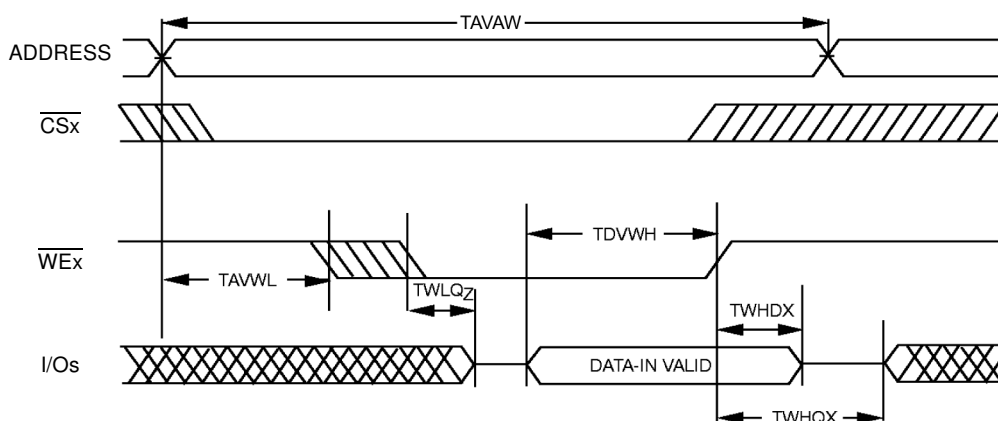
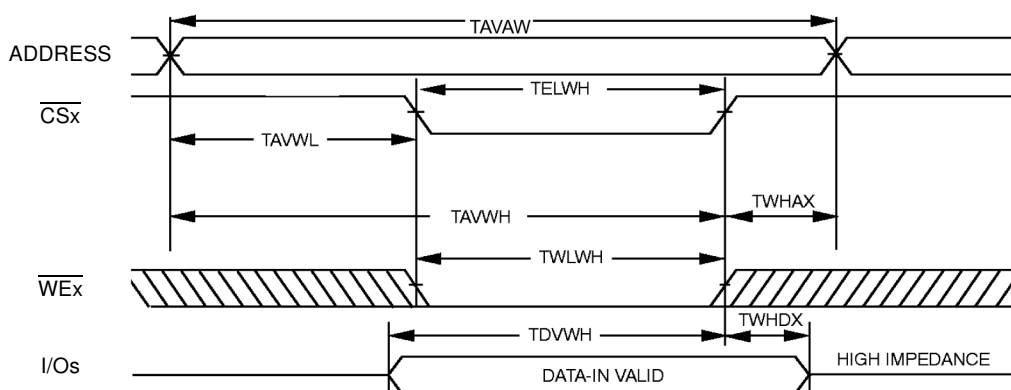


Figure 9. Write Cycle 3. \overline{CS} Controlled



The internal write time of the memory is defined by the overlap of \overline{CS} Low and \overline{WE} LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write. Data out is high impedance if $\overline{OE} = V_{IH}$.

Read Cycle

www.DataSheet4U.com **Table 5.** Read cycle timings⁽¹⁾

| Symbol | Parameter | AT68166FT-25 | | AT68166FT-20 | | AT68166FT-18 (preliminary) | | Unit |
|--------|--|--------------|-----|--------------|-----|-------------------------------|-----|------|
| | | min | max | min | max | min | max | |
| TAVAV | Read cycle time | 25 | - | 20 | - | 18 | - | ns |
| TAVQV | Address access time | - | 25 | - | 20 | - | 18 | ns |
| TAVQX | Address valid to low Z | 5 | - | 5 | - | 5 | - | ns |
| TELQV | Chip-select access time | - | 25 | - | 20 | - | 18 | ns |
| TELQX | $\overline{\text{CS}}$ low to low Z ⁽²⁾ | 5 | - | 5 | - | 5 | - | ns |
| TEHQZ | $\overline{\text{CS}}$ high to high Z ⁽²⁾ | - | 10 | - | 9 | - | 9 | ns |
| TGLQV | Output Enable access time | - | 12 | - | 10 | - | 9 | ns |
| TGLQX | $\overline{\text{OE}}$ low to low Z ⁽²⁾ | 2 | - | 2 | - | 2 | - | ns |
| TGHQZ | $\overline{\text{OE}}$ high to high Z ⁽²⁾ | - | 10 | - | 9 | - | 9 | ns |

- Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.
 2. Parameters guaranteed, not tested, with output loading 5 pF. (See "AC Test Loads Waveforms" on page 10.)

Figure 10. Read Cycle nb 1: Address Controlled ($\overline{CS} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$)

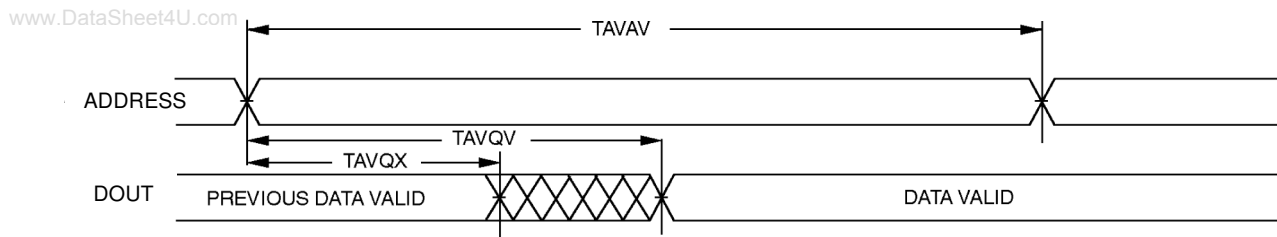
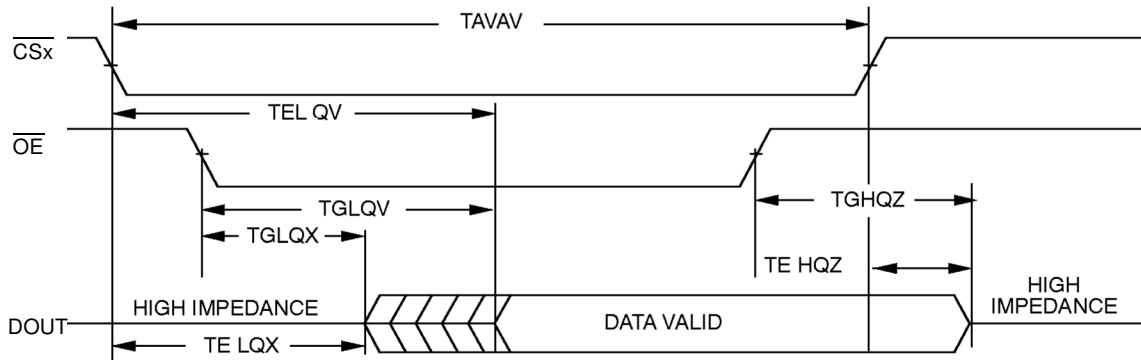


Figure 11. Read Cycle nb 2: Chip Select Controlled ($\overline{WE} = V_{IH}$)



Typical Applications

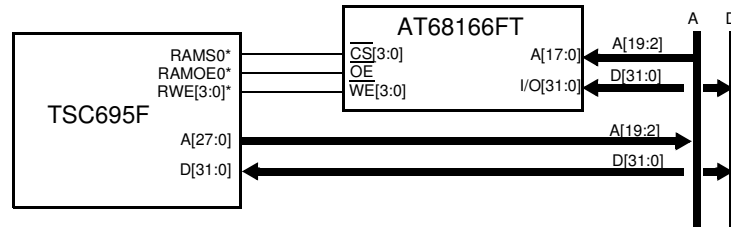
This section presents some standard implementations of the AT68166FT in application.

32-bit mode application

When used on a 32-bit (word) application, the module shall be connected as follow :

- The 32 lines of data are connected to distinct data lines
- The four \overline{CS}_x are connected together and linked to a single host \overline{CS} output
- Each one of the four \overline{WE}_x is connected to a dedicated \overline{WE} line on the host to allow byte, half word and word format write.

Figure 12. 32-bit typical application (1 SRAM bank)

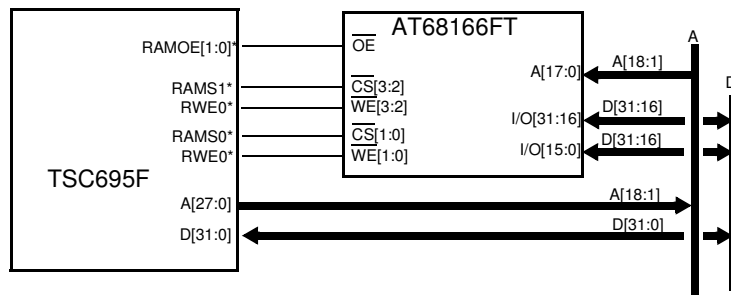


16-bit mode application

When used on a 16-bit (half word) application, the module can be connected as presented in the following figure. This allows use of a single AT68166FT part for two SRAM memory banks.

All input controls of the AT68166FT not used in the application shall be pulled-up.

Figure 13. 16-bit typical application (two SRAM banks)



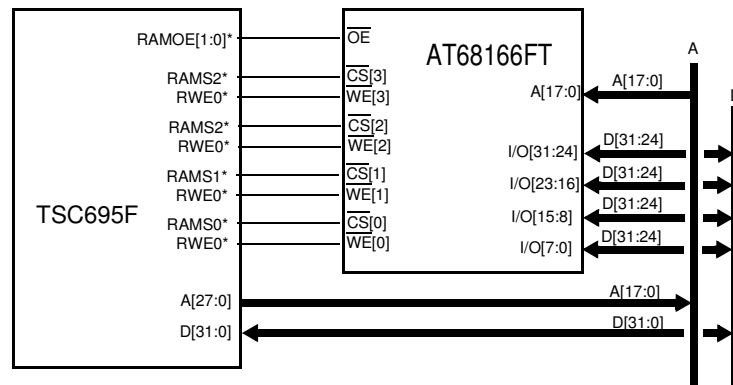
8-bit mode application

When used on a 8-bit (byte) application, the module can be connected as presented in the following figure. This allows use of a single AT68166FT part for up to four SRAM memory banks.

All input controls of the AT68166FT not used in the application shall be pulled-up.

Figure 14. 8-bit typical application (two SRAM banks)

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Ordering Information

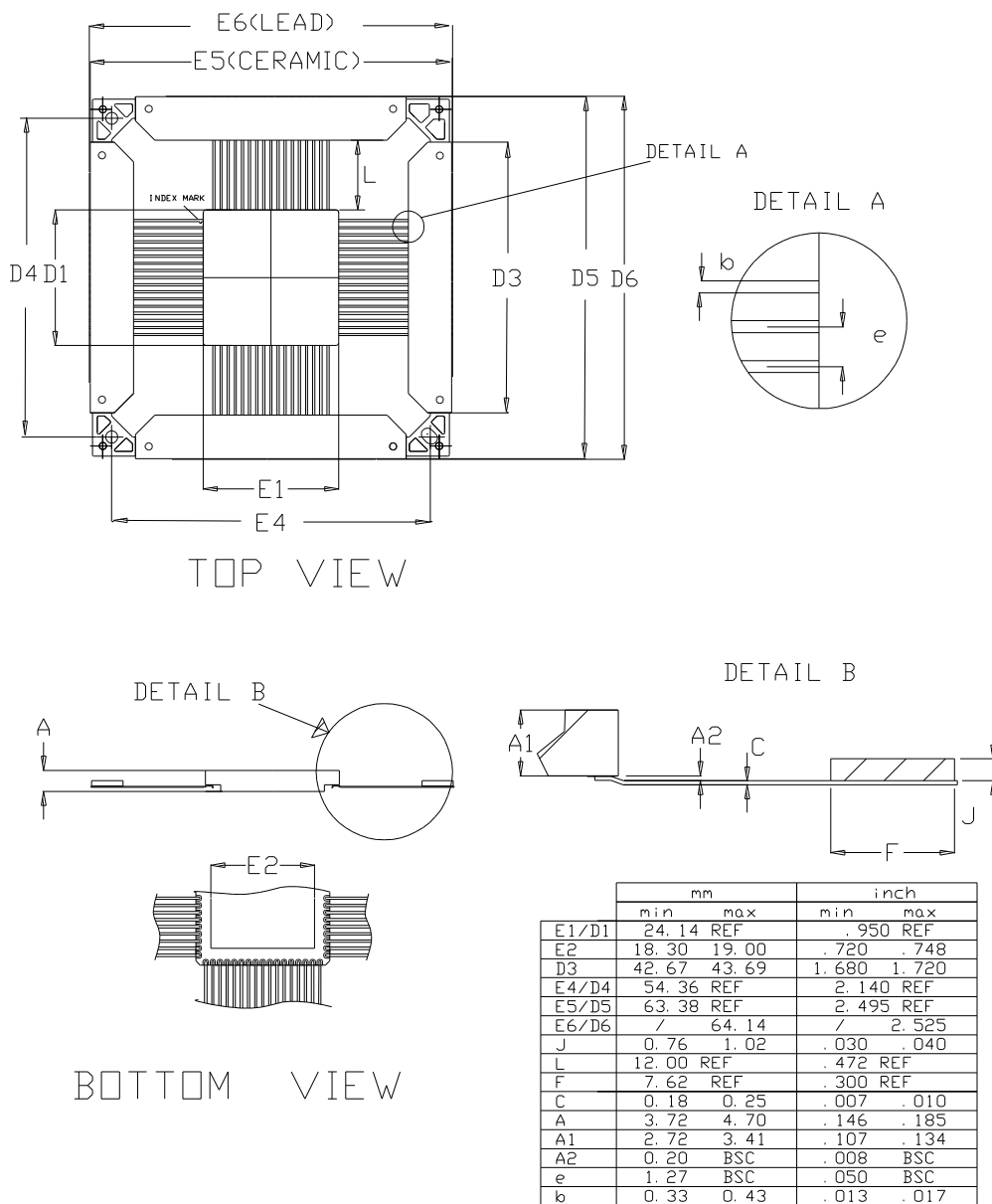
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| Part Number | Temperature Range | Speed | Package | Flow |
|--------------------------------------|-------------------|-------|---------|---------------------|
| AT68166FT | | | | |
| AT68166FT-YM25-E | 25°C | 25 ns | MQFPT68 | Engineering Samples |
| 5962-0622901QXC | -55° to +125°C | 25 ns | MQFPT68 | QML Q |
| 5962-0622901VXC | -55° to +125°C | 25 ns | MQFPT68 | QML V |
| 5962R0622901VXC | -55° to +125°C | 25 ns | MQFPT68 | QML V RHA |
| AT68166FT-YM25-SCC | -55° to +125°C | 25 ns | MQFPT68 | ESCC |
| AT68166FT-YS20-E | 25°C | 20 ns | MQFPT68 | Engineering Samples |
| AT68166FT-YS20-MQ ⁽²⁾ | -55° to +125°C | 20 ns | MQFPT68 | QML Q |
| AT68166FT-YS20-SV ⁽²⁾ | -55° to +125°C | 20 ns | MQFPT68 | QML V |
| AT68166FT-YS20-SR ⁽²⁾ | -55° to +125°C | 20 ns | MQFPT68 | QML V RHA |
| AT68166FT-YS20-SCC ⁽²⁾ | -55° to +125°C | 20 ns | MQFPT68 | ESCC |
| AT68166FT-YS18-E ⁽¹⁾ | 25°C | 18 ns | MQFPT68 | Engineering Samples |
| AT68166FT-YS18-MQ ⁽¹⁾⁽²⁾ | -55° to +125°C | 18 ns | MQFPT68 | QML Q |
| AT68166FT-YS18-SV ⁽¹⁾⁽²⁾ | -55° to +125°C | 18 ns | MQFPT68 | QML V |
| AT68166FT-YS18-SR ⁽¹⁾⁽²⁾ | -55° to +125°C | 18 ns | MQFPT68 | QML V RHA |
| AT68166FT-YS18-SCC ⁽¹⁾⁽²⁾ | -55° to +125°C | 18 ns | MQFPT68 | ESCC |

- Note:
1. Please contact your local sales office.
 2. Will be replaced by SMD part number when available.

Package Drawings

68-lead Quad Flat Pack (950 Mils) with non conductive tie bar



Note: Lid is connected to Ground.

Note: YM and YS package drawings are identical.

Document Revision History

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Changes from 7531C to 7531D

1. Update of access time parameters.

Changes from 7531D to 7531E

1. Added YS package.

Changes from 7531E to 7531F

1. Updated ordering information.

Changes from 7531F to 7531G

1. Split datasheet into two separate documents: removed AT68166F from this document. Please refer to document 7747 on the Atmel web site.



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