T-77-29

DSPG7002

Advance Information

December 1989, Rev. 1.1

THE DSP GROUP, INC.

Variable Speed & IC Repeat Speech Processor

(Long IC Repeat Applications)

GENERAL DESCRIPTION

The DSPG7002 Variable Speed & IC Repeat Speech Processor chip set performs the following functions:

- Time Scale Modification of speech signals for variable speed speech playback applications.
- High quality digital speech compression for IC repeat applications.
- Voice activated recording.

This chip set is ideal for dictation, transcription and other speech reproduction applications. The DSPG7002 utilizes the proprietary FLEXISPEECH digital signal processing Time Scale Modification (TSM) technology to increase (up to 200%) or decrease (down to 50%) the playback speed of speech signals. This processing does not affect the quality of the reproduced speech, nor its natural sound, intonation or the speaker identity. When used in conjunction with variable speed tape recorders, the chip set derives synchronization signals from the recorder mechanism.

The DSPG7002 incorporates a high quality speech compression technique, capable of digitally coding speech signals at rates of 13 kbps. This allows efficient storage of a speech segment for the 'IC repeat' function.

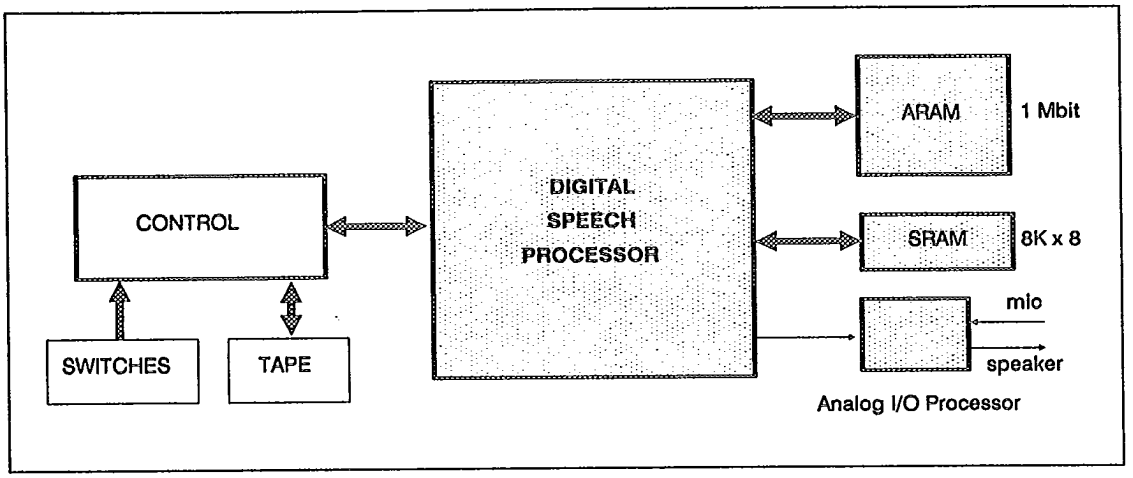
The DSPG7002 incorporates also a highly reliable 'speech specific' speech detector that supports voice activated recording for tape recorders.

The DSPG7002 is specially designed for long time IC Repeat applications. The chip set comprises of a digital speech processor, a CODEC, 1Mbit ARAM and a 8K*8 SRAM.

FEATURES

- High quality real-time speech restoration for variable-speed speech playback (0.5 to 2.0)
- High resolution control of time scale factor (not limited to multiples of the pitch period)
- Natural sounding speech output for any speaker: male, female, children
- Voice activated recording
- High quality, low rate digital speech compression
- Robust operation under noisy conditions
- Simple host interface
- Low power, CMOS technology

The DSP Group, Inc., 1900 Powell Street, Suite 1120, Emeryville, CA 94608
Tel: (415) 655-7311 Fax: (415) 655-7537



DSPG7002 Block Diagram.

Specifications

AUDIO BANDWIDTH: 0—3200 Hz

AUDIO LEVELS: 100mV—2V PTP

TIME SCALE MODIFICATION FACTORS (default):

- Compression ... 0.5, 0.625, 0.75, 0.875
- Original ... 1
- Expansion ... 1.125, 1.25, 1.5, 1.75, 2

TAPE SPEED CONTROL: Automatic (pulse rate modulated) or via host command

THROUGHPUT DELAY: 16 milliseconds

INTERFACE LEVEL: TTL

IC Repeat length:

- up to 75 seconds (per 1 Mbit)

Physical Description

- DSPG7002-11 Digital Signal Processor (64 pin PLCC) 1ea.
- DSPG7000-25 Analog I/O Processor (24 pin PLCC) 1 ea.
- DSPG7000-31 1 Mbit ARAM - IC Repeat Memory (16 pin DIP) 1 ea.
- DSPG7000-34 64 Kbit SRAM (28 pin PLCC) 1 ea.

Note: Specifications are subject to change without prior notice.