NAND Controller
GLS55LC200

Data Sheet

FEATURES:

- **CompactFlash Association Specification Revision 3.0 Standard Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6
  - Supports up to Multi-word DMA Mode-4
  - Supports up to Ultra DMA Mode-4
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: Single or Dual 8-bit access
    - Supports up to 4 flash media devices per channel
    - Supports up to 8 flash media devices directly
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
    - 2 KByte and 4 KByte program page size
- **3.3V Power Supply and NAND Flash Interface**
- **5.0V or 3.3V Host Interface Through V_{DDQ} Pins**
- **Low Current Operation:**
  - Active mode: 25 mA/35 mA (3.3V/5.0V) (typical)
  - Sleep mode: 80 µA/100 µA (3.3V/5.0V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Programmable, Multitasking NAND Interface**
- **Firmware Storage in Embedded SuperFlash®**
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard CompactFlash commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 8 random single-bit errors per 512-byte sector
- **Built-in Internal System Clock**
- **Multi-tasking Technology Enables Fast Sustained Write Performance (Host to Flash)**
  - Supports up to 30 MByte/sec
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 30 MByte/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 5 sec. (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 100-lead TQFP – 14mm x 14mm
- **All non-Pb (lead-free) Devices are RoHS Compliant**

PRODUCT DESCRIPTION

The GLS55LC200 NAND Controller is the core of a high-performance, flash media-based, data storage system. The controller recognizes the control, address, and data signals on the CF bus and translates them into memory accesses for standard NAND-type flash media. Using both Single Level Cell (SLC) and Multi-Level Cell (MLC) flash media, this technology supports solid state mass storage applications by offering new, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The NAND Controller supports standard CF protocols with up to PIO Mode-6, Multi-word DMA Mode-4, and Ultra DMA Mode-4 interface. The CF interface is widely used in products such as portable and desktop computers, digital cameras, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, and set-top boxes.

The NAND Controller uses SuperFlash® memory technology, and is factory pre-programmed with an embedded flash file system. Upon initial power-on, the GLS55LC200 recognizes the flash media devices, sets up a bad block table, executes all the necessary handshaking routines for flash media support, and, finally, performs the low-level format. This process typically takes about 3 second plus 0.5 seconds per gigabyte of drive capacity, allowing a 4 GByte flash drive to be fully initialized in about 5 seconds. For added manufacturing flexibility, system debug, re-initialization, and user customization can be accomplished through the CF interface.

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The GLS55LC200 high-performance NAND Controller offers sustained read and write performance up to 30 MByte/sec. The GLS55LC200 directly supports up to eight flash media devices with appropriate output loading and frequency.

The NAND Controller comes pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

The NAND controller comes packaged in an industry-standard 100-lead TQFP package for easy integration into an SMT manufacturing process.

GENERAL DESCRIPTION

The NAND Controller contains a microcontroller and embedded flash file system integrated in a TQFP package. Refer to Figure 1 for the NAND Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

Performance-optimized NAND Controller

The NAND Controller translates standard CF signals into flash media data and control signals. The following components contribute to the controller's operation.

Microcontroller Unit (MCU)

The MCU coordinates all related components to complete requested operations.

Internal Direct Memory Access (DMA)

The NAND Controller uses internal DMA which allows instant data transfer from buffer to flash media. This increases the data transfer rate by eliminating the microcontroller overhead associated with the traditional, firmware-based approach.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NAND Controller. It reduces the power consumption of the NAND Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

SRAM Buffer

The NAND Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

Embedded Flash File System

The embedded flash file system is an integral part of the NAND Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media Writes and Reads.
2. Provides flash media wear-leveling to spread the flash writes across all memory address spaces to increase the longevity of flash media.
3. Keeps track of data file structures.

Error Correction Code (ECC)

The NAND Controller uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging process. To aid in validation, always provide the SCI access to PCB design.

Programmable, Multi-tasking NAND Interface

The multi-tasking interface enables fast, sustained write and read performance by allowing multiple Read, Program, and Erase operations to multiple flash media devices. The programmable NAND interface enables timely support of fast changing NAND technology.

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FUNCTIONAL BLOCKS

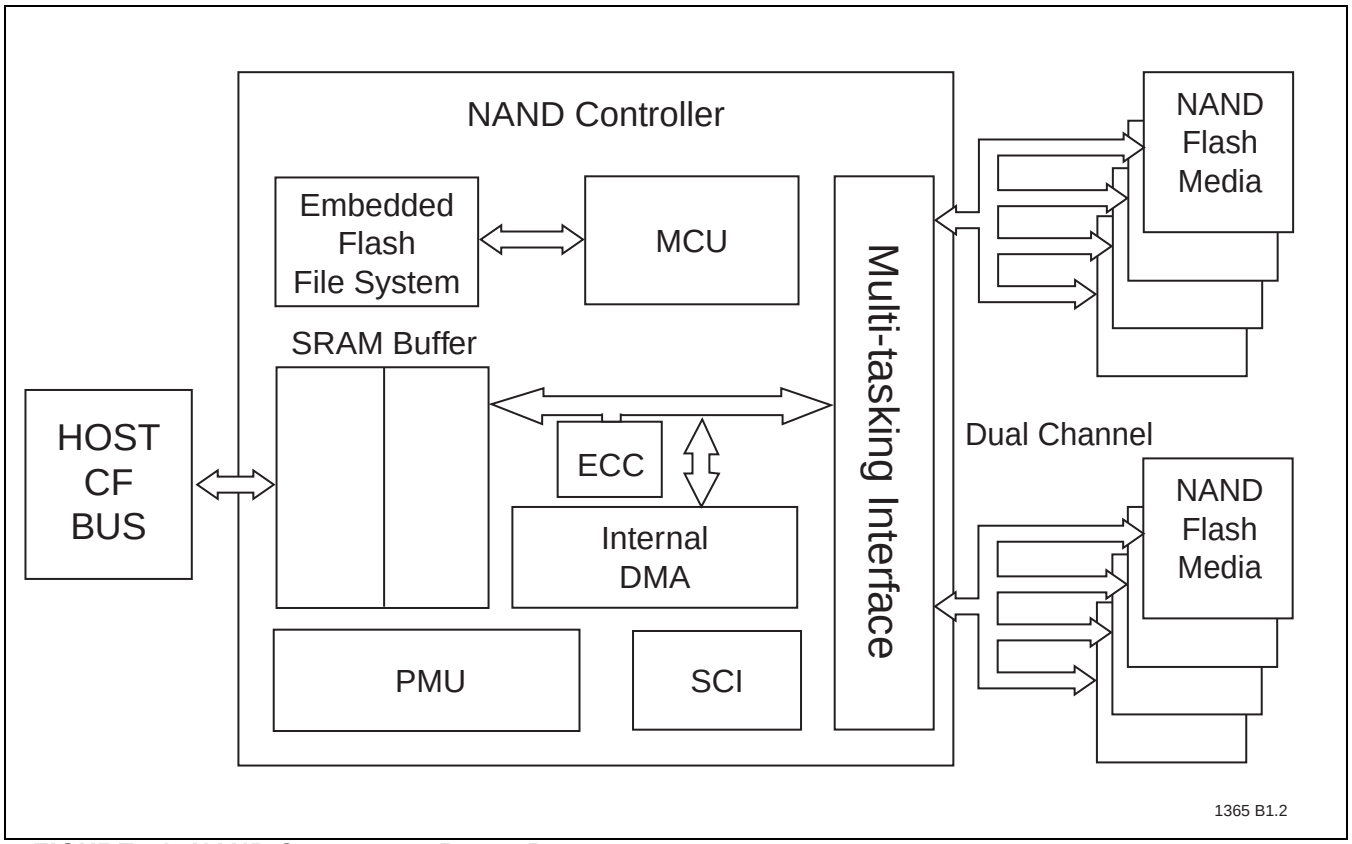
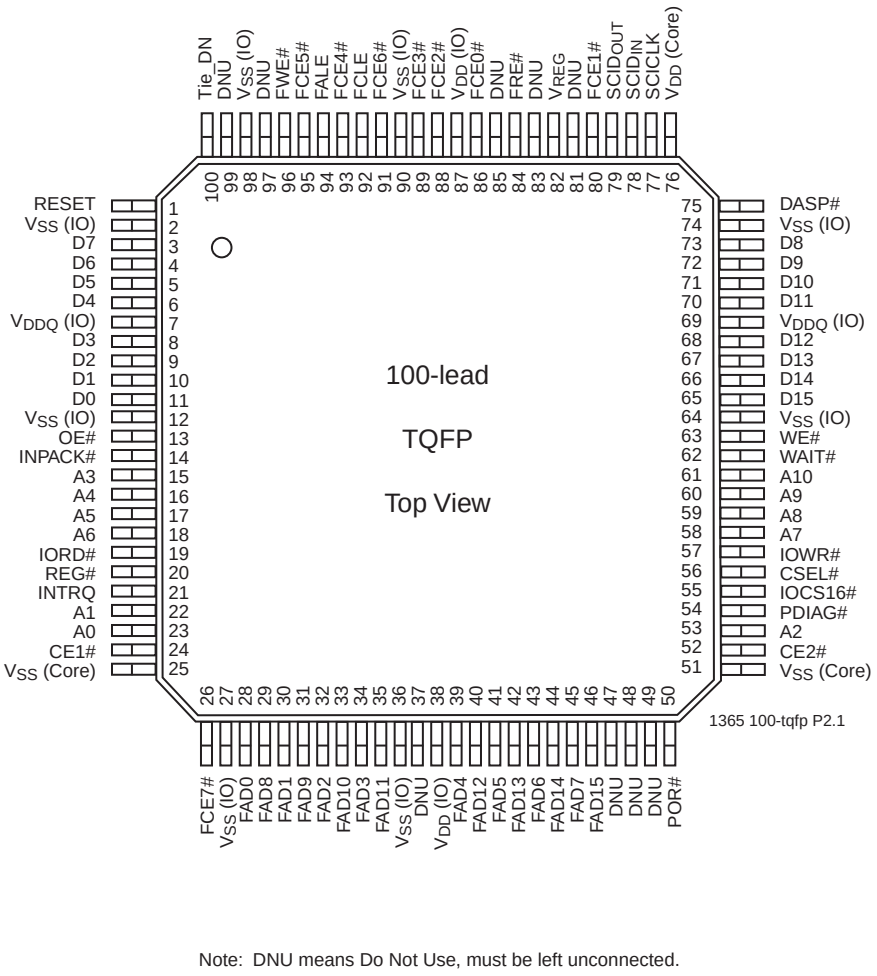


FIGURE 1: NAND CONTROLLER BLOCK DIAGRAM

PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NAND controller sources are outputs.



Note: DNU means Do Not Use, must be left unconnected.

FIGURE 2: PIN ASSIGNMENTS FOR 100-LEAD TQFP

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TABLE 1: PIN ASSIGNMENTS (1 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
Host Interface				
A_{10}-A_0 (Memory Card mode)	61 60 59 58	I	I1Z	These address lines, along with the REG# signal, are used to select the following: The I/O port address registers within the NAND, the memory mapped port address registers within the NAND, a byte in the card's information structure and its configuration control and status registers.
A_{10}-A_0 (PC Card I/O mode)	18 17 16 15 53 22 23			This signal is the same as the PC Card Memory mode signal.
A_2-A_0 (True IDE mode)	53 22 23			In True IDE mode only A[2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
A_{10}-A_3	61 60 59 58 18 17 16 15			
BVD1 (Memory Card mode)	54	I/O	I1U, O1	This signal is asserted high as BVD1 is not supported.
STSCHG# (PC Card I/O mode)				This signal is asserted low to alert the host to changes in the Ready and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status register.
PDIAG# (True IDE mode)				In the True IDE mode, this input/output is the Pass Diagnostic signal in the master/slave handshake protocol.
BVD2 (Memory Card mode)	75	I/O	I1U, O6	This signal is asserted high as BVD2 is not supported.
SPKR# (PC Card I/O mode)				This output line is always driven to a high state in I/O mode since the NAND controller does not support the audio function.
DASP# (True IDE mode)				In the True IDE mode, this input/output is the Disk Active/Slave Present signal in the master/slave handshake protocol.
CE1#, CE2# (Memory Card mode)	24 52	I	I2U	**Card Enable:** These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the Odd Byte of the word. CE1# accesses the Even Byte or the Odd Byte of the word depending on A_0 and CE2#. A multiplexing scheme based on A_0, CE1#, CE2# allows 8-bit hosts to access all data on D_0-D_7.
CE1#, CE2# (PC Card I/O mode)				**Card Enable:** This signal is the same as the PC Card Memory mode signal.
CS0#, CS1# (True IDE mode)				In the True IDE mode CS0# is the chip select for the task file registers while CS1# is used to select the Alternate Status register and the Device Control register.

TABLE 1: PIN ASSIGNMENTS (CONTINUED) (2 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
CSEL# (Memory Card mode)	56	I	I1U	This signal is not used for this mode.
CSEL# (PC Card I/O mode)				This signal is not used for this mode.
CSEL# (True IDE mode)				This internally pulled up signal is used to configure this device as a master or a slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a master. When the pin is open, this device is configured as a slave.
D_{15}-D_0 (Memory Card mode)	65 66 67 68 70 71 72 73 3 4 5 6 8 9 10 11	I/O	I1Z, O2	These lines carry the Data, Commands and Status information between the host and the controller. D_0 is the LSB of the Even Byte of the Word. D_8 is the LSB of the Odd Byte of the Word.
D_{15}-D_0 (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
D_{15}-D_0 (True IDE mode)				In True IDE mode, all Task File operations occur in Byte-Mode on the low order bus D_7-D_0 while all data transfers are 16 bit using D_{15}-D_0.
INPACK# (Memory Card mode)	14	O	O1	This signal is not used in this mode.
INPACK# (PC Card I/O mode)				The Input Acknowledge signal is asserted by the NAND when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the NAND and the CPU.
DMARQ (True IDE mode)				In True IDE mode DMA request to host.
IORD# (Memory Card mode)	19	I	I2U	This signal is not used in this mode.
IORD# (PC Card I/O mode)				This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the NAND when the card is configured to use the I/O interface.
IORD# (True IDE mode)				In True IDE mode, this signal has the same function as in PC card I/O mode.
HDMARDY# (True IDE mode)				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
HSTROBE (True IDE mode)				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.

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TABLE 1: PIN ASSIGNMENTS (CONTINUED) (3 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
IOWR# (Memory Card mode)	57	I	I2U	This signal is not used in this mode.
IOWR# (PC Card I/O mode)				The I/O Write strobe pulse is used to clock I/O data on the card data bus into the NAND controller registers when the NAND is configured to use the I/O interface.
IOWR# (True IDE mode)				In True IDE mode, this signal has the same function as in PC Card I/O mode.
STOP (True IDE mode)				When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst
OE# (Memory Card mode)	13	I	I2U	This is an Output Enable strobe generated by the host interface. It is used to read data from the NAND in Memory mode and to read the CIS and configuration registers.
OE# (PC Card I/O mode)				In PC Card I/O mode, this signal is used to read the CIS and configuration registers.
ATASEL# (True IDE mode)				To enable True IDE mode this input should be grounded by the host.
Ready (Memory Card mode)	21	O	O1	In Memory mode this signal is set high when the NAND is ready to accept a new data transfer operation and held low when the card is busy. At power up and at Reset, the Ready signal is held low (busy) until the NAND has completed its power up or reset function. No access of any type should be made to the NAND during this time.
IREQ# (PC Card I/O mode)				I/O Operation - After the NAND has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE mode)				In True IDE mode signal is the active high Interrupt Request to the host.
REG# (Memory Card mode)	20	I	I2U	This signal is used during Memory cycles to distinguish between Common Memory and Register (Attribute) Memory Attribute Memory Select accesses. High for Common Memory, Low for Attribute Memory.
REG# (PC Card I/O mode)				The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
DMACK (True IDE mode)				In True IDE mode DMA Acknowledge - input from host.
RESET (Memory Card mode)	1	I	I2U	When the pin is high, this signal Resets the NAND. The NAND is Reset only at power up if this pin is left high or open from power-up. The NAND is also Reset when the Soft-Reset bit in the Card Configuration Option register is set.
RESET (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
RESET# (True IDE mode)				In the True IDE mode this input pin is the active low hardware reset from the host.

TABLE 1: PIN ASSIGNMENTS (CONTINUED) (4 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
WAIT# (Memory Card mode)	62	O	O1	The WAIT# signal is driven low by the NAND to signal the host to delay completion of a memory or I/O cycle that is in progress.
WAIT# (PC Card I/O mode)				This signal is the same as the PC Card Memory mode signal.
IORDY# (True IDE mode)				In true IDE mode, except in Ultra DMA modes, this signal may be used as IORDY.
DDMARDY# (True IDE mode)				When Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
DSTROBE (True IDE mode)				When Ultra DMA mode DMA Write is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
WE# (Memory Card mode)	63	I	I2U	This is a signal driven by the host and used for strobing memory write data to the registers of the NAND when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
WE# (PC Card I/O mode)				In PC Card I/O mode, this signal is used for writing the configuration registers.
WE# (True IDE mode)				In True IDE mode this input signal is not used and should be connected to V_{DD} by the host.
WP (Memory Card mode)	55	O	O2	The NAND does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
IOIS16# (PC Card I/O mode)				When the NAND is configured for I/O Operation Pin 55 is used for the I/O# Selected is 16-bit Port (IOIS16#) function. A Low signal indicates that a 16 bit or Odd Byte only operation can be performed at the addressed port.
IOCS16# (True IDE mode)				In True IDE mode this output signal is asserted low when this device is expecting a word data transfer cycle.

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TABLE 1: PIN ASSIGNMENTS (CONTINUED) (5 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
Flash Media Interface				
FRE#	84	O	O5	Active Low Flash Media Chip Read
FWE#	96	O	O5	Active Low Flash Media Chip Write
FCLE	92	O	O5	Active High Flash Media Chip Command Latch Enable
FALE	94	O	O5	Active High Flash Media Chip Address Latch Enable
FAD15	46	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44			
FAD13	42			
FAD12	40			
FAD11	35			
FAD10	33			
FAD9	31			
FAD8	29			
FAD7	45	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43			
FAD5	41			
FAD4	39			
FAD3	34			
FAD2	32			
FAD1	30			
FAD0	28			
FCE7#	26	O	O4	Active Low Flash Media Chip Enable pin
FCE6#	91			
FCE5#	95			
FCE4#	93			
FCE3#	89			
FCE2#	88			
FCE1#	80			
FCE0#	86			
Serial Communication Interface (SCI)				
SCICLK	77	I	I3U	SCI interface clock
$SCID_{IN}$	78	I	I3U	SCI interface data input
$SCID_{OUT}$	79	O	O4	SCI interface data output
Miscellaneous				
V_{DD} (core)	76	PWR		V_{DD} (3.3V)
V_{DD} (IO)	38 87	PWR		V_{DD} (3.3V)
V_{DDQ} (IO)	7 69	PWR		V_{DDQ} (5V/3.3V) for Host interface
V_{REG}	82	O		External capacitor pin. Connect this pin with a 4.7uF capacitor to ground.

TABLE 1: PIN ASSIGNMENTS (CONTINUED) (6 OF 6)

Signal Name	100-lead	Pin Type	I/O Type[1]	Name and Functions
V_{SS} (core)	25 51	PWR		Ground for core
V_{SS} (IO)	2 12 27 36 64 74 90 98	PWR		Ground for I/O
POR#	50	I	Analog Input[2]	**Power-on Reset (POR):** Active Low
Tie_DN	100			Pin must be connected to V_{SS}
DNU[3]	37 47 48 49 81 83 85 97 99			Do Not Use, must be left unconnected.

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1. IxU = Input with on-chip pull-up.
   IxZ = Input without on-chip pull-up.
2. Analog input for supply voltage detection
3. All DNU pins should not be connected.

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CAPACITY SPECIFICATION

Table 2 shows the default capacity and specific settings for heads, sectors, and cylinders. Users can change the default settings in the drive ID table (see Table 20) for customization. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance will be reduced.

TABLE 2: Default NAND Settings

Capacity[1]	Total Bytes	Cylinders[2]	Heads[2]	Sectors[2]	Max LBA
128 MB	128,450,560	490	16	32	250,880
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1 GB	1,024,966,656	1986	16	63	2,001,888
2 GB	2,048,901,120	3970	16	63	4,001,760
4 GB	4,110,188,544	7964	16	63	8,027,712
6 GB	6,146,703,360	11910	16	63	12,005,280
8 GB	8,195,604,480	15880	16	63	16,007,040
16 GB	16,391,208,960	16383[3]	16	63	32,014,080
32 GB	32,001,048,576	16383[3]	16	63	62,502,048

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1. These flash drive capacities can only be manufactured by using the specified version of the Compact Flash Card Controller.
2. Cylinders, Heads, and Sectors can be re-configured from the default settings during the manufacturing process.
3. Cylinders, Heads, and Sectors are not applicable for these capacities. Only LBA addressing applies.

Functional Specifications

Table 4-2 shows the performance and the maximum capacity supported by GLS55LC200.

TABLE 3: Functional Specification

Functions	GLS55LC200
NAND Supported Capacity	up to 32 GB
NAND Performance-Sustained Write speed	Up to 30.0 MB/sec
NAND Performance-Sustained Read speed	Up to 30.0 MB/sec

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MANUFACTURING SUPPORT

The NAND controller firmware contains a list of supported standard NAND flash media devices. Upon initial Power-on, the controller scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices in the NAND controller, the controller performs drive recognition based on the algorithm provided by the flash media suppliers. This includes setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format.

Please contact Greenliant for the most current list of supported NAND Flash media devices.

In the event that the NAND flash media device ID is not recognized by the NAND controller, the user has an option of adding this device to the controller device table through the manufacturing interface provided by Greenliant. Please contact Greenliant for the NAND controller manufacturing interface software. If the drive initialization fails, and a visual inspection is unable to determine the problem, the GLS55LC200 NAND controller provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

CF Interface

The CompactFlash interface can be used for manufacturing support. Greenliant provides an example of a DOS-based solution (an executable routine downloadable from Greenliant's web site) for manufacturing debug and rework.

Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used to report manufacturing errors. The SCI consists of 3 active signals: $SCID_{OUT}$, $SCID_{IN}$, and SCICLK.

POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Power-on and Brown-out Reset circuitry reset the device to a known state. Power-on Reset asserts when the device is turned on. Brown-out Reset asserts when the detected voltage falls below an acceptable level. For more information about the Power-on and Brown-out Reset timing, see Figure 3 and Table 4.

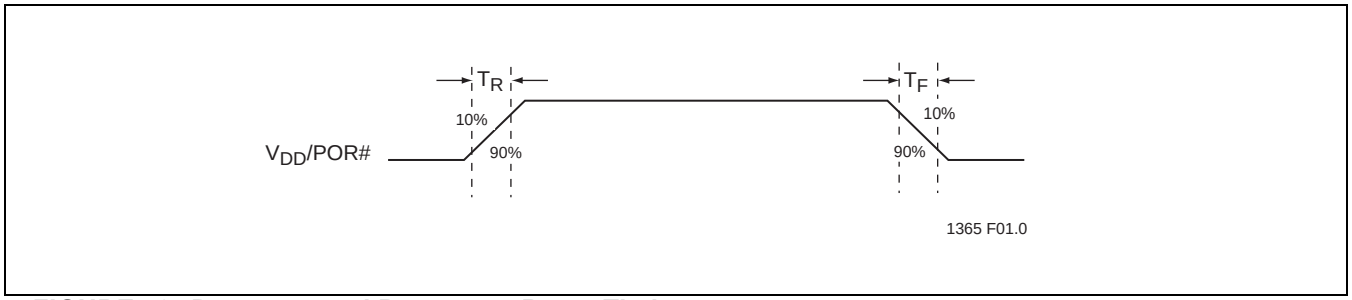

FIGURE 3: Power-on and Brown-out Reset Timing

TABLE 4: Power-on and Brown-out Reset Timing

Item	Symbol	Min	Max	Units
V_{DD}/POR# Rise Time[1]	T_R		200	ms
V_{DD}/POR# Fall Time[2]	T_F		200	ms

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1. V_{DD} Rise Time should be greater than or equal to POR# Rise Time.
2. V_{DD} Fall Time should be slower than or equal to POR# Fall Time.

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CARD CONFIGURATION

The NANDs are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the NAND that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

TABLE 5: Registers and Memory Space Decoding

CE2#	CE1#	REG#	OE#	WE#	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_7-D_0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_{15}-D_8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit D_{15}-D_0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_7-D_0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_{15}-D_8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit D_{15}-D_0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

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TABLE 6: Configuration Registers Decoding

CE2#	CE1#	REG#	OE#	WE#	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

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Note: The location of the card configuration registers should always be read from the CIS locations 0000H to 0198H.
No writes should be performed to the NAND attribute memory except to the card configuration register addresses.
All other attribute memory locations are reserved.

Attribute Memory Function

Attribute memory is a space where NAND identification and configuration information are stored. This memory is limited to 8-bit wide accesses, only at even addresses. The card configuration registers are also located in this space.

For the Attribute Memory Read function, signals REG# and OE# must be active and WE# inactive during the cycle. As in the Main Memory Read functions, the signals CE1# and CE2# control the Even Byte and Odd Byte address, but only the Even Byte data is valid during the Attribute Memory access. Refer to Table 7 below for signal states and bus validity for the Attribute Memory function.

TABLE 7: Attribute Memory Function

Function Mode	REG#	CE2#	CE1#	A_{10}	A_9	A_0	OE#	WE#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access CIS (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Don't Care	Even Byte

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Note: The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

Configuration Option Register (Address 200H in Attribute Memory)

The Configuration Option register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the NAND.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET — Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the NAND in the Reset state. Setting this bit to one (1) is equivalent to assertion of the RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the NAND in the same un-configured Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control register.

LevlREQ — This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse mode is selected. Set to zero (0) by Reset.

Conf5-Conf0 — Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the NAND as shown below.
Note: Conf5 and Conf4 are reserved and must be written as (0).

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TABLE 8: Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, any 16 Byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0H-1F7H/3F6H-3F7H
0	0	0	0	1	1	I/O Mapped, 170H-177H/376H-377H

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TABLE 9: Card Configuration and Status Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	XE#	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	XE#	Audio	PwrDwn	0	0

Changed — Indicates that one or both of the Pin Replacement register CRdy or CWProt bits are set to one (1). When the Changed bit is set, Pin 46 (STSCHG#) is held low if the SigChg bit is a One (1) and the NAND is configured for the I/O interface.

SigChg — This bit is set and reset by the host to enable and disable a state-change “signal” from the Status register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (STSCHG#) signal will be held high while the NAND is configured for I/O.

IOis8 — The host sets this bit to a one (1) if the NAND is to be configured in an 8-bit I/O mode. The NAND is always configured for both 8- and 16-bit I/O, so this bit is ignored.

XE#: — This bit has value 0 and is not writable.

Audio: — This bit should always be zero for NANDs.

PwrDwn — This bit indicates whether the host requests the NAND to be in the power saving or active mode. When the bit is one (1), the NAND enters a power down mode. When zero (0), the host is requesting the NAND to enter the active mode. The PCMCIA Ready value becomes BUSY when this bit is changed. Ready will not become ready until the power state requested has been entered. The NAND automatically powers down when it is idle and powers back up when it receives a command.

Int — This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEn bit in the Device Control register, this bit is a zero (0).

Pin Replacement Register (Address 204H in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRDY/BSY#	CWProt	1	1	RDY/BSY#	WProt
Write	0	0	CRDY/BSY#	CWProt	0	0	MRDY/BSY#	MWProt

CRDY/BSY# This bit is set to one (1) when the bit RDY/BSY# changes state. This bit can also be written by the host.

CWProt This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RDY/BSY# This bit is used to determine the internal state of the RDY/BSY# signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRDY/BSY#.

WProt: This bit is always zero (0).
When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRDY/BSY# This bit acts as a mask for writing the corresponding bit CRDY/BSY#.

MWProt: This bit when written acts as a mask for writing the corresponding bit CWProt.

TABLE 10: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by host
X	1	1	1	Set by host

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Socket and Copy Register (Address 206H in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

Reserved This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive # This bit indicates the drive number of the card for twin card configuration.
Twin card configuration is currently not supported

X The socket number is ignored by the NAND.

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I/O Transfer Function

I/O Function

The I/O transfer to or from the NAND can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal IOIS16# is asserted by the NAND. Otherwise, the IOIS16# signal is de-asserted. When a 16 bit transfer is attempted, and the IOIS16# signal is not asserted by the NAND, the system must generate a pair of 8-bit references to access the word's Even Byte and Odd Byte. The NAND permits both 8 and 16 bit accesses to all of its I/O addresses, so IOIS16# is asserted for all addresses to which the NAND responds.

TABLE 11: I/O Function

Function Code	REG#	CE2#	CE1#	A_0	IORD#	IOWR#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Input Access (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Odd Byte
Byte Output Access (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	Odd Byte
Word Input Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word Output Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Odd Byte	Even Byte
I/O Read Inhibit	V_{IH}	X	X	X	V_{IL}	V_{IH}	Don't Care	Don't Care
I/O Write Inhibit	V_{IH}	X	X	X	V_{IH}	V_{IL}	High Z	High Z
High Byte Input Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
High Byte Output Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

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Common Memory Transfer Function

Common Memory Function

The Common Memory Transfer to or from the NAND can be either 8 or 16 bits.
The NAND permits both 8 and 16 bit accesses to all of its Common Memory addresses.

TABLE 12: Common Memory Function

Function Code	REG#	CE2#	CE1#	A_0	OE#	WE#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Read Access (8 bits)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Odd Byte
Byte-Write Access (8 bits)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	Odd Byte
Word Read Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word-Write Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
Odd Byte-Write Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

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True IDE Mode I/O Transfer Function

True IDE Mode I/O Function

The NAND can be configured in a True IDE mode of operation. The NAND is configured in this mode only when the OE# input signal is grounded by the host during the power off to power on cycle. In this True IDE mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data register are allowed. In this mode no Memory or Attribute registers are accessible to the host. NANDs permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

Note: Removing and reinserting the NAND while the host computer's power is on will reconfigure the Compact-Flash to PC Card ATA mode from the original True IDE mode. To configure the NAND in True IDE mode, the 50-pin socket must be power cycled with the NAND inserted and OE# (output enable) asserted.

Table 13 defines the function of the operations for the True IDE mode.

TABLE 13: True IDE Mode I/O Function

Function Code	CE2#	CE1#	A_0-A_2	IORD#	IOWR#	D_{15}-D_8	D_7-D_0
Invalid mode	V_{IL}	V_{IL}	X	X	X	High Z	High Z
Standby mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	Don't Care	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	Odd Byte In	Even Byte In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Odd Byte Out	Even Byte Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	Don't Care	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out

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SOFTWARE INTERFACE

CF-ATA Drive Register Set Definition and Protocol

The NAND can be configured as a high performance I/O device through:

1. Standard PC-AT disk I/O address spaces 1F0H-1F7H, 3F6H-3F7H (primary); 170H-177H, 376H-377H (secondary) with IRQ 14 (or other available IRQ)
2. Any system decoded 16 Byte I/O block using any available IRQ
3. Memory space

The communication to or from the NAND is done using the Task File registers which provide all the necessary registers for control and status information. The CompactFlash interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods.

TABLE 14: I/O Configurations

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0H-FH, 400H-7FFH	Memory Mapped
1	I/O	XX0H-XXFH	I/O Mapped 16 Contiguous registers
2	I/O	1F0H-1F7H, 3F6H-3F7H	Primary I/O Mapped
3	I/O	170H-177H, 376H-377H	Secondary I/O Mapped

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I/O Primary and Secondary Address Configura- tions

TABLE 15: Primary and Secondary I/O Decoding

REG#	A_9-A_4	A_3	A_2	A_1	A_0	IORD#=0	IOWR#=0	Note
0	1F(17)H	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)H	0	0	0	1	Error register	Features	1,2
0	1F(17)H	0	0	1	0	Sector Count	Sector Count	
0	1F(17)H	0	0	1	1	Sector No.	Sector No.	
0	1F(17)H	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)H	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)H	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)H	0	1	1	1	Status	Command	
0	3F(37)H	0	1	1	0	Alt Status	Device Control	

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1.Register 0 is accessed with CE1# low and CE2# low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D_{15}-D_0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.

2.A byte access to register 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

Note: Address lines which are not indicated are ignored by the NAND for accessing all the registers in this table.

Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the NAND, the registers are accessed in the block of I/O space decoded by the system as follows:

TABLE 16: Contiguous I/O Decoding

REG#	A_3	A_2	A_1	A_0	Offset	IORD#=0	IOWR#=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	

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1. Register 0 is accessed with CE1# low and CE2# low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9, and D are non-overlapping duplicates of the registers at offset 0 and 1.
   Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

   Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

Note: Address lines which are not indicated are ignored by the NAND for accessing all the registers in this table.

Memory Mapped Addressing

When the NAND registers are accessed via memory references, the registers appear in the common memory space window: 0-2 KByte as follows:

TABLE 17: Memory Mapped Decoding

REG#	A_{10}	A_9-A_4	A_3	A_2	A_1	A_0	Offset	OE#=0	WE#=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	X	0	0	0	1	1	Error	Features	1,2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	

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TABLE 17: Memory Mapped Decoding

REG#	A_{10}	A_9-A_4	A_3	A_2	A_1	A_0	Offset	OE#=0	WE#=0	Notes
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

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1.Register 0 is accessed with CE1# low and CE2# low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.
A byte access to address 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

2.Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

3.Accesses to even addresses between 400H and 7FFH access register 8. Accesses to odd addresses between 400H and 7FFH access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data register FIFO and does not allow random access to the data buffer within the NAND. A word access to address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

True IDE Mode Addressing

When the NAND is configured in the True IDE mode, the I/O decoding is as follows:

TABLE 18: True IDE Mode I/O Decoding

CE2#	CE1#	A_2	A_1	A_0	IORD#=0	IOWR#=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control

TABLE 18: True IDE Mode I/O Decoding

CE2#	CE1#	A_2	A_1	A_0	IORD#=0	IOWR#=0

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CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when CE1# is high and CE2# is low unless IOIS16# is high (not asserted) and an I/O cycle is being performed.

Data Register (Address - 1F0H[170H];Offset 0,8,9) The Data register is a 16 bit register, and it is used to transfer data blocks between the NAND data buffer and the Host. This register overlaps the Error register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data register and Error/Feature register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, access to the 1F1H, 171H or offset 1 are not defined for word (CE2#=0 and CE1#=0) operations. These accesses are treated as accesses to the Word Data register. The duplicated registers at offsets 8, 9 and DH have no restrictions on the operations that can be performed by the socket.

Data Register	CE2#	CE1#	A_0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D_{15}-D_0
Even Data Register	1	0	0	0,8	D_7-D_0
Odd Data Register	1	0	1	9	D_7-D_0
Odd Data Register	0	1	X	8,9	D_{15}-D_8
Error / Feature Register	1	0	1	1, DH	D_7-D_0
Error / Feature Register	0	1	X	1	D_{15}-D_8
Error / Feature Register	0	0	X	DH	D_{15}-D_8

Error Register (Read Only) This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BBK	UNC	0	IDNF	0	ABRT	0	AMNF	**0000 0000b**

Symbol **Function**

Bit 7 (ICRC/BBK) This bit is set when a Bad Block is detected. During an ultra-DMA transfer, this bit is set on detection of a CRC error.

Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.

Bit 5 This bit is 0.

Bit 4 (IDNF) The requested sector ID is in error or cannot be found.

Bit 3 This bit is 0.

Bit 2 (ABRT) This bit is set if the command has been aborted because of an NAND Controller status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been

issued. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that ends with an error condition.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

Feature Register (Address - 1F1H[171H]; Offset 1, 0DH Write Only) This register provides information regarding features of the NAND that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with CE2# low and CE1# high.

Sector Count Register (Address - 1F2H[172H]; Offset 2) This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the NAND. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Sector Number (LBA 7-0) Register (Address - 1F3H[173H]; Offset 3) This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any NAND data access for the subsequent command.

Cylinder Low (LBA 15-8) Register (Address - 1F4H[174H]; Offset 4) This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of then Logical Block Address.

Cylinder High (LBA 23-16) Register (Address - 1F5H[175H]; Offset 5) This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

Drive/Head (LBA 27-24) Register (Address 1F6H[176H]; Offset 6) The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol **Function**

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number register D7-D0.

LBA15-LBA8: Cylinder Low register D7-D0.

LBA23-LBA16: Cylinder High register D7-D0.

LBA27-LBA24: Drive/Head register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. The NAND is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Status & Alternate Status Registers (Address 1F7H[177H]&3F6H[376H]; Offsets 7 & E) These registers return the NAND status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	**1000 0000b**

Symbol **Function**

Bit 7 (BUSY) The busy bit is set when the NAND has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing NAND operations. This bit is cleared at power up and remains cleared until the NAND is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the NAND is ready.

Bit 3 (DRQ) The Data Request is set when the NAND requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is required that the host retry any media access command (such as Read Sectors and Write Sectors) that ends with an error condition.

Device Control Register (Address - 3F6H[376H]; Offset E) This register is used to control the NAND interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	X	X	X	X	SW Rst	-IEn	0	**0000 1000b**

Symbol **Function**

Bits 7-3 These bits are ignored by the NAND.

Bit 2 (SW Rst) This bit is set to 1 in order to force the NAND to perform an ATA Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration registers (Sections to) as a hardware reset does. The card remains in Reset until this bit is reset to ‘0.’

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Bit1(-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the NAND are disabled. This bit also controls the Int bit in the Configuration and Status register. This bit is set to 0 at Power-on and Reset.

Bit0 This bit is ignored by the NAND.

CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the NANDs. Commands are issued to the NAND by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes (see Table 19) of command acceptance, all dependent on the host not issuing commands unless the NAND is not busy (BSY=0).

Table 19 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

TABLE 19: NAND Controller Command Set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase-Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format-Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-

TABLE 19: NAND Controller Command Set (Continued) (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Translate-Sector	87H	-	Y	Y	Y	Y	Y
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector(s)-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

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1.FR - Features register
2.SC - Sector Count register
3.SN - Sector Number register
4.CY - Cylinder registers
5.DH - Drive/Head register
6.LBA - Logical Block Address mode supported (see command descriptions for use)
7.Y - The register contains a valid parameter for this command.
8.For the Drive/Head register:Y means both the NAND Controller and Head parameters are used;
D means only the NAND Controller parameter is valid and not the Head parameter.

Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the NAND Controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 20. All reserved bits or words are zero. Table 20 gives the definition for each field in the Identify-Drive information.

TABLE 20: Identify-Drive Information (1 of 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	xxxxH	2	Reserved
5	xxxxH	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[3]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-14	eeeeH[4]	10	User-programmable serial number in ASCII

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TABLE 20: Identify-Drive Information (Continued) (2 of 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
15-19	ddddH[5]	10	Greenliant preset, unique ID in ASCII
20	0002H	2	Buffer type
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[6]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[7]	40	User Definable Model number
47	8001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	01xxH	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	0x07H	2	DMA data transfer is supported in NAND Controller
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80-81	0000H	4	Reserved – NAND does not return an ATA version
82	706AH	2	Features/command sets supported
83	400CH	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	xx1FH	2	UDMA modes
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91-127	0000H	74	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-162	0000H	6	Reserved
163	xx12H	2	CF Advanced True IDE Timing Mode capabilities and settings
164	001BH	2	CF Advanced PC Card I/O and Memory Timing Mode capability
165-255	0000H	184	Reserved

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1. XXXX = This field is subject to change by the host or the device.
2. bbbb - default value set by controller. The selections could be user programmable.

3. n - calculated data based on product configuration
4. eeee - the default value is '0000000000'
5. dddd - unique number of each device
6. aaaa - any unique Greenliant firmware revision
7. cccc - default value is 'xxxMB NAND' or 'xxxGB NAND' where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

Word 0: General Configuration Word 0 indicates the general characteristics of the device. Depending on the desired configuration, this field can utilize standard or alternate configuration values.

In standard configuration, when Word 0 of the Identify drive information is 848AH, then the device acts as a CompactFlash storage card, operating in compliance with the CFA specification and command sets. PCMCIA operation modes should only report 848AH value if they are always intended as removable devices.

Bit	Function
15-0	Standard Configuration Value 848AH: This is the recommended value.

To use the CompactFlash as the root storage device, some systems require Bit 6 of Word 0 to be set to '1.' This configuration is necessary when all the disk storage in a host is replaced by the CF in True IDE mode. To allow for this alternate configuration, the following values for Word 0 are valid.

Bit	Function
15-0	CF Preferred Alternate Configuration Values 044AH: Alternate value of Word 0. This value turns on ATA device and turns off the removable media and removable device while preserving all retired bits. 0040H: This value turns on ATA device and turns off the removable media and removable device while zeroing all retired bits.
15-12	Configuration Flag 8H: Word 0 = 848AH 0H: Bits [11:0] are set as described in below. The CF supports the CFA command set and report that in Bit 2 of Word 83. All other values for Bits [15:12] are prohibited.

Bit	Name	Definition
11-8	Retired	Retired ATA bit definitions. The value of these bits should be either the preferred value of '0H' or the value of '4H'.
7	Removable Media Device	1: Card contains media that can be removed during operation 2: Card contains non-removable media
6	Not Removable Controller and/or Device	1: Card is non-removable during operation 2: Card can be removed during operation.
5-0	Retired/Reserved	Retired ATA bit definitions. These value of these bits should either be '00H' or '0AH'. Bit 2 = '0' Bit 0 = '0' (reserved)

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Word 1: Default Number of Cylinders This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads This field contains the number of translated heads in the default translation mode.

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Word 6: Default Number of Sectors per Track This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors This field contains the number of sectors per NAND Controller. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

Word 10-19: Serial Number The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a Greenliant preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of spaces.

Word 20: Buffer Type This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the NAND Controller.

Word 23-26: Firmware Revision This field contains the revision of the firmware for this product.

Word 27-46: Model Number This field is reserved for the model number for this product.

Word 47: Read-/Write-Multiple Sector Count This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only value of '1' is supported.

Word 49: Capabilities BitFunction

13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: NAND Controller supports PIO Mode-4.
9	LBA support 1: NAND Controller supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

Word 51: PIO Data Transfer Cycle Timing Mode This field defines the mode for PIO data transfer. NAND Controller supports up to PIO Mode-4.

Word 53: Translation Parameters Valid BitFunction

0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and 4.
2	1: words 88 are valid to support Ultra DMA data transfer.

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

Word 60-61: Total Sectors Addressable in LBA Mode This field contains the number of sectors addressable for the NAND Controller in LBA mode only.

Word 63: Multi-word DMA Transfer Mode This field identifies the multi-word DMA transfer modes supported by the NAND Controller and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

Word 64: Advanced PIO Data Transfer Mode Bits (7:0) is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits (7:2) are Reserved for future PIO modes.

Bit	Function
0	1: NAND Controller supports PIO Mode-3.
1	1: NAND Controller supports PIO Mode-4.

Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the NAND Controller supports when performing Multi-word DMA transfers on a per word basis. Greenliant's NAND Controller supports up to Multi-word DMA Mode-2, so this field is set to 120ns.

Word 66: Device Recommended Multi-word DMA Cycle Time This field defines the NAND Controller recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the NAND Controller may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at

this rate does not ensure that flow control will not be used, but implies that higher performance may result. Greenliant's NAND Controller supports up to Multi-word DMA Mode-2, so this field is set to 120 ns.

Word 67: Minimum PIO Transfer Cycle Time Without Flow Control This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one.The NAND Controller's minimum cycle time is 120 ns. A value of 0078H is reported.

Word 68: Minimum PIO Transfer Cycle Time With IORDY This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The NAND Controller's minimum cycle time is 120 ns, e.g., PIO Mode-4. A value of 0078H is reported.

Words 82-84: Features/command sets supported Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	0: SMART feature set is not supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13-9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported
2	1: CFA feature set is supported

1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Words 85-87: Features/command sets enabled Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-9	0: Reserved
8	0: Set-Max security extension not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled

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2	0: CFA feature set is disabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	**Function**
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Word 88: UDMA Modes	**BitFunction**
15-13	Reserved
12	1: Ultra DMA mode 4 is selected
	0: Ultra DMA mode 4 is not selected
11	1: Ultra DMA mode 3 is selected
	0: Ultra DMA mode 3 is not selected
10	1: Ultra DMA mode 2 is selected
	0: Ultra DMA mode 2 is not selected
9	1: Ultra DMA mode 1 is selected
	0: Ultra DMA mode 1 is not selected
8	1: Ultra DMA mode 0 is selected
	0: Ultra DMA mode 0 is not selected
7-5	Reserved
4	1: Ultra DMA mode 4 and below are supported
3	1: Ultra DMA mode 3 and below are supported
2	1: Ultra DMA mode 2 and below are supported
1	1: Ultra DMA mode 1 and below are supported
0	1: Ultra DMA mode 0 is supported

Word 89: Time required for Security erase unit completion Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes

Value	Time
255	>508 minutes

Word 128: Security Status BitFunction

8 Security Level
1: Security mode is enabled and the security level is maximum
0: and security mode is enabled, indicates that the security level is high

5 Enhanced security erase unit feature supported
1: Enhanced security erase unit feature set is supported

4 Expire
1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset

3 Freeze
1: Security is frozen

2 Lock
1: Security is locked

1 Enable/Disable
1: Security is enabled
0: Security is disabled

0 Capability
1: NAND Controller supports security mode feature set
0: NAND Controller does not support security mode feature set

Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings This word describes the capabilities and current settings for CF modes utilizing the True IDE interface.

Four separate fields determine support and selection options in the Advanced PIO and Advanced Multi-word DMA timing modes. For information on the older modes, see “Word 63: Multi-word DMA Transfer Mode” on page 31 and “Word 64: Advanced PIO Data Transfer Mode” on page 31. When the Identity drive command executes, the device returns 0492H.

Bit **Function**

2-0 Advanced True IDE PIO Mode Support
Indicates the maximum True IDE PIO mode supported by the card

Value	Time
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

5-3 Advanced True IDE Multi-word DMA Mode Support
Indicates the maximum True IDE Multi-word DMA mode supported by the card

Value	Time
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

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8-6 Advanced True IDE PIO Mode Selected
Indicates the current True IDE PIO mode selected on the card

Value	Time
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

11-9 Advanced True IDE Multi-word DMA Mode Selected
Indicates the current True IDE Multi-word DMA mode selected on the card

Value	Time
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

15-12 Reserved

Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 21 defines all features that are supported.

TABLE 21: Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H[1]	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 22 defines the values.
09H	Enable Extended Power Operations
0AH	NOP - Accepted for backward compatibility.
55H[1]	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H[1]	Disable Write Cache
89H	Disable Extended Power operations
8AH	NOP - Accepted for backward compatibility.

TABLE 21: Features Supported

Feature	Operation
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH[2]	Set the host current source capability Allows trade-off between current drawn and Read/Write speed
BBH	4 Bytes of data apply on Read/Write-Long-Sector commands.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

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1. Greenliant NAND controller does not implement cache operations. These commands are returned with no error.
2. Greenliant NAND controller has fixed power consumption. The command will be accepted and returned with no error.

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

TABLE 22: Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

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1. Mode = transfer mode number, all other values are not valid

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

Data Sheet

Error Posting

The following table summarizes the valid status and error value for all the CF-ATA Command set.

TABLE 23: Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check-Power-mode				V		V	V	V		V
Execute-Drive-Diagnostic						V		V		V
Erase-Sector(s)	V		V	V	V	V	V	V		V
Flush-Cache				V		V	V	V		V
Format-Track			V	V	V	V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request-Sense				V		V		V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-mode				V		V	V	V		V
Set-Sleep-mode				V		V	V	V		V
Stand-By				V		V	V	V		V
Stand-By-Immediate				V		V	V	V		V
Translate-Sector	V		V	V	V	V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple -w/o-Erase	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-w/o-Erase	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

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Note: V = valid on this command

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
D.C. Voltage on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential . . . . . -0.5V to V_{DDQ}+0.5V
Transient Voltage (<20 ns) on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential . . . . . -2.0V to V_{DDQ}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Please refer to Table 1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 24: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

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TABLE 25: Operating Range

Range	Ambient Temperature	V_{DD}		V_{DDQ}			
		3.3V		3.3V		5V	
		Min	Max	Min	Max	Min	Max
Commercial	0°C to +70°C	3.135V	3.465V	3.135V	3.465V	4.5V	5.5V
Industrial	-40°C to +85°C	3.135V	3.465V	3.135V	3.465V	4.5V	5.5V

TABLE 26: AC Conditions of Test

Input Rise/Fall Time . . . . . 10 ns
Output Load Media . . . . . C_L = 100 pF for 3.3V / 80 pF for 3V
Output Load Host . . . . . C_L = 100 pF
See Figure 4

Note: All AC specifications are guaranteed by design.

Data Sheet

TABLE 27: Recommended System Power-on Timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready	3 sec + (0.5 sec/ GByte)	100	sec
$T_{PU-READY1}$[1]	Host Power-on/Reset to Ready Operation	200	1000	ms
$T_{PU-WRITE1}$[1]	Host Power-on/Reset to Write Operation	200	1000	ms

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 28: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	10 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 29: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

DC Characteristics

TABLE 30: DC Characteristics for Media Interface V_{DD} = 3.3V

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH3} V_{IL3}	I3	Input Voltage	2.0	 0.8	V	V_{DD}=V_{DD} Max V_{DD}=V_{DD} Min
I_{IL3}	I3Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{U3}	I3U	Input Pull-Up Current	-160	-20	uA	V_{IN} = GND, V_{DD} = V_{DD} Max
V_{T+4} V_{T-4}	I4	Input Voltage Schmitt Trigger	 0.8	2.0	V	V_{DD} = V_{DD} Max V_{DD} = V_{DD} Min
I_{IL4}	I4Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{OH4} V_{OL4}	O4	Output Voltage	2.4	 0.4	V	I_{OH4}=I_{OH4} Min I_{OL4}=I_{OL4} Max
I_{OH4}		Output Current	-2		mA	V_{DD}=V_{DD} Min
I_{OL4}		Output Current		2	mA	V_{DD}=V_{DD} Min
V_{OH5} V_{OL5}	O5	Output Voltage	2.4	 0.4	V	I_{OH5}=I_{OH5} Min I_{OL5}=I_{OL5} Max
I_{OH5}		Output Current	-4		mA	V_{DD}=V_{DD} Min
I_{OL5}		Output Current		4	mA	V_{DD}=V_{DD} Min

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TABLE 31: DC Characteristics for Host Interface V_{DDQ} = 3.3V or V_{DDQ} = 5V

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1} V_{IL1}	I1	Input Voltage	2.0	 0.8	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-150	-6	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{T+2} V_{T-2}	I2	Input Voltage Schmitt Trigger	 0.8	2.0	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-150	-6	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{OH1} V_{OL1}	O1	Output Voltage	2.4	 0.4	V	I_{OH1}=I_{OH1} Min I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2} V_{OL2}	O2	Output Voltage	2.4	 0.4	V	I_{OH2}=I_{OH2} Min I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-8		mA	V_{DDQ} Min
I_{OL2}		Output Current		8	mA	V_{DDQ} Min
V_{OH6} V_{OL6}	O6	Output Voltage for DASP# pin	2.4	 0.4	V	I_{OH6}=I_{OH6} Min I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current for DASP# pin	-4		mA	V_{DDQ} Min
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ} Max

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TABLE 32: Power Consumption

Symbol	Type	Parameter	Min	Max	Units	Conditions
I_{DD}[1,2]	PWR	Power supply current (T_A = 0°C to +70°C)		50	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{DD}[1,2]	PWR	Power supply current (T_A = -40°C to +85°C)		100	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = 0°C to +70°C)		700	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = -40°C to +85°C)		950	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max

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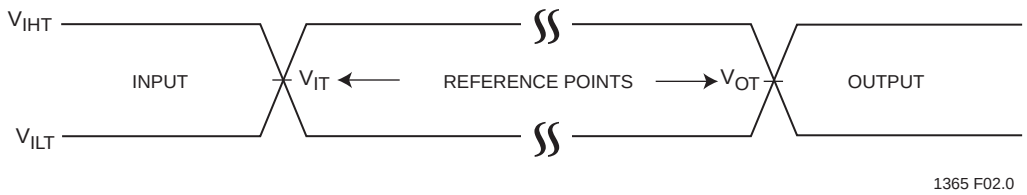
1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Data Sheet

AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 4: AC Input/Output Reference Waveforms

Media Side Interface Timing Specifications

TABLE 33: GLS55LC200 Timing Specifications

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	30	-	ns
T_{CLH}	FCLE Hold Time	20	-	ns
T_{CS}	FCE# Setup Time	30	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	20	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	15	-	ns
T_{WP}	FWE# Pulse Width	16	-	ns
T_{WH}	FWE# High Hold Time	10	-	ns
T_{WC}	Write Cycle Time	30	-	ns
T_{ALS}	FALE Setup Time	30	-	ns
T_{ALH}	FALE Hold Time	20	-	ns
T_{DS}	FAD[15:0] Setup Time	15	-	ns
T_{DH}	FAD[15:0] Hold Time	5	-	ns
T_{RP}	FRE# Pulse Width	16	-	ns
T_{RR}	Ready to FRE# Low	20	-	ns
T_{RES}	FRE# Data Setup Time	4	-	ns
T_{RC}	Read Cycle Time	30	-	ns
T_{REH}	FRE# High Hold Time	10	-	ns

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Note: All AC specifications are guaranteed by design.

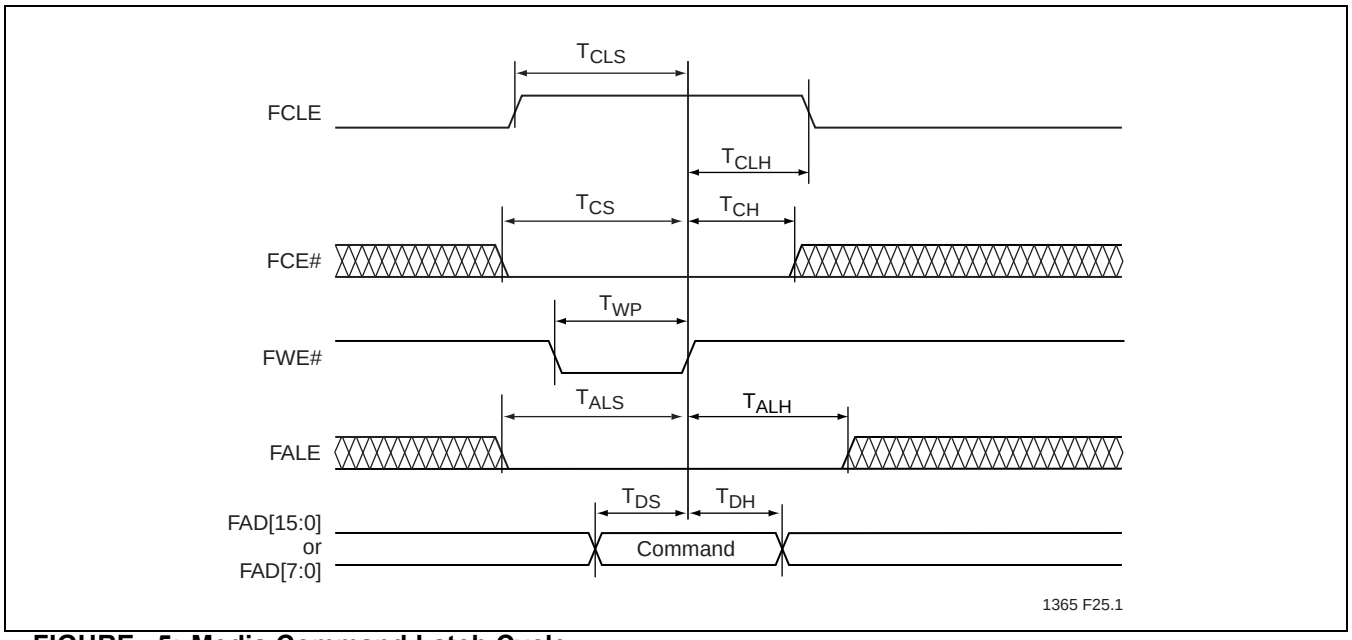


FIGURE 5: Media Command Latch Cycle

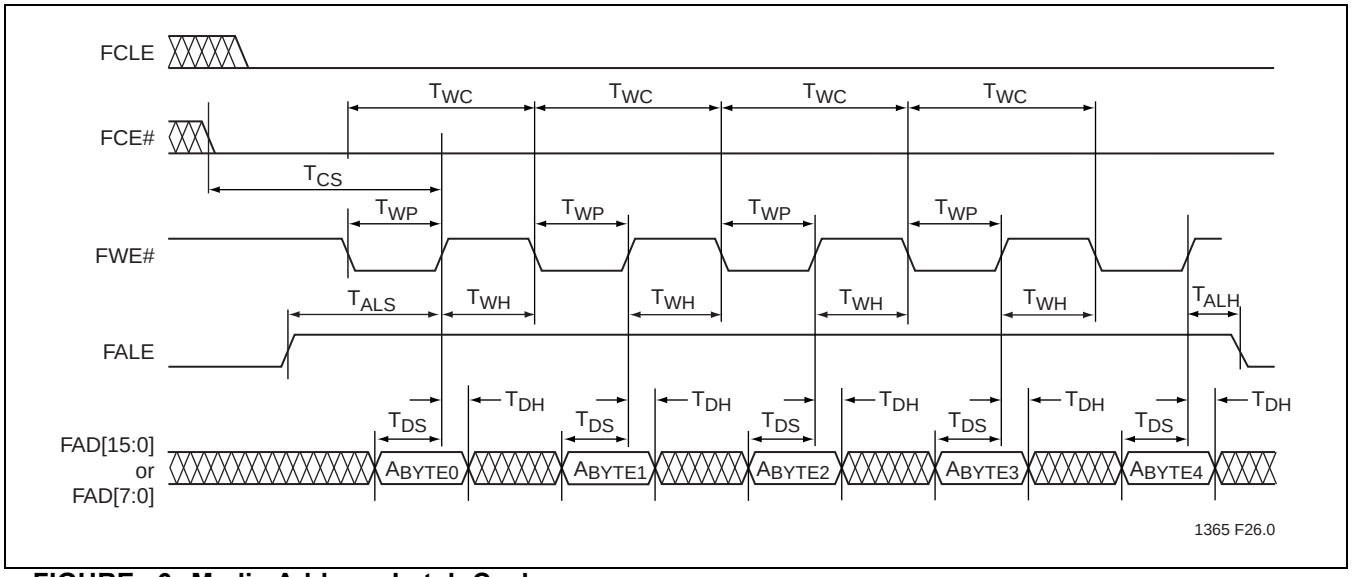


FIGURE 6: Media Address Latch Cycle

Data Sheet

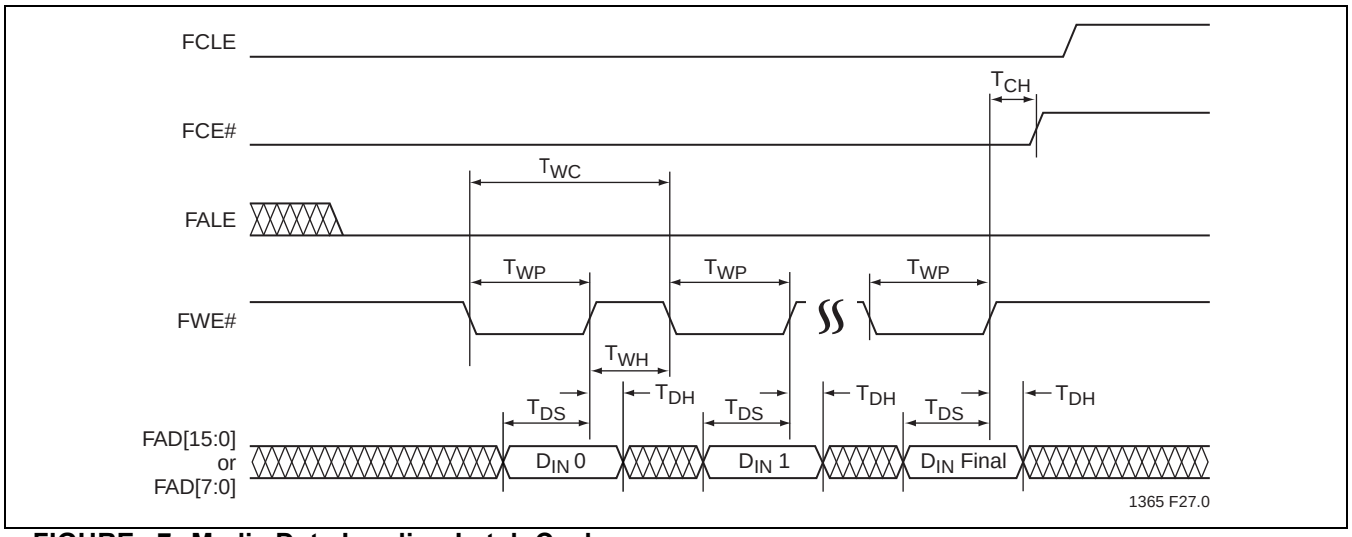


FIGURE 7: Media Data Loading Latch Cycle

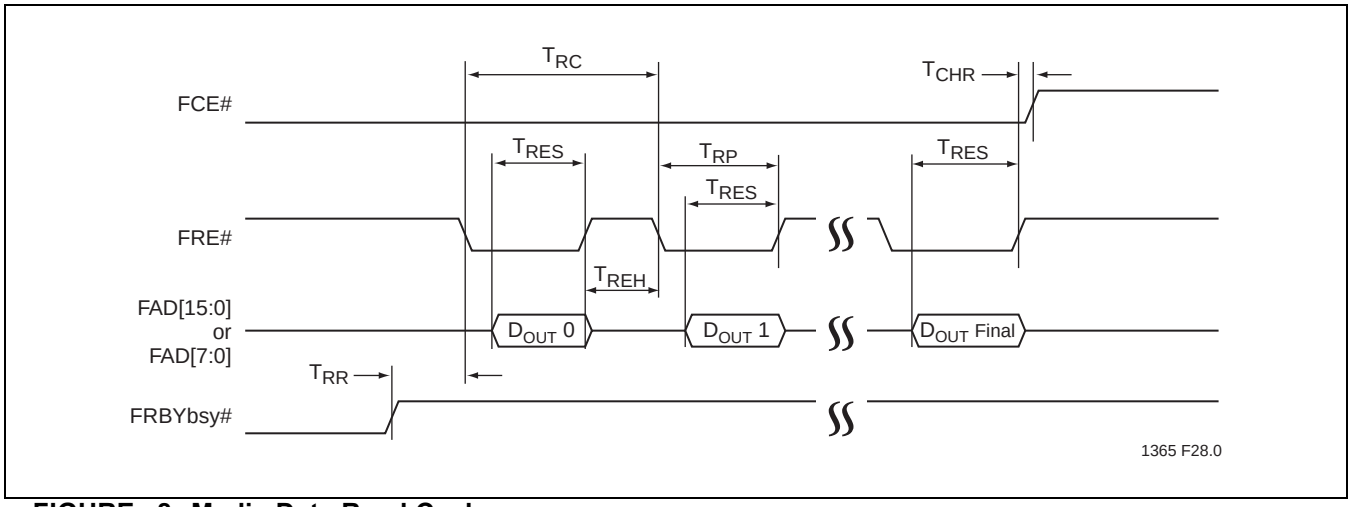


FIGURE 8: Media Data Read Cycle

APPENDIX

Differences between CF-ATA and PC Card- ATA/True IDE

This section details differences between CF-ATA vs. PC Card ATA and the differences between CF-ATA vs. True IDE.

Electrical Differences

TTL Compatibility CF is not TTL compatible, it is a purely CMOS interface. Refer to Section 2.3.2 of this specification.

Pull Up Resistor Input Leakage Current The minimum pull up resistor input leakage current is 50K ohms rather than the 10K ohms stated in the PCMCIA specification.

Functional Differences

Additional Set Features Codes in CF-ATA The following Set Features codes are not PC Card ATA or True IDE, but provide additional functionality in CF-ATA.

- 69H, Accepted for backward compatibility
- 96H, Accepted for backward compatibility
- 97H, Accepted for backward compatibility
- 9AH, Set the host current source capability

Additional Commands in CF-ATA The following commands are not standard PC Card ATA commands, but provide additional functionality in CF-ATA.

The command codes for the commands below are defined as vendor unique in PC Card ATA/True IDE.

- C0H, Erase-Sectors
- 87H, Translate-Sector

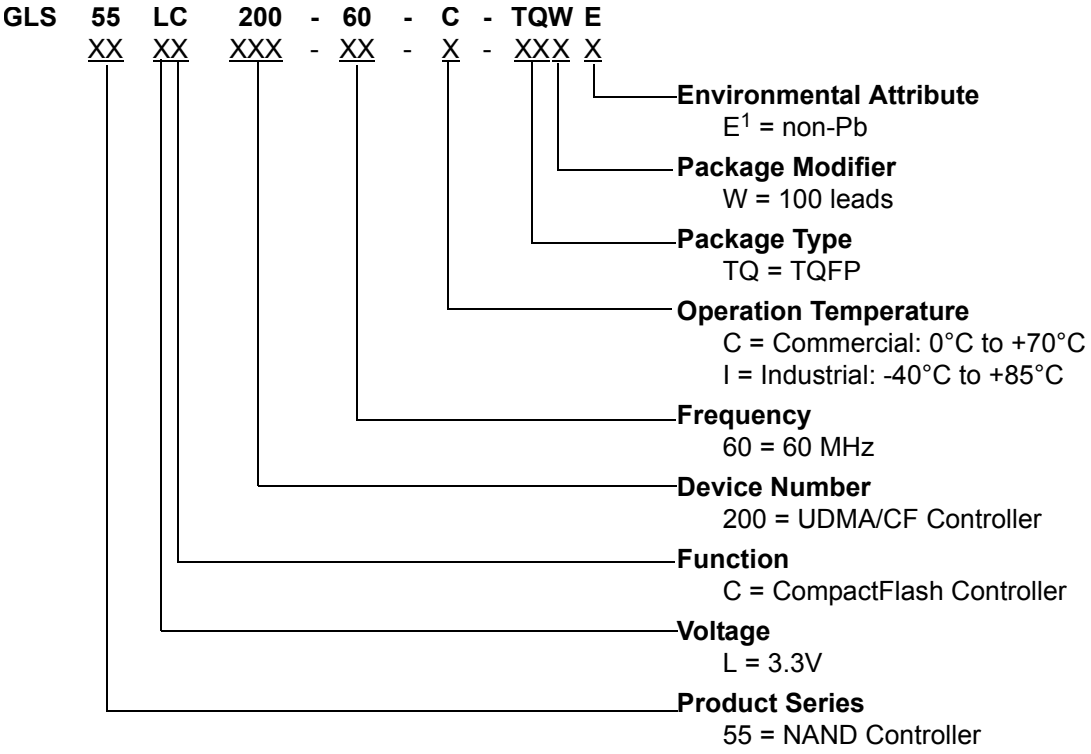
The command codes for the commands below are defined as reserved in PC Card ATA/True IDE:

- 03H, Request-Sense
- 38H, Write-Without-Erase
- CDH, Write-Multiple-Without-Erase

Idle Timer The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in PC Card ATA/True IDE.

Recovery from Sleep Mode For CF devices, recovery from sleep mode is accomplished by simply issuing another command to the device.
A hardware or software reset is not required.

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder. Greenliant non-Pb solder devices are “RoHS Compliant”.

Valid Combinations

Valid combinations for GLS55LC200

GLS55LC200-60-C-TQWE

GLS55LC200-60-I-TQWE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Data Sheet

PACKAGING DIAGRAM

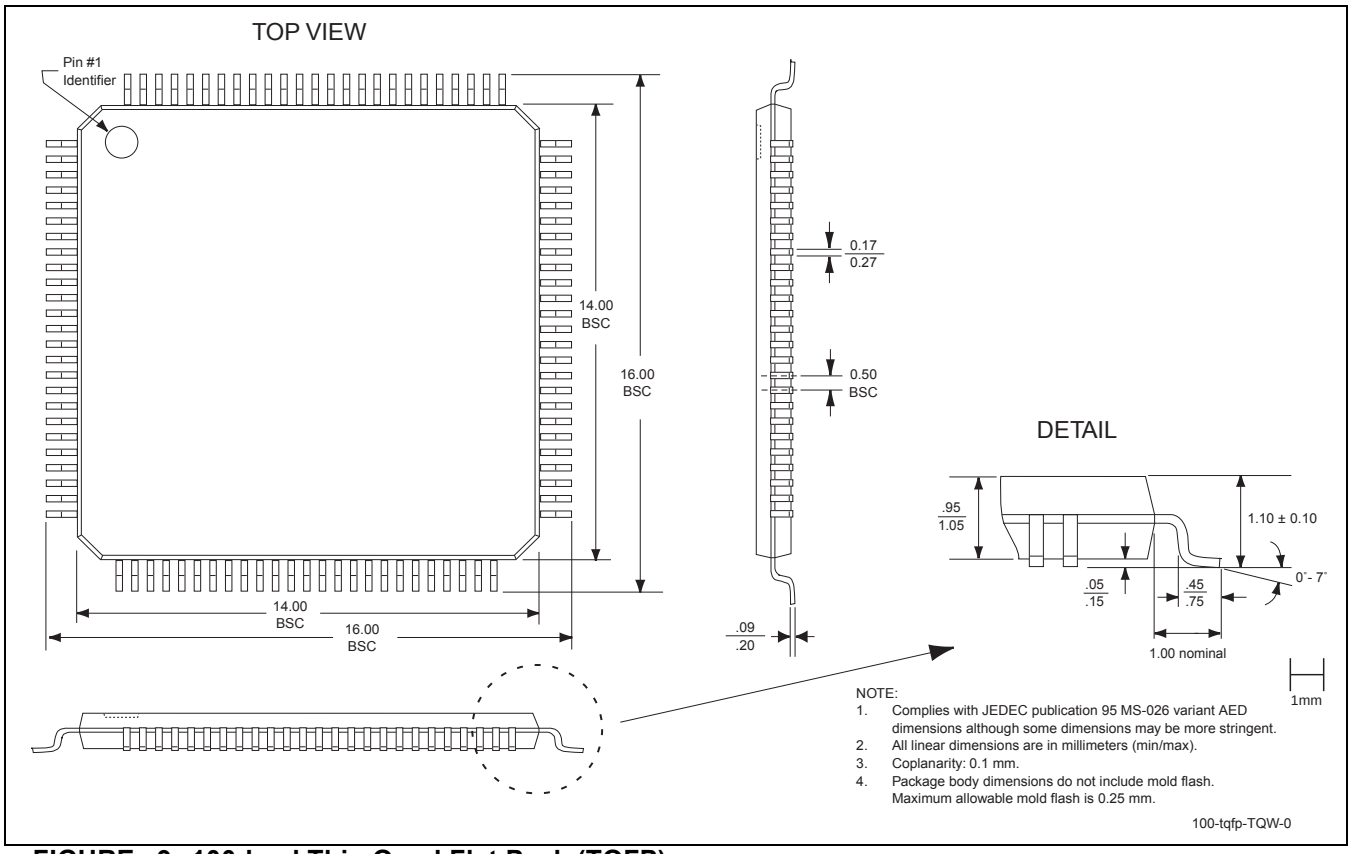


FIGURE 9: 100-lead Thin Quad Flat Pack (TQFP)
Greenliant Package Code: TQW

TABLE 34: Revision History

Number	Description	Date
00	• Initial Release of Data Sheet	Jan 2008
01	• Changed FWP# to DNU in Pin Assignment figure, page 8 and Pin Assignment table, page 13 • In Table 33, removed T_{CHR} and T_{RHZ}. Edited Min/Max values • Edited Figure 6 and Figure 8 • Deleted F5H, Wear-Level from 10.1.2.2 “Additional Commands in CF-ATA” on page 45 • Edited text in 6.0 “Power-on and brown-out Reset Characteristics” on page 13	May 2008
02	• Globally changed product name from CompactFlash Card Controller to NAND Controller	May 2009
03	• Transferred from SST to Greenliant	May 2010
04	• In Table 1 on page 10, added “Connect this pin with a 4.7uF capacitor to ground.” to VREG “External Capacitor Pin”.	Oct 2010

Data Sheet

PCMCIA STANDARD

CompactFlash memory cards are fully electrically compatible with the PCMCIA specifications listed below. These specifications may be obtained from:

PCMCIA
2635 North First St. Ste. 209
San Jose, CA 95131 USA

Phone: 408-433-2273
Fax: 408-433-9558

COMPACTFLASH SPECIFICATION

CompactFlash memory cards are fully compatible with the CompactFlash Specification published by the Compact-Flash Association. Contact the CompactFlash Association for more information.

CompactFlash Association
P.O. Box 51537
Palo Alto, CA 94303 USA