SIEMENS

3.3V 4M x 64-Bit SDRAM Module — HYS64V4000GU
3.3V 4M x 72-Bit SDRAM Module — HYS72V4000GU

168 pin unbuffered DIMM Modules

Preliminary Information

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual-In-Line SDRAM Module
- 1 bank 4M x 64, 4M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Performance:

		-10	-12	Units
f_{CK}	Clock frequency (max.)	100	83	MHz
t_{CK3}	Clock cycle time (min.)	10	12	ns
t_{AC3}	Clock access time (min.) $\overline{\text{CAS}}$ latency = 3	8	9	ns

- Single +3.3V($\pm$ 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes sixteen / eighteen 4M x 4 SDRAMs in TSOPII-44 packages
- 4096 refresh cycles every 64 ms
- Gold contact pad
- Card Size: 133,35mm x 31,75mm x 4,00 mm
- This SDRAM product familiy is intended to be fully pin and architecture compatible with the 168 pin Unbuffered DRAM DIMM module family.

The HYS64(72)V4000GU are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 4M x 64 and 4M x 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use eight 4M x 4 SDRAMs for the 4M x 64 organisation and an additional SDRAM for the 4M x 72 organisation. Decoupling capacitors are mounted on the PC board.

The DIMMs use optional serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYS 64V4000GU-10		L-DIM-168-17	100 Mhz 4M x 64 SDRAM module
HYS 64V4000GU-12		L-DIM-168-17	83 Mhz 4M x 64 SDRAM module
HYS 72V4000GU-10		L-DIM-168-17	100 MHz 4M x 72 SDRAM module
HYS 72V4000GU-12		L-DIM-168-17	83 Mhz 4M x 72 SDRAM module

Pin Names

A0-A10	Address Inputs (RA0 ~ RA10 / CA0 ~ CA9)
A11 (BS)	Bank Select
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bits (x72 organisation only)
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Read / Write Input
$\overline{\text{CKE0, CKE1}}$	Clock Enable
CLK0 - CLK3	Clock Input
DQMB0 - DQMB7	Data Mask
$\overline{\text{CS0, CS2}}$	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

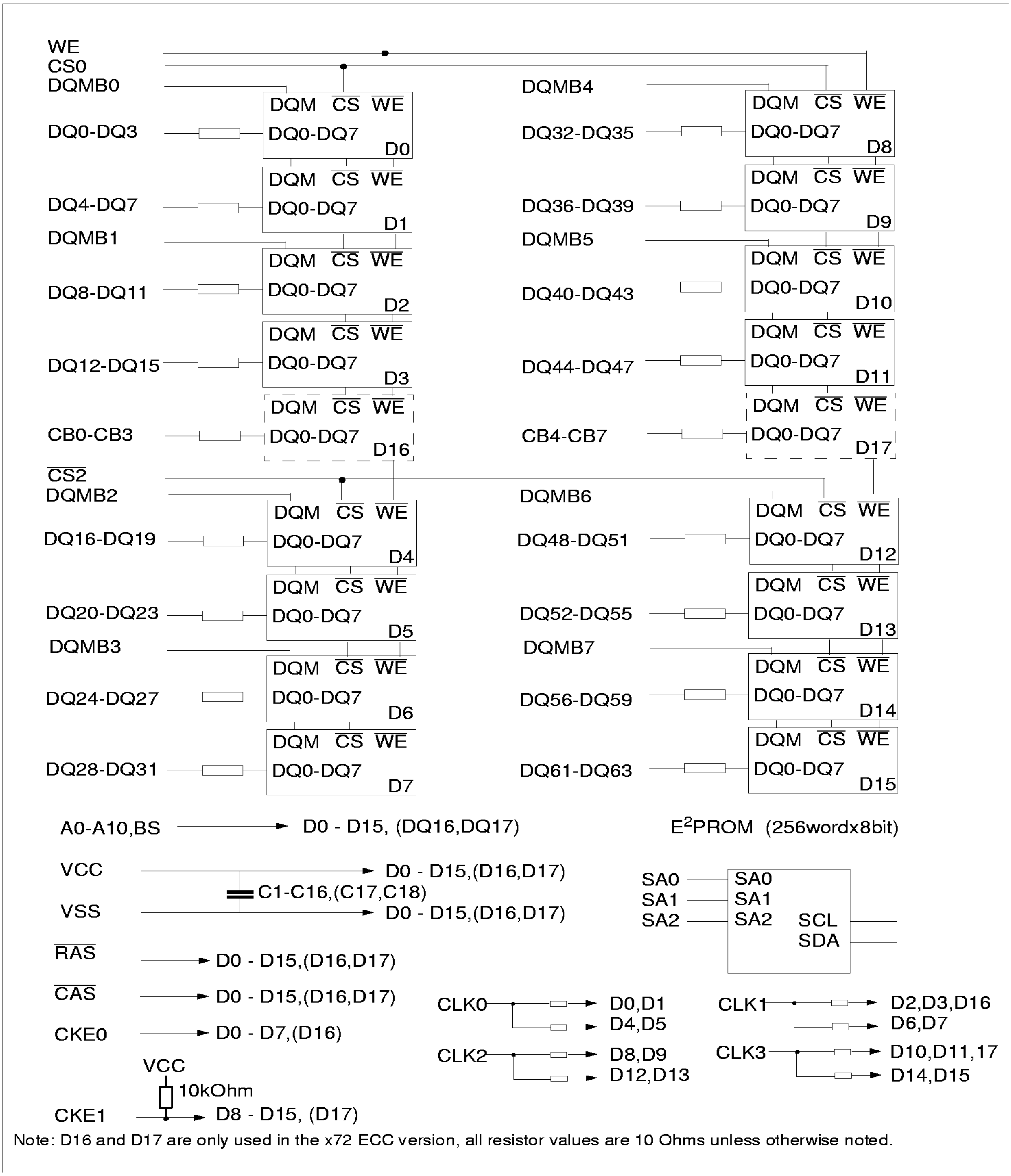
Address Format:

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
4M x 64	HYS 64V2000GS	11	10	1	4k	64 ms	15,6 µs
4M x 72	HYS 72V2000GS	11	10	1	4k	64 ms	15,6 µs

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	DU		86	DQ32	128	CKE0
3	DQ1	45	CS2		87	DQ33	129	NC
4	DQ2	46	DQMB2		88	DQ34	130	DQMB6
5	DQ3	47	DQMB3		89	DQ35	131	DQMB7
6	VCC	48	DU		90	VCC	132	NC
7	DQ4	49	VCC		91	DQ36	133	VCC
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	NC (CB2)		94	DQ39	136	CB6
11	DQ8	53	NC (CB3)		95	DQ40	137	CB7
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ16		97	DQ41	139	DQ48
14	DQ10	56	DQ17		98	DQ42	140	DQ49
15	DQ11	57	DQ18		99	DQ43	141	DQ50
16	DQ12	58	DQ19		100	DQ44	142	DQ51
17	DQ13	59	VCC		101	DQ45	143	VCC
18	VCC	60	DQ20		102	VCC	144	DQ52
19	DQ14	61	NC		103	DQ46	145	NC
20	DQ15	62	DU		104	DQ47	146	DU
21	NC (CB0)	63	CKE1		105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS		106	NC (CB5)	148	VSS
23	VSS	65	DQ21		107	VSS	149	DQ53
24	NC	66	DQ22		108	NC	150	DQ54
25	NC	67	DQ23		109	NC	151	DQ55
26	VCC	68	VSS		110	VCC	152	VSS
27	WE	69	DQ24		111	CAS	153	DQ56
28	DQMB0	70	DQ25		112	DQMB4	154	DQ57
29	DQMB1	71	DQ26		113	DQMB5	155	DQ58
30	CS0	72	DQ27		114	NC	156	DQ59
31	DU	73	VCC		115	RAS	157	VCC
32	VSS	74	DQ28		116	VSS	158	DQ60
33	A0	75	DQ29		117	A1	159	DQ61
34	A2	76	DQ30		118	A3	160	DQ62
35	A4	77	DQ31		119	A5	161	DQ63
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	CLK2		121	A9	163	CLK3
38	A10	80	NC		122	A11=BS	164	NC
39	NC	81	NC		123	NC	165	SA0
40	VCC	82	SDA		124	VCC	166	SA1
41	VCC	83	SCL		125	CLK1	167	SA2
42	CLK0	84	VCC		126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Block Diagram for 4M x 64/72 SDRAM DIMM modules

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 80	80	μA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 80	80	μA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min. (x64)	max. (x72)	
Input capacitance (A0 to A11)	C_{I1}	80	90	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}	80	90	pF
Input capacitance (CKE0, CKE1)	C_{I3}	45	55	pF
Input capacitance (CLK0 - CLK3, CS0, CS2)	C_{I4}	25	30	pF
Input capacitance (DQMB0 - DQMB7)	C_{I5}	10	15	pF
Input / Output capacitance (DQ0-DQ63,CB0-CB7)	C_{IO}	10	10	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	8	pF
Input/Output Capacitance	C_{sd}	10	10	pF

Standby and Refresh Currents (T_a = 0 to 70°C, VCC = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	Speed Sort	X64	X72		Note
Operating Current	Icc1	Burst length = 1, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation	-10 -12	2320 2000	2900 2500	mA mA	1,2
Operating Current	Icc1	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), Io=0 mA 2 bank interleave operation	-10 -12	2320 2000	2900 2000	mA mA	1,2
Precharged Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)		48	60	mA	
	Icc2PS	CKE<=VIL(max), tck=infinite		32	40	mA	
Precharged Standby Current in Non-power Down Mode	Icc2N	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles		480	600	mA	$\overline{CS}$= High
	Icc2NS	CKE>=VIH(min), tck=infinite, no input change		240	300	mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)		48	60	mA	
	Icc3PS	CKE<=VIL(max), tck=infinite		32	40	mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck (min.) input changed one time		560	700	mA	$\overline{CS}$= High
	Icc3NS	CKE=>VIH(min),tck=infinite, no input change		320	400	mA	
Burst Operating Current	Icc4	Burst length = full page, trc = infinite, CL = 3, tck>=tck (min.), Io = 0 mA 2 banks activated	-10 -12	2160 1920	2700 2400	mA mA	1,2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)	-10 -12	2000 1720	2500 2200	mA mA	1,2
Self Refresh Current	Icc6	CKE=<0,2V		32	40	mA	1,2

AC Characteristics 3)4)
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-10		-12			
		min	max	min	max		
Clock and Clock Enable							
Clock Cycle Time	t_{CK}						
$\overline{CAS}$ Latency = 3		10		12		ns	
$\overline{CAS}$ Latency = 2		15		18		ns	
$\overline{CAS}$ Latency = 1		30		36		ns	
System Frequency	f_{CK}						
$\overline{CAS}$ Latency = 3		–	100	–	83	MHz	
$\overline{CAS}$ Latency = 2		–	66	–	55	MHz	
$\overline{CAS}$ Latency = 1		–	33	–	27	MHz	
Clock Access Time	t_{AC}						
$\overline{CAS}$ Latency = 3		–	8	–	9	ns	
$\overline{CAS}$ Latency = 2		–	9	–	10	ns	
$\overline{CAS}$ Latency = 1		–	27	–	27	ns	
Clock High Pulse Width	t_{CH}	3.5	–	4	–	ns	
Clock Low Pulse Width	t_{CL}	3.5	–	4	–	ns	
CKE Setup Time	t_{CKS}	3	–	3.5	–	ns	
CKE Hold Time	t_{CKH}	1	–	1.5	–	ns	
CKE Setup Time (Power down mode)	t_{CKSP}	3	–	3.5	–	ns	
Transition time (rise and fall)	t_T	1	30	1	30	ns	
Common Parameters							
Command Setup time	t_{CS}	3	–	3	–	ns	
Command Hold Time	t_{CH}	1	–	1.5	–	ns	
Address Setup Time	t_{AS}	3	–	3	–	ns	
Address Hold Time	t_{AH}	1	–	1.5	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	30	–	30	–	ns	
Cycle Time	t_{RC}	75	120k	96	120k	ns	
Active Command Period	t_{RAS}	45	120k	60	120k	ns	
Precharge Time	t_{RP}	30	–	36	–	ns	
Bank to Bank Delay Time	t_{RRD}	20	–	24	–	ns	
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	1	–	CLK	

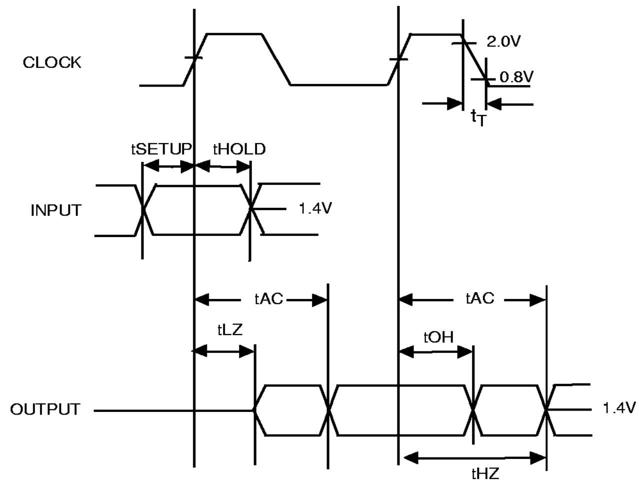
Parameter	Symbol	Limit Values				Unit	Note
		-10		-12			
		min	max	min	max		
Refresh Cycle							
Self Refresh Exit Time	t_{SREX}	2CLK $+t_{RC}$	–	2CLK $+t_{RC}$	–	ns	6
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	ms	5
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}						7
$\overline{CAS}$ Latency = 3		–	6	–	8	ns	
$\overline{CAS}$ Latency = 2		–	8	–	11	ns	
$\overline{CAS}$ Latency = 1		–	25	–	25	ns	
DQM Data Out Disable Latency	t_{DQZ}	2	–	2	–	CLK	
Write Cycle							
Data In Setup Time	t_{DS}	3	–	3	–	ns	
Data In Hold Time	t_{DH}	1	–	1.5	–	ns	
Data input to Precharge	t_{DPL}	2	–	2	–	CLK	
Data In to Active/refresh	t_{DAL}	5	–	5	–	CLK	8
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

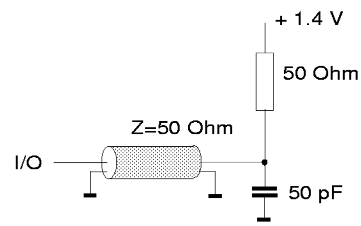
Clock Frequency and Latency

Parameter		Symbol	Speed Sort				Unit
			-10		-12		
Clock Frequency	max.	t_{CK}	**100**	**66**	**83**	**66**	MHz
Clock Cycle Time	min.	t_{CK}	10	15	12	15	ns
$\overline{CAS}$ Latency	min.	t_{AA}	3	2	3	3	CLK
RAS to CAS Delay	min.	t_{RCD}	3	2	3	2	CLK
RAS Latency	min.	t_{RL}	6	4	6	5	CLK
Bank Cycle time	min.	t_{RC}	8	5	8	7	CLK
Bank Active Cycle Time	min.	t_{RAS}	5	3	5	4	CLK
Bank Active Cycle Time	max.	t_{RAS}	120	120	120	120	µs
Precharge Time	min.	t_{RP}	3	2	3	3	CLK
Data In to Precharge	min.	t_{DPL}	2	1	2	2	CLK
Data In to Active / Refresh	min.	t_{DAL}	5	3	5	5	CLK
Bank to Bank Delay Time	min.	t_{RRD}	2	2	2	2	CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time	min.	t_{CCD}	1	1	1	1	CLK
Write Latency	fixed	t_{WL}	0	0	0	0	CLK
DQM Write Mask Latency	fixed	t_{DQW}	0	0	0	0	CLK
DQM Data Disable Latency	fixed	t_{DQZ}	2	2	2	2	CLK
Clock Suspend Latency	fixed	t_{CSL}	1	1	1	1	CLK

Notes:

1. The specified values are valid when addresses are changed no more than once during tck(min.) and when No Operation commands are registered on every rising clock edge during tRC(min).
2. The specified values are valid when data inputs (DQ's) are stable during tRC(min.).
3. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{il} = 0.8V and V_{ih} = 2.0V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown.





5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to "wake-up" the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
8. t_{DAL} is equivalent to t_{DPL} + t_{RP}.

A serial presence detect storage device - E^2PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

SPD-Table:)

Byte#	Description	SPD Entry Value	Hex			
			x64 -10	x64 -12	x72 -10	x72 -12
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11	0B	0B	0B	0B
4	Number of Column Addresses (for x4 SDRAM)	10	0A	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	64 / 72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0/ 12.0 ns	A0	C0	A0	C0
10	SDRAM Access time from Clock at CL=3	8.0 / 9.0 ns	80	90	80	90
11	Dimm Config (Error Det/Corr.)	none / ECC	00	00	02	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x4	04	04	04	04
14	Error Checking SDRAM data width	n/a / x4	00	00	04	04
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	02	02	02
18	Supported CAS Latencies	$\overline{\text{CAS}}$ latency = 1, 2 & 3	07	07	07	07
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Minimum Clock Cycle Time at CAS Latency = 2	15.0 / 18.0 ns	F0	30	F0	30
24	Maximum data access time from Clock for CL=2	9.0 / 10.0 ns	90	A0	90	A0
25	Minimum Clock Cycle Time at CL = 1	30 / 36 ns	78	90	78	90
26	Maximum Data Access Time from Clock at CL=1	27 ns	6C	6C	6C	6C
27	Minimum Row Precharge Time	30 / 36 ns	1E	24	1E	24
28	Minimum Row Active to Row Active delay tRRD	20 / 24 ns	14	18	14	18
29	Minimum RAS to CAS delay tRCD	30 ns	1E	1E	1E	1E
30	Minimum Ras pulse width tRAS	45 / 60 ns	2D	3C	2D	3C
31	Module Bank Density (per bank)	32 MByte	08	08	08	08
32-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1	01	01	01	01
63	Checksum for bytes 0 - 62		F4	A5	02	B3
64-127	Manufactures's information (optional) (FFh if not used)		FF	FF	FF	FF
128+	Unused storage locations		FF	FF	FF	FF

L-DIM-168-17
SDRAM DIMM Module package