3.3 V 168-pin Registered SDRAM Modules

PC133 128 MByte Module
PC133 256 MByte module
PC133 512 MByte Module
PC133 1 GByte Module

- 168-pin Registered 8 Byte Dual-In-Line SDRAM Module for PC and Server main memory applications
- One bank 16M × 72, 32M x 72 and 64M × 72 two bank 128M × 72 organization
- Optimized for ECC applications with very low input capacitances
- JEDEC standard Synchronous DRAMs (SDRAM) Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Single + 3.3 V (± 0.3 V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes SDRAMs in TSOPII-54 packages with registers and PLL.
- Card Size: 133.35 mm × 43.18 mm × 3.99/ 8.13 mm with Gold contact pads
- These modules all fully compatible with the current PC133 and INTELs PC100 specifications
- Performance:

		-7.5	Unit
f_{CK}	Clock Frequency (max.) @ CL = 3	133	MHz
t_{CK}	Clock Cycle Time (min.) @ CL = 3	7.5	ns
t_{AC}	Clock Access Time (min.) $\overline{\text{CAS}}$ Latency = 3	5.4	ns

The HYS 72Vxx3xxGR-7.5 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 16M × 72, 32M x 72, 64M × 72 and 128M × 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for ECC applications. The 32M x 72 (256Mbyte) registered DIMM module is available in two versions (12 or 13 row addresses). All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board. The DIMMs use a serial presence detects scheme implemented via a serial E^2PROM using the 2-pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
HYS 72V16300GR-7.5	PC133R-333-542-B2	one bank 128 MB Reg. DIMM	64 MBit
HYS 72V16301GR-7.5	PC133R-333-542-B2	one bank 128 MB Reg. DIMM	128 MBit
HYS 72V32301GR-7.5	PC133R-333-542-B2	one bank 256 MB Reg. DIMM	128 Mbit
HYS 72V32300GR-7.5	PC133R-333-542-AA	one bank 256 MB Reg. DIMM	256 Mbit
HYS 72V64300GR-7.5	PC133R-333-542-B2	one bank 512 MB Reg. DIMM	256 MBit
HYS 72V128320GR-7.5	PC133R-333-542-B2	two banks 1 GByte Reg. DIMM	256 MBit (stacked)

Note: HYS 72V32301GR-7.5*All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS 64V16300GR-7.5-C, indicating Rev.C dies are used for SDRAM components.*

Pin Definitions and Functions

A0 - A11, A12	Address Inputs (A12 is used for 256Mbit based modules only)	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	$\overline{CS0}$ - $\overline{CS3}$	Chip Select
DQ0 - DQ63	Data Input/Output	REGE	Register Enable
CB0 - CB7	Check Bits	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out
CKE0	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input	–	–

Address Format

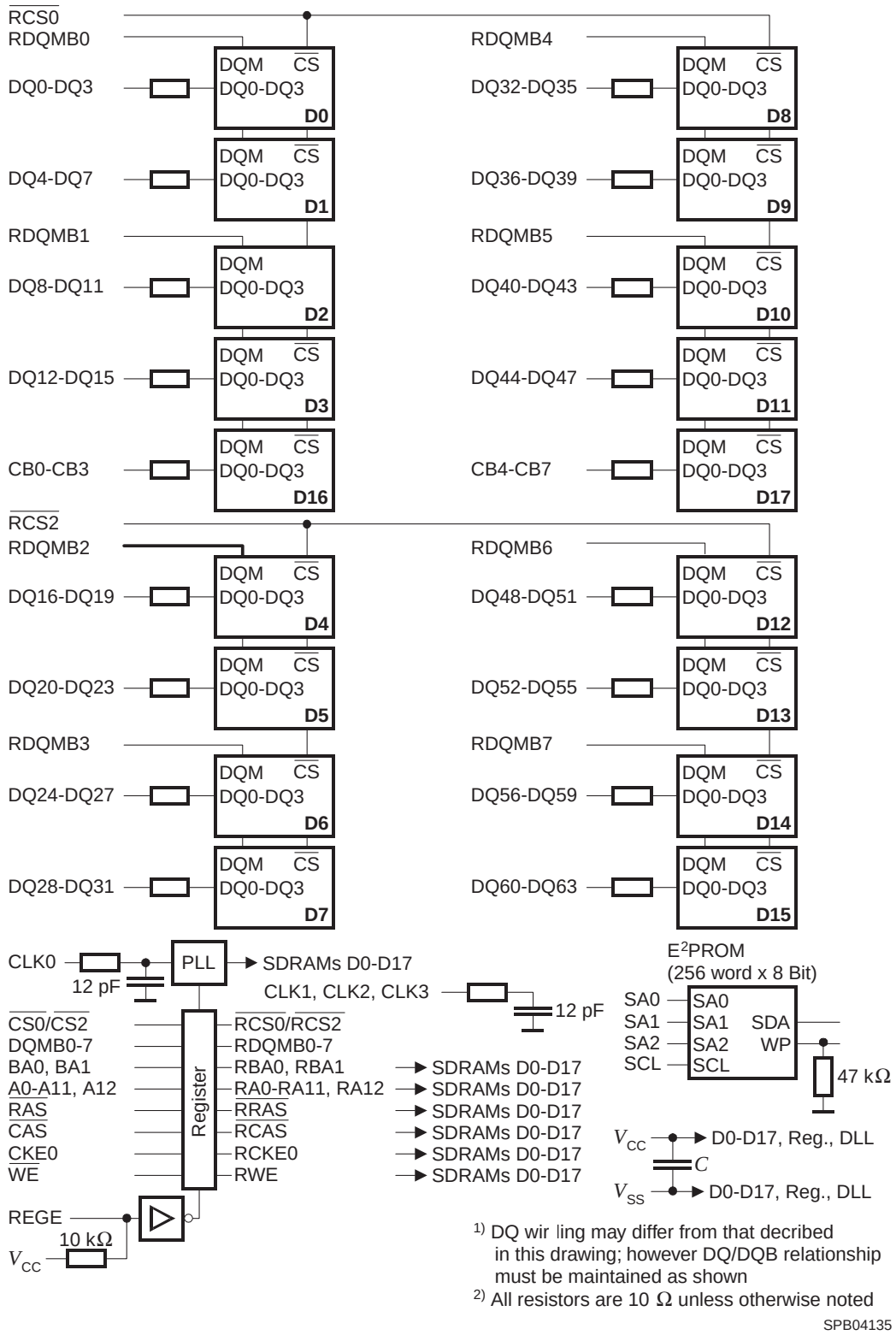
Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128 MB	16M × 72	1	16M × 4	18	12/2/10	4k	64 ms	15.6 µs
128 MB	16M × 72	1	16M x 8	9	12/2/10	4k	64 ms	15.6 µs
256 MB	32M x 72	1	32M x 4	18	12/2/11	4k	64 ms	15.6 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	1	64M × 4	18	13/2/11	8k	64 ms	7.8 µs
1 GB	128M × 72	2	64M × 4	36	13/2/11	8k	64 ms	7.8 µs

Pin Configuration

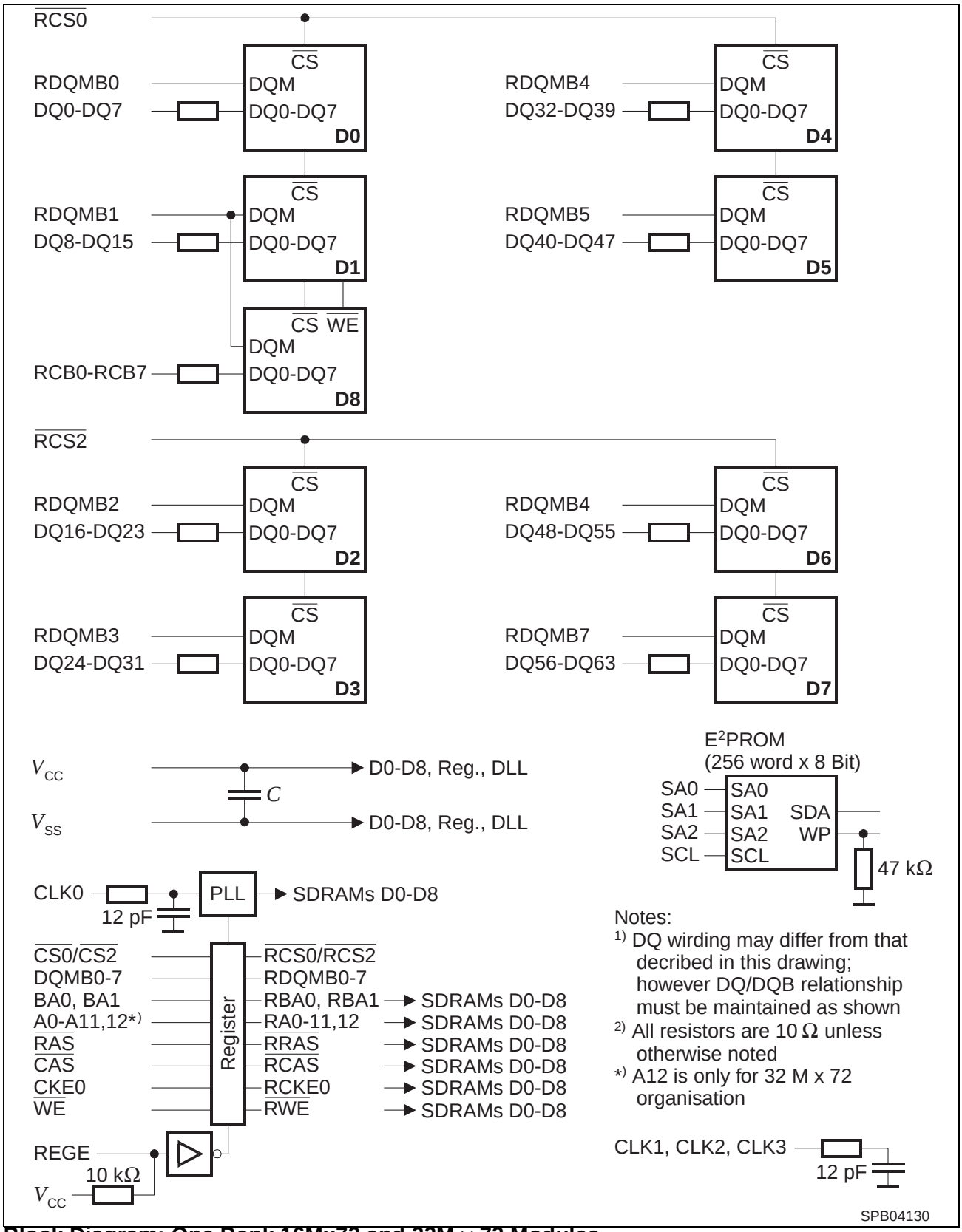
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	$\overline{CS2}$	87	DQ33	129	$\overline{CS3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DU	90	V_{DD}	132	N.C.
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	N.C.	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{CS0}$	72	DQ27	114	$\overline{CS1}$	156	DQ59
31	DU	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61

Pin Configuration (cont'd)

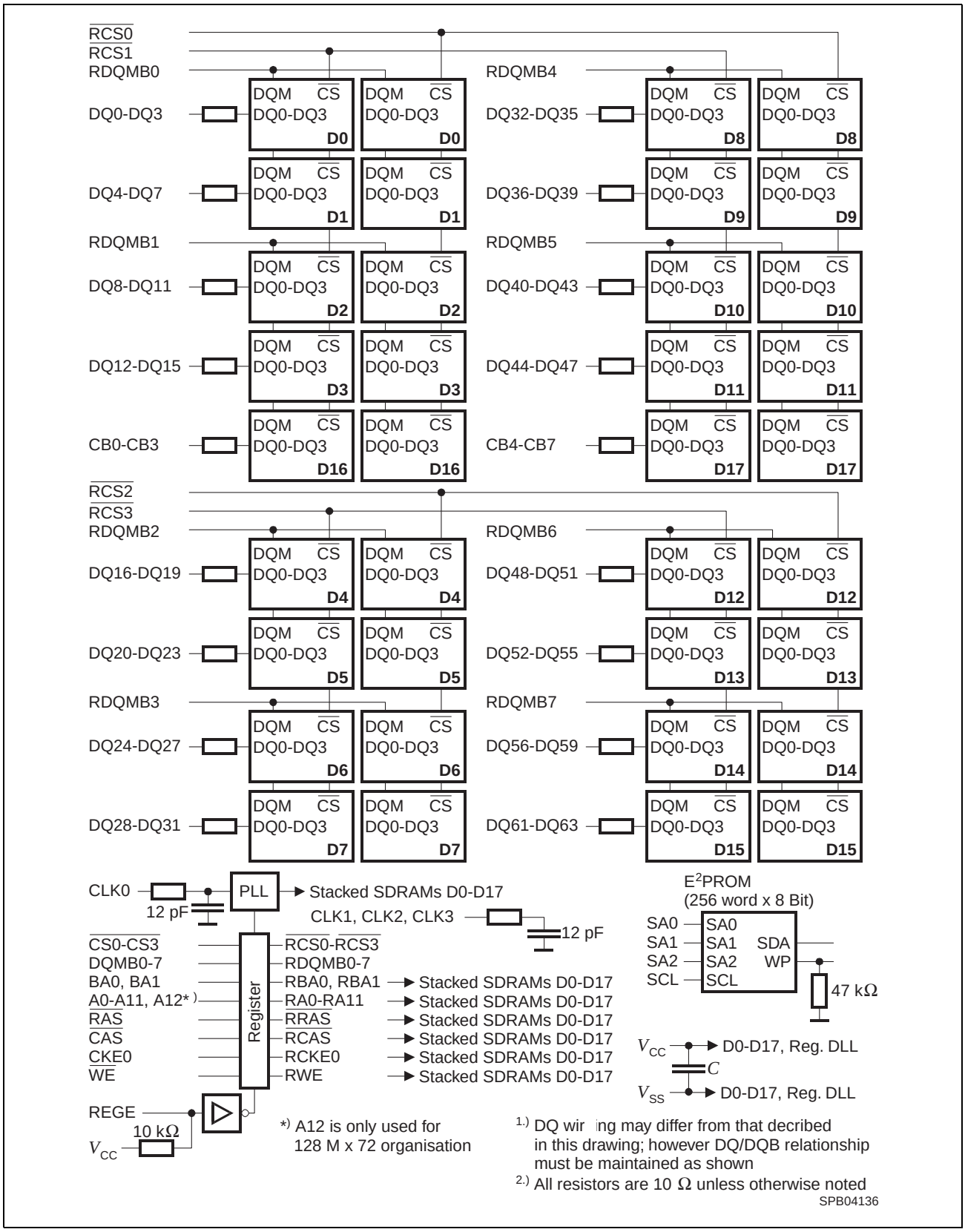
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{DD}	126	A12	168	V_{DD}



Block Diagram: One Bank 16M × 72, 32M × 72 and 64M × 72 SDRAM DIMM Modules HYS72V16300GR, HYS72V32301GR and HYS 72V64300GR using x4 organized SDRAMs



Block Diagram: One Bank 16Mx72 and 32M × 72 Modules
HYS72V16301 & HYS72V32300GR using x8 organized SDRAMs



Block Diagram: Two Bank 128M × 72 SDRAM DIMM Modules
HYS 72V128320GR Using Stacked x4 Organized SDRAMs

DC Characteristics

T_A = 0 to 70 °C [1]; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 10	10	µA

Capacitance

T_A = 0 to 70 °C [1]; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values (max.)		Unit
		One Bank modules	Two Bank Modules	
Input Capacitance (all inputs except CLK and CKE)	C_{IN}	10	20	pF
Input Capacitance (CLK)	C_{CLK}	30	30	pF
Input Capacitance (CKE)	C_{CKE}	17	30	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	17	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	8	8	pF

Operating Currents per SDRAM Component
T_A = 0 to 70 °C [1], V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter	Test Condition	Symbol	64 Mb	128 Mb	256 Mb	Unit	Note
			max.				
Operating current t_{RC} = $t_{RC(MIN.)}$, t_{CK} = $t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1} x4	100	120	270	mA	2)
Precharge stand-by current in Power Down Mode $\overline{CS}$ = $V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	2	2	2	mA	2)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS}$ = $V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	35	40	35	mA	2)
No operating current t_{CK} = min., $\overline{CS}$ = $V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	45	50	50	mA	2)
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	8	10	10	mA	2)
Burst operating current t_{CK} = min., Read command cycling	–	I_{CC4} x4	60	120	270	mA	2), 3)
Auto refresh current t_{CK} = min., Auto Refresh command cycling	–	I_{CC5}	130	180	240	mA	2)
Self refresh current Self Refresh Mode, CKE = 0.2 V	–	I_{CC6}	1	1.5	2.5	mA	2)

AC Characteristics (SDRAM Device Specification) [4), 5)]
T_A = 0 to 70 °C [1)]; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

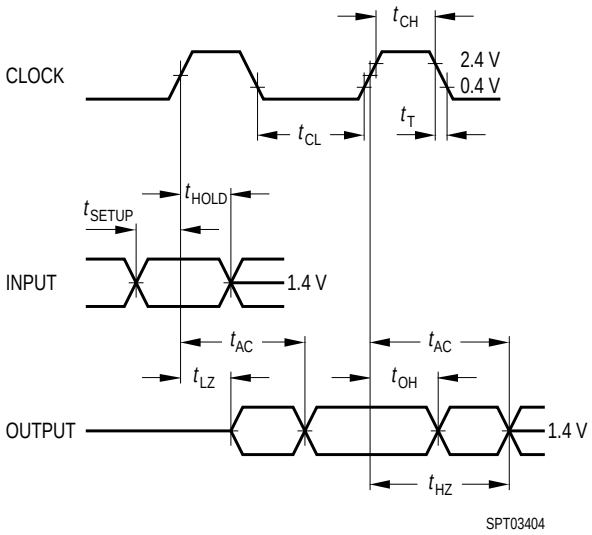
Parameter	Symbol	Limit Values		Unit	Note
		-7.5			
		min.	max.		
Clock and Access Time					
Clock Cycle Time	t_{CK}				–
$\overline{CAS}$ Latency = 3		7.5	–	ns	
$\overline{CAS}$ Latency = 2 (64Mb & 128Mb based mod.)		10	–	ns	
$\overline{CAS}$ Latency = 2 (256Mb based modules)		12	–	ns	
Clock Frequency	f_{CK}				–
$\overline{CAS}$ Latency = 3		–	133	MHz	
$\overline{CAS}$ Latency = 2 (64Mb & 128Mb based mod.)		–	100	MHz	
$\overline{CAS}$ Latency = 2 (256Mb based modules)		–	83	MHz	
Access Time from Clock	t_{AC}				–
$\overline{CAS}$ Latency = 3		–	5.4	ns	
$\overline{CAS}$ Latency = 2		–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	ns	–
Clock Low Pulse Width	t_{CL}	2.5	–	ns	–
Transition Time	t_T	0.5	10	ns	–
Setup and Hold Parameters					
Input Setup Time	t_{IS}	1.5	–	ns	–
Input Hold Time	t_{IH}	0.8	–	ns	–
Power Down Mode Entry Time	t_{SB}	–	1	CLK	–
Power Down Mode Exit Setup Time	t_{PDE}	1	–	CLK	–
Mode Register Setup Time	t_{RCS}	2	–	CLK	–
Common Parameters					
Row to Column Delay Time	t_{RCD}	20	–	ns	–
Row Precharge Time	t_{RP}	20	–	ns	–
Row Active Time	t_{RAS}	45	100k	ns	–
Row Cycle Time	t_{RC}	67.5	–	ns	–
Activate (a) to Activate (b) Command Period	t_{RRD}	2	–	CLK	–
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	CLK	–

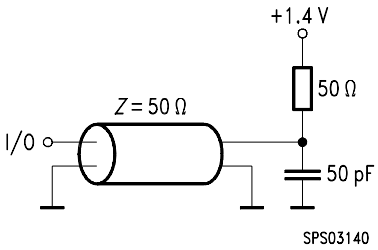
AC Characteristics (SDRAM Device Specification) (cont'd) [4), 5)]
T_A = 0 to 70 °C [1)]; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

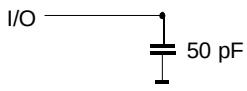
Parameter	Symbol	Limit Values		Unit	Note
		-7.5			
		min.	max.		
Refresh Cycle					
Refresh Period 64&128MBit SDRAM Based Modules 256 MBit SDRAM Based Modules	t_{REF}	 – –	 15.6 7.8	 µs µs	–
Self Refresh Exit Time	t_{SREX}	1	–	CLK	[6)]
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	–
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	[7)]
Data Out to High Impedance Time	t_{HZ}	3	7	ns	[7)]
DQM Data Out Disable Latency	t_{DQZ}	–	2	CLK	–
Write Cycle					
Data Input to Precharge (write recovery)	t_{WR}	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	CLK	–

Notes

1. The registered DIMM modules are designed to operate under system operating conditions between 0-55 deg C ambient, maximum sustained bandwidth and 0 LFM airflow.
2. These parameters depend on the cycle rate. All values are measured at 133 MHz operation frequency. Input signals are changed once during tck excepts for Icc6 and for standby currents when tck = infinity.
3. These parameters are measured with continous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the Vcc current is excluded.
4. An initial pause of 100 µs is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.
5. AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
6. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
7. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.







Measurement conditions for t_{AC} and t_{OH}

A serial presence detect storage device - E^{2}PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^{2}PROM device during module production using a serial presence detect protocol (I^{2}C synchronous 2-wire bus).

SPD-Table for -7.5 Registered DIMM Modules with PLL

Byte#	Description	SPD Entry Value	Hex					
			128 MB 1 Bank 1)	128 MB 1 Bank 2)	256 MB 1 Bank*)	256 MB 1 Bank**)	512 MB 1 Bank	1 GB 2 Banks
0	Number of SPD Bytes	128	80					
1	Total Bytes in Serial PD	256	08					
2	Memory Type	SDRAM	04					
3	Number of Row Addresses (without BS bits)	12/13	0C	0C	0C	0D	0D	0D
4	Number of Column Addresses	10/11	0A	0A	0B	0A	0B	0B
5	Number of DIMM Banks	1/2	01	01	01	01	01	02
6	Module Data Width	72	48					
7	Module Data Width (cont'd)	0	00					
8	Module Interface Levels	LVTTL	01					
9	Cycle Time at CL = 3	7.5 ns	75					
10	Access Time from Clock at CL = 3	5.4 ns	54					
11	DIMM Config (Error Det/Corr.)	ECC	02					
12	Refresh Rate/Type	15.6/7.8 µs	80	80	80	82	82	82
13	SDRAM Width, Primary	x4 / x8	04	08	04	08	04	04
14	Error Checking SDRAM Data Width	x4 / x8	04	08	04	08	04	04
15	Minimum t_{CCD}	1 CLK	01					
16	Burst Length Supported	1, 2, 4, 8 & (full page)	8F	0F	0F	0F	0F	0F
17	Number of SDRAM Banks	4	04					
18	SDRAM Supported $\overline{CAS}$ Latencies	2 & 3	06					
19	SDRAM $\overline{CS}$ Latencies	0	01					
20	SDRAM $\overline{WE}$ Latencies	0	01					
21	SDRAM DIMM Module Attributes	with PLL	1F					
22	SDRAM Device Attributes	V_{DD} tol +/– 10%	0E					
23	Min. Clock Cycle Time at CL = 2	10/12 ns	A0	A0	A0	C0	C0	C0
24	Max. Data Access Time from Clock for CL = 2	6.0	60	60	60	60	60	60
25	Min. Clock Cycle Time at CL = 1	not supported	00					
26	Max. Data Access Time from Clock at CL = 1	not supp.	00					

SPD-Table for -7.5 Registered DIMM Modules with PLL (cont'd)

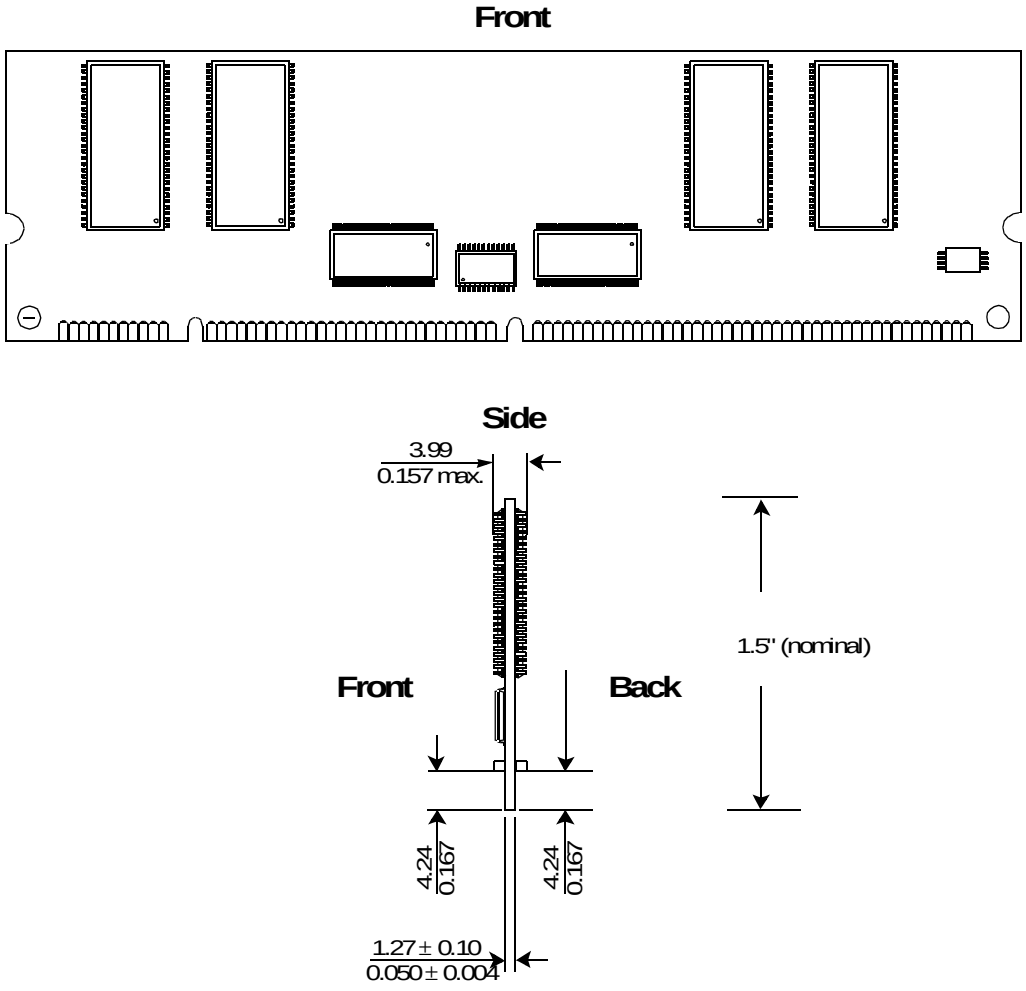
Byte#	Description	SPD Entry Value	Hex					
			128 MB 1 Bank 1)	128 MB 1 Bank 2)	256 MB 1 Bank*)	256 MB 1 Bank**)	512 MB 1 Bank	1 GB 2 Banks
27	SDRAM Minimum t_{RP}	20 ns	14					
28	SDRAM Minimum t_{RRD}	15 ns	0F					
29	SDRAM Minimum t_{RCD}	20 ns	14					
30	SDRAM Minimum t_{RAS}	45 ns	2D					
31	Module Bank Density (per bank)	128 MByte/ 256 Mbyte 512 MByte	20	20	40	40	80	80
32	SDRAM Input Setup Time	1.5 ns	15					
33	SDRAM Input Hold Time	0.8 ns	08					
34	SDRAM Data Input Setup Time	1.5 ns	15					
35	SDRAM Data Input Hold Time	0.8 ns	08					
36-61	Superset Information (may be used in future)	–	00					
62	SPD Revision	JEDEC 2	02					
63	Checksum for Bytes 0 - 62	–	C8	50	69	93	CC	CD
64-125	Manufacturer's Information	–						
126	Frequency Specification	–	64					
127	Details of Clocks	–	8F	8F	8F	8D	8D	8D
128+	Unused Storage Locations	–	FF	FF	FF	FF	FF	FF

1) HYS72V16300GR-7.5
2) HYS72V16301GR-7.5
*) HYS72V32301GR-7.5
**) HYS72V32300GR-7.5

Package Outlines

Module Package
JEDEC MO-161
Registered DIMM Modules Raw Card AA L-DIM168-44

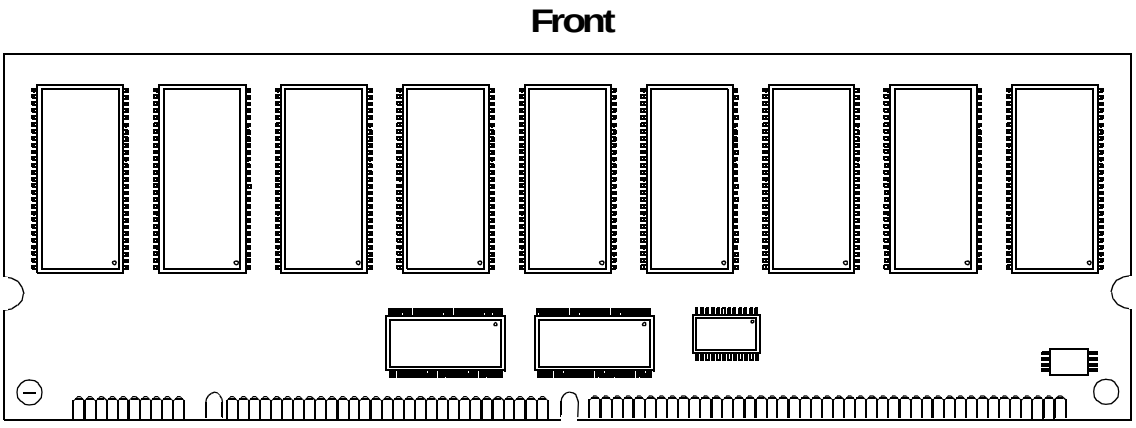
256MB modules

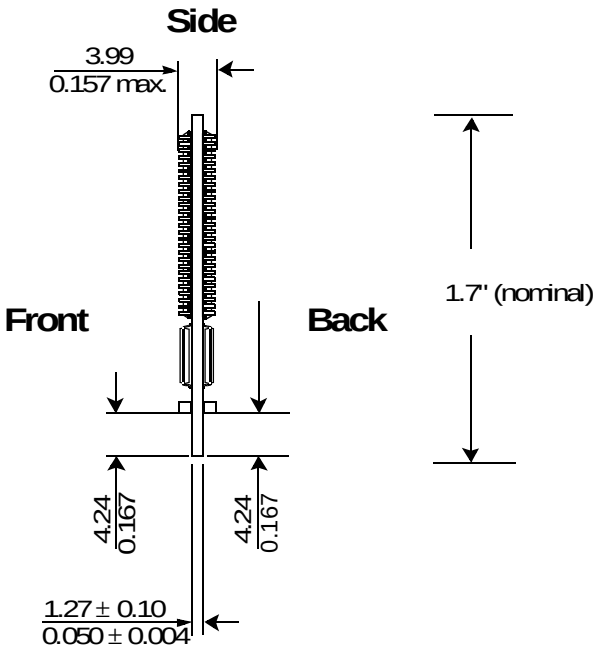


Package Outlines

Module Package
JEDEC MO-161
Registered DIMM Modules Raw Card B L-DIM168-37-2

128MB, 256MB & 512MB modules

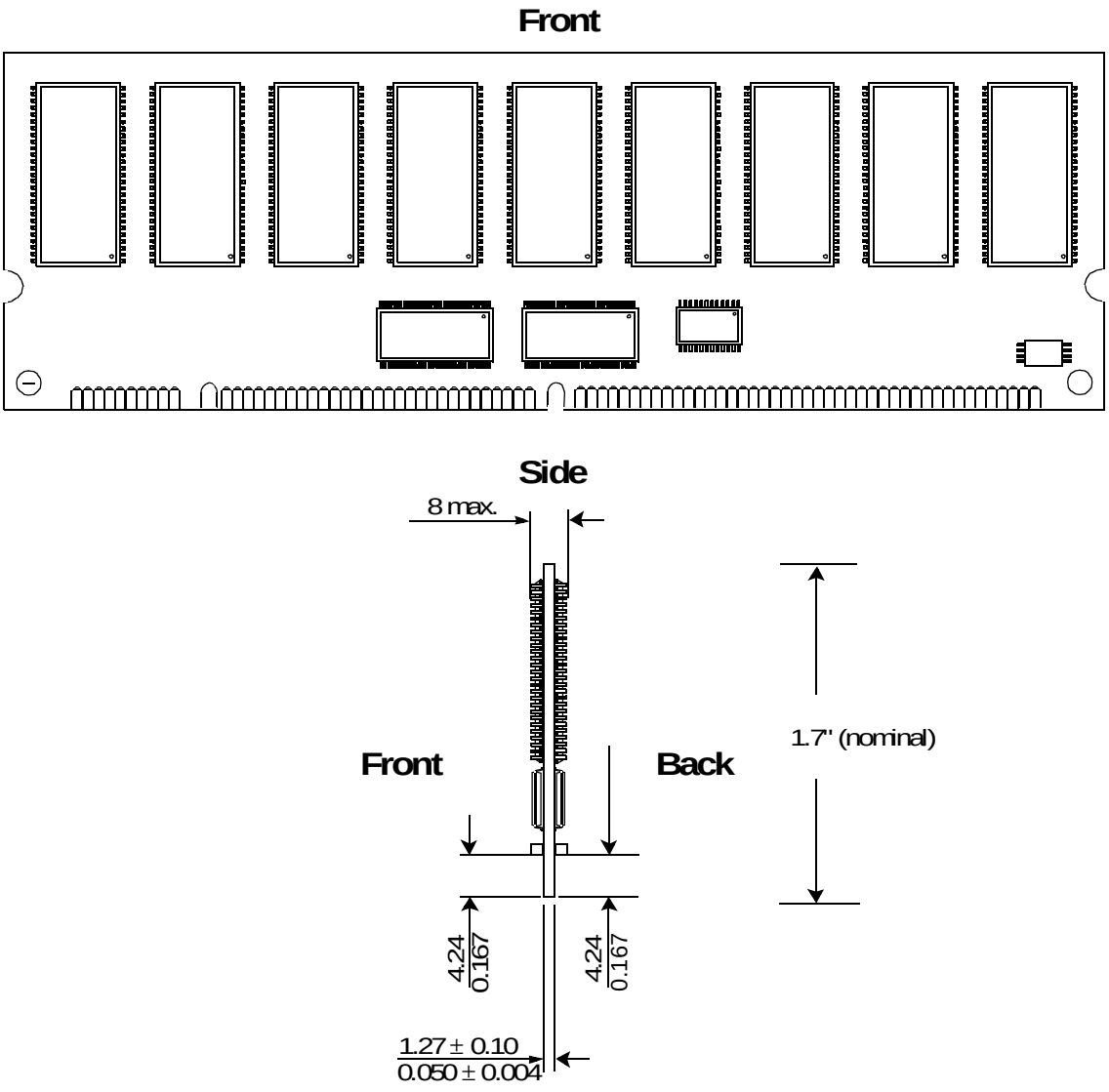




Package Outlines

Module Package
JEDEC MO-161
Registered DIMM Modules Raw Card B L-DIM168-37-2

1 GByte module



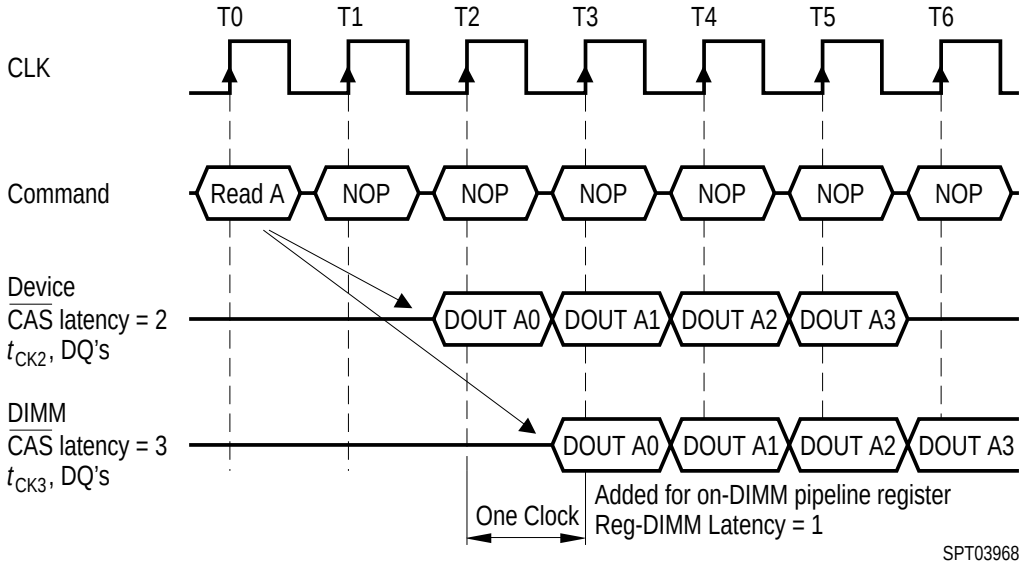
Functional Description

All these PC133 168-pin Registered DIMMs conform to a compatible set of timing and operation characteristics intended to comply with the 133 MHz standards. The Registered DIMMs achieve high speed data transfer rate up to 133 MHz.

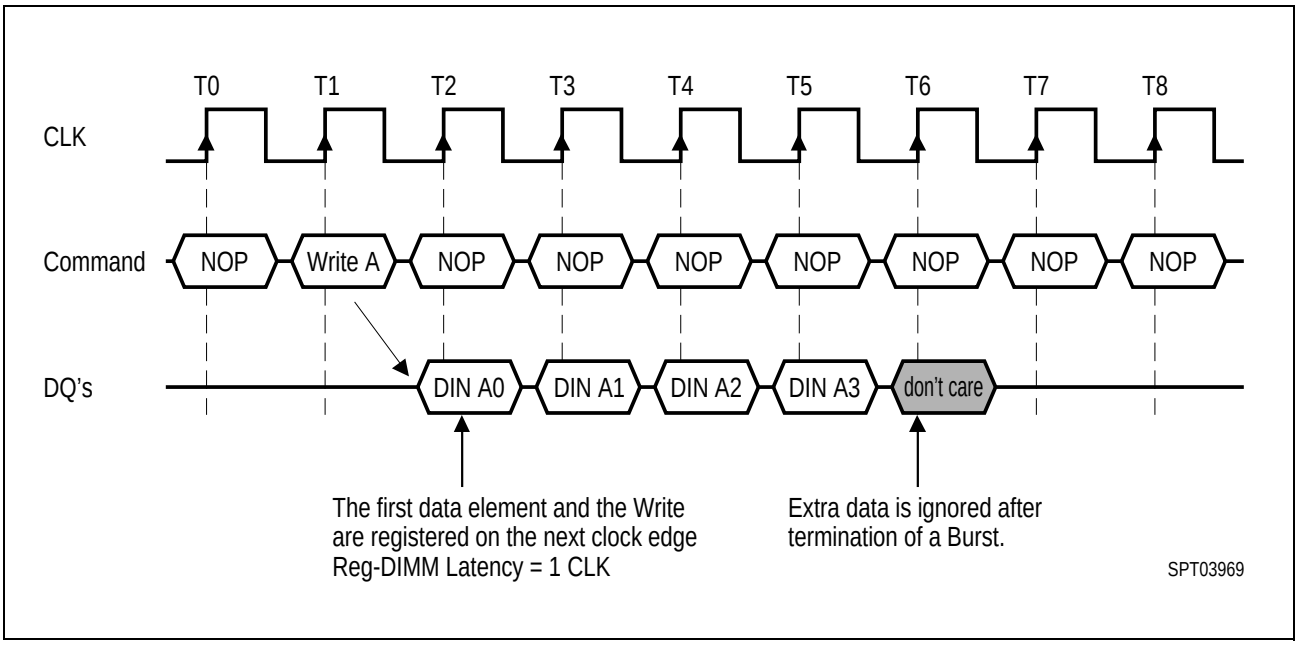
All control and address signals are synchronized with the positive edge of externally supplied clocks and are registered on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input control and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device $\overline{\text{CAS}}$ latency, in the case two clocks. With the register, the data is delayed according to the device $\overline{\text{CAS}}$ latency plus an additional clock cycle. This is know as the DIMM $\overline{\text{CAS}}$ latency, and in this example is four three. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.

Registered DIMM Burst Read Operation (BL = 4)



In case of a Burst Write Command the data-in is delayed one clock due the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. the remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.



Registered DIMM Burst Write Operation (BL = 4)