LSI LOGIC

L64735
Discrete Cosine Transform Processor

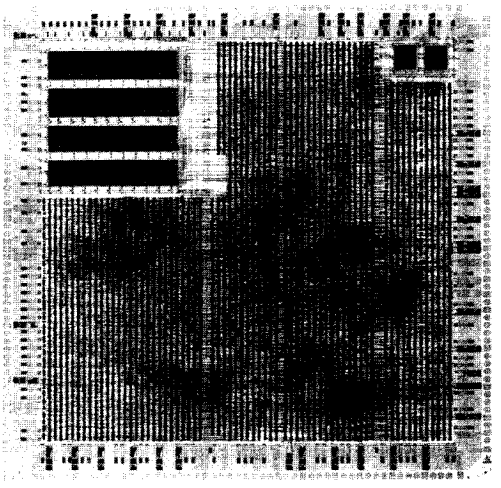
Description

The Discrete Cosine Transform Processor computes both the forward and inverse DCT over 8 x 8 data blocks and meets the proposed International Consultative Committee for Telephones and Telegraphs (CCITT) standard (H.261). The device operates with either signed or unsigned pixel data. Eight-bit unsigned pixel data is transformed into 11-bit signed DCT coefficients while 9-bit signed pixel data is transformed into 12-bit signed DCT coefficients. DCT coefficients are accepted and generated in either raster order or zig-zag order. The pixel data I/O is always in raster order. The device supports data rates up to 35 MHz.

The cosine basis functions and control signals are generated internally.

The user only supplies a signal indicating the beginning of the data block, the direction of the transform, the format of the pixel data and the ordering of the DCT coefficients. The discrete cosine transform is ideal for image or video compression systems as the DCT coefficients can typically be coded with fewer bits of information than the original image. To ensure proper tracking between an encoder and decoder, the proposed CCITT standard has placed strict limits on the statistics of the errors encountered when computing the inverse DCT. This device complies fully with these requirements.

The device is available in 68-pin ceramic and plastic PGAs and 100-pin PQFP's.



L64735 Chip

Features

- 8 x 8 data block
- Handles continuous data streams
- 9-bit signed or 8-bit unsigned pixel data
- Raster order pixel data
- Zig-zag or raster order DCT coefficients
- Compatible with proposed CCITT standard
- Bypass mode
- 20/27/35 MHz clock rates
- Simple external control
- L64735 is available in a 68-pin CPGA or PPGA (ceramic or plastic pin grid array) or 100-pin PQFP (plastic quad flat pack) package

Pin Listing and Description

(SIGNAL.0 is always the LSB)

PIX.0:8
Nine-bit I/O bus for PIXel data. The pixel data is input on this bus when FORWARD is HIGH and output on this bus when FORWARD is LOW. If UNSIGNED is HIGH, the 8-bit unsigned values are taken from and supplied on the 8 most significant bits of this bus (the LSB is ignored).

PBS
I/O indicating a Pixel Block Start on the PIX bus when HIGH.

PBID
Pixel Block ID I/O. Auxiliary data passed to (FORWARD HIGH) or from (FORWARD LOW) DBID for use by other devices. The data on this pin is only valid when PBS is HIGH or a multiple of 64 cycles after PBS last went HIGH and is delayed by 168 cycles to maintain alignment with the data.

DCTCOEFF.0:11
Twelve-bit DCT COEFficient I/O bus. The DCT coefficients are input on this bus when FORWARD is LOW and output on this bus when FORWARD is HIGH. When UNSIGNED is HIGH, the 11-bit DCT coefficient data values are taken from and supplied on the 11 most significant bits of this bus (the LSB is ignored).

April 1991 Order Number 44022

Pin Listing and Description (SIGNAL.0 is always the LSB) (Continued)

DBS
I/O indicating a DCT coefficient Block Start on the DCTCOEFF bus when HIGH.

DBID
DCT coefficient Block ID I/O. Auxiliary data passed to or from PBID for use by other devices. The data on this pin is only valid when DBS is HIGH or a multiple of 64 cycles after DBS last went HIGH and is delayed by 168 cycles to maintain alignment with the data.

FORWARD
FORWARD transform mode select input. When HIGH, the device computes the forward DCT and when LOW, the device computes the inverse DCT.

ORDERZZ
Input used to select the order of the DCT coefficient data. When HIGH, zig-zag ordering is used. When LOW, the DCT coefficients are generated and accepted in raster order.

UNSIGNED
Input used to select the pixel data format. When HIGH, the pixel data is in 8-bit unsigned format. When LOW, 9-bit signed format pixel data is generated and accepted.

BYPASS
Input used to pass data directly from input to output. When BYPASS is LOW, normal forward or inverse DCT computations are performed. When BYPASS is HIGH, the data on the PIX bus is passed directly to the MSBs of the DCTCOEFF bus when FORWARD is HIGH. If FORWARD is LOW and BYPASS is HIGH, the 9 MSBs of the DCTCOEFF bus are passed to the PIX bus.

OE
Output Enable Input. When HIGH, the bidirectional signals are driven as determined by FORWARD. When LOW, all bidirectional signals float.

CLK
System clock. Controls all system functions at LOW to HIGH transitions.

RESET
Internal controller active HIGH reset for testing. Should be LOW for normal operation.

TESTO
LSI Logic test output. Should be left unconnected.

Pin Description Summary

Pin	No. of Pins	I/O	Description
PIX.0:8	9	I/O	Pixel input or output bus
PBS	1	I/O	Pixel block start flag
PBID	1	I/O	Pixel block ID I/O
DCTCOEFF.0:11	12	I/O	DCT coefficient input or output bus
DBS	1	I/O	DCT coefficient block start flag
DBID	1	I/O	DCT coefficient block ID I/O
FORWARD	1	I	Forward/inverse mode flag
ORDERZZ	1	I	Raster/zig-zag format select
UNSIGNED	1	I	Pixel data format select
BYPASS	1	I	Flag to bypass DCT computation
OE	1	I	Output enable input
CLK	1	I	Clock
RESET	1	I	Internal controller reset
TESTO	1	O	Test output. No connect

Operating Modes

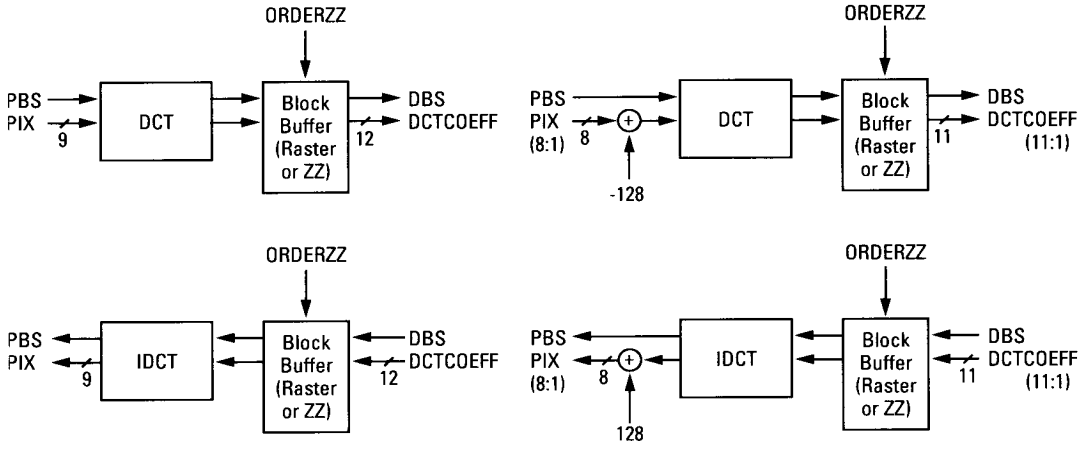


Figure 1. Functional Modes

Functional Description

The device operates in four primary modes as shown in Figure 1. The top diagrams show the forward transform operation (FORWARD HIGH) while inverse transform operation is shown in the bottom diagrams. Nine-bit signed pixel data is transformed to/from 12-bit DCT Coefficients when UNSIGNED is LOW (left diagrams) and 8-bit unsigned pixel data is transformed to/from 11-bit DCT Coefficients when UNSIGNED is HIGH (right diagrams).

The normal mode of operation occurs when BYPASS is LOW and OE is HIGH. In the forward (FORWARD is HIGH) and inverse (FORWARD is LOW) DCT modes, the processor inputs and outputs are related by the equations in Table 2.

When BYPASS is HIGH, the input data is passed directly from the active input to the active output. The direction of data flow is the same when the forward or inverse transform is being computed as specified by the FORWARD pin. The data will be delayed by two cycles. In addition, when FORWARD is HIGH, the 9-bits on the PIX bus will appear on the MSBs of the DCTCOEFF bus and when FORWARD is LOW, the 9 MSBs on the DCTCOEFF bus will appear on PIX bus.

Table 2. DCT Mode

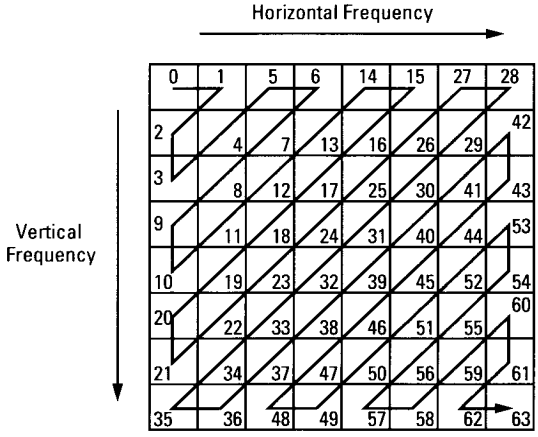
Transform	Equation
Forward	$BD(u,v) = \frac{1}{4} C(u)\,C(v) \sum_{x=0}^{7} \sum_{y=0}^{7} bd(x,y) \cos\left[\frac{\pi u(2x+1)}{16}\right] \cos\left[\frac{\pi v(2y+1)}{16}\right]$
Inverse	$bd(x,y) = \frac{1}{4} \sum_{u=0}^{7} \sum_{v=0}^{7} C(u)C(v)\,BD(u,v) \cos\left[\frac{\pi u(2x+1)}{16}\right] \cos\left[\frac{\pi v(2y+1)}{16}\right]$

Note:

$$C(i) = \begin{cases} \frac{1}{\sqrt{2}} & \text{if } i = 0 \\ 1 & \text{if } i \neq 0 \end{cases}$$

Data Ordering

The pixel and DCT coefficient data are always accessed a block at a time with 64 consecutive values being input or output in 64 consecutive clock cycles. The pixel data is always input and output in raster order. The DCT coefficients can be specified to be in either raster (ORDERZZ LOW) or zig-zag order (ORDERZZ HIGH). Zig-zag order is normally used when the DCT coefficients are run coded. These two orders are shown in Figure 2 (raster on the right and zig-zag on the left).



0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

Figure 2. Zig-zag and Raster Ordering

Output Rounding and Clipping

The data formats on the PIX and DCTCOEFF buses are controlled by the UNSIGNED pin. UNSIGNED is set HIGH when processing 8-bit unsigned pixel data and LOW when processing two's complement pixel data (the difference of two unsigned images). When UNSIGNED is HIGH, the constant 128 is subtracted from the input pixel data in the forward transform and added to the output pixel data in the inverse transform to ensure that all DCT coefficients can be represented by an 11-bit signed number. In all cases, the output of the device is rounded and clipped to the appropriate range. In Table 3, the data formats and ranges for the PIX and DCTCOEFF buses are shown. "S" represents the sign bits (negative significance) and "b" represents the data bits (positive significance). "X" represents bits which are or should be ignored.

Table 3. Data Formats and Ranges

UNSIGNED	PIX.8:0		DCTCOEFF.11:0	
	Data	Range	Data	Range
0	Sbbbbbbbb	-256 to 255	Sbbbbbbbbbbb	-2048 to 2047
1	bbbbbbbbX	0 to 255	SbbbbbbbbbbX	-1024 to 1023

Setting the Operation Mode

There are four external signals which determine the operation of the device. The FORWARD, BYPASS, UNSIGNED and ORDERZZ pins set the function of the device and the format of the DCTCOEFF and PIX buses. When any of these signals change, all partial results inside the device may be corrupted. To prevent the loss of data, the user should wait for 168 cycles after the last input value has been latched before changing the function.

Performance

Error Performance

Table 4 shows the error performance of the device for various operating conditions. The input data in each case is random and for the inverse DCT was generated according to the proposed CCITT standard which requires the simulation of 60,000 blocks. The output of the device was compared to the forward or inverse transform of the input data when computed with double precision floating point and rounded to the number of bits indicated. All error measures are referenced to the LSB of the output. The format for each entry is: measured_error/specified_max_error.

It is also interesting to know how well the original image is reconstructed after passing through the forward and inverse DCT. One million random inputs in the range -256 to 256 were formed into 8 x 8 blocks and processed by a forward DCT and inverse DCT. The reconstructed pixel values were compared with the original pixel values. The results are summarized in Table 5.

It can be seen that 90.4% of the time the original 9-bit signed image is reconstructed without error. In 9.6% of the cases, one LSB of error occurs in the reconstruction. No errors larger than one LSB occured.

Table 4. Error Performance

DCT	No. Input Bits	No. Output Bits	Max Magnitude Error	Mean Error	Mean Sq Error	Max Pixel Mean Error	Max Pixel Mean Sq Error
Inv DCT	12	9	1/1	.0006/.0015	.019/.020	.008/.015	.021/.060
For DCT	9	12	1/NA	.0002/NA	.060/NA	.0062/NA	.084/NA

Table 5. Error Performance After Reconstruction

Error Magnitude	Number	Percentage
0	904,188	90.4%
1	95812	9.6%
>1	0	0%

Latency

Although the execution time is only 64 cycles, there is a latency or delay of 168 cycles between the first input of a data block and the first output of the data block.

Functional Waveforms

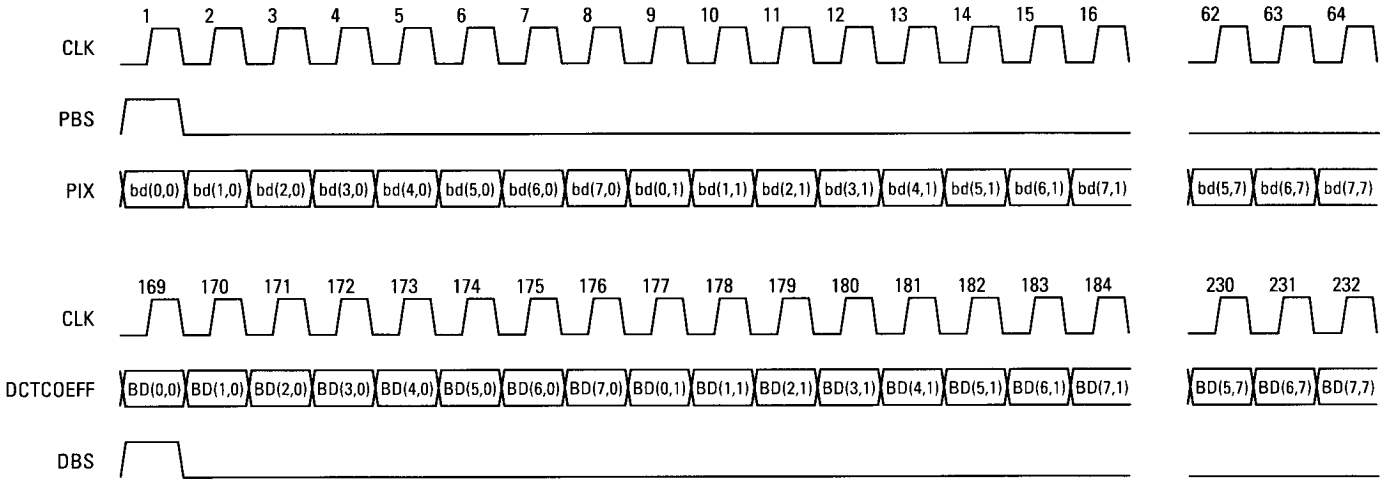


Figure 3. DCT Mode (FORWARD HIGH, ORDERZZ LOW)

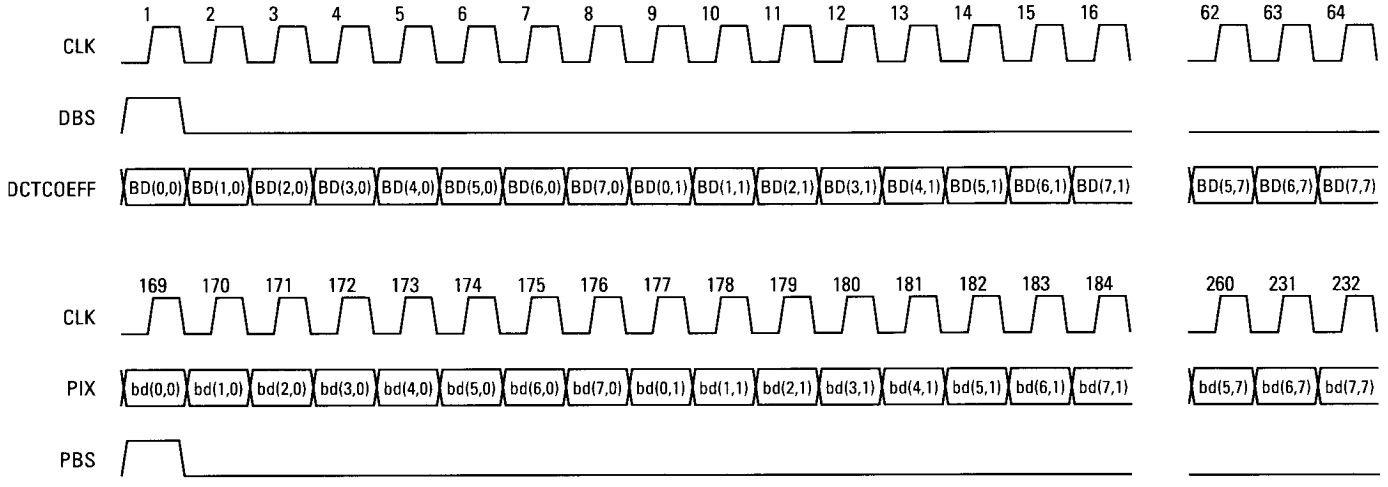


Figure 4. IDCT Mode (FORWARD LOW, ORDERZZ LOW)

Notes:
1. bd (x,y) represents the pixel data.
2. BD (x,y) represents the DCT Coefficient data.

AC Timing Waveforms

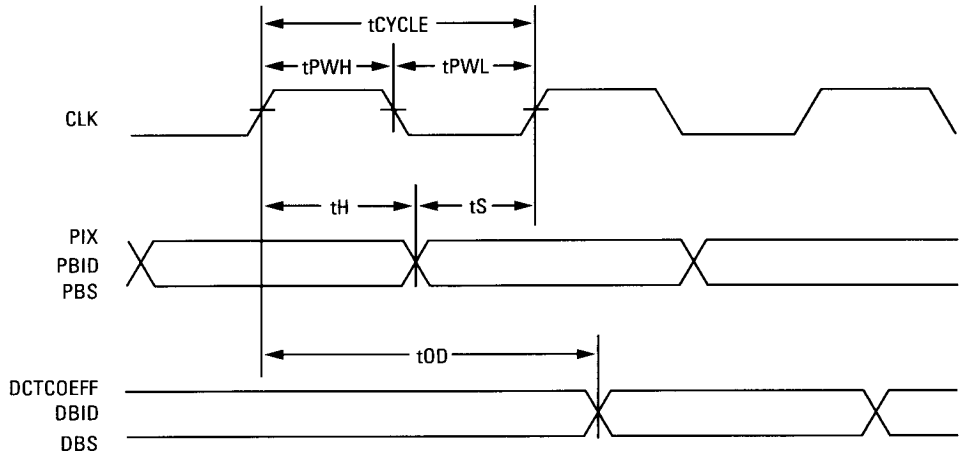


Figure 5. Forward Transform (FORWARD HIGH)

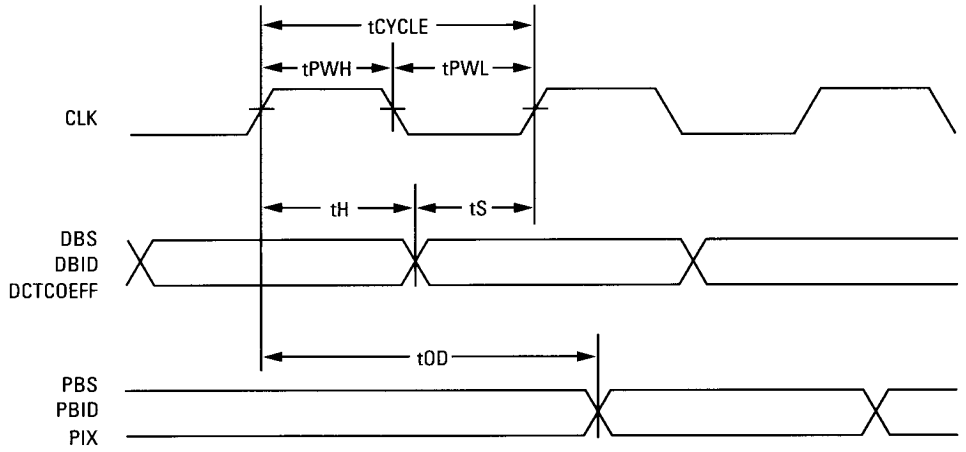


Figure 6. Inverse Transform (FORWARD LOW)

AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

		L64735-35		L64735-27		L64735-20	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
tCYCLE	CLK cycle time	28		37		50	
tPWH	Min CLK pulse width, HIGH	12		17		20	
tPWL	Min CLK pulse width, LOW	12		17		20	
tS	Input setup time to CLK	6		9		11	
tH	Input hold time CLK	2		2		2	
tOD	DO Output Delay from CLK		18*		20*		27*

Notes:
1. All times are in ns.
2. *output loading = 50 pF.

L64735 Package Pin Information (68-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
D10	BYPASS	K3	DCTCOEFF.9	B7	PIX.5	K1	VDD
F10	CLK	L2	DCTCOEFF.10	A6	PIX.6	K10	VDD
J11	DBID	H1	DCTCOEFF.11	B5	PIX.7	K2	VDD
J10	DBS	E10	FORWARD	A5	PIX.8	L10	VDD
K9	DCTCOEFF.0	H10	OE	E11	RESET	L6	VDD
L8	DCTCOEFF.1	G10	ORDERZZ	G1	TESTO	B1	VSS
K8	DCTCOEFF.2	A4	PBID	F11	UNSIGNED	B6	VSS
L7	DCTCOEFF.3	B4	PBS	A2	VDD	C10	VSS
K7	DCTCOEFF.4	A10	PIX.0	A7	VDD	F2	VSS
K5	DCTCOEFF.5	B9	PIX.1	B10	VDD	G11	VSS
L4	DCTCOEFF.6	A9	PIX.2	B11	VDD	J2	VSS
K4	DCTCOEFF.7	B8	PIX.3	B2	VDD	K11	VSS
L3	DCTCOEFF.8	A8	PIX.4	E1	VDD	L5	VSS

L64735 Package Pin Information (68-Pin PGA, By Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VDD	B7	PIX.5	G1	TESTO	K7	DCTCOEFF.4
A4	PBID	B8	PIX.3	G10	ORDERZZ	K8	DCTCOEFF.2
A5	PIX.8	B9	PIX.1	G11	VSS	K9	DCTCOEFF.0
A6	PIX.6	B10	VDD	H1	DCTCOEFF.11	K10	VDD
A7	VDD	B11	VDD	H10	OE	K11	VSS
A8	PIX.4	C10	VSS	J2	VSS	L2	DCTCOEFF.10
A9	PIX.2	D10	BYPASS	J10	DBS	L3	DCTCOEFF.8
A10	PIX.0	E1	VDD	J11	DBID	L4	DCTCOEFF.6
B1	VSS	E10	FORWARD	K1	VDD	L5	VSS
B2	VDD	E11	RESET	K2	VDD	L6	VDD
B4	PBS	F2	VSS	K3	DCTCOEFF.9	L7	DCTCOEFF.1
B5	PIX.7	F10	CLK	K4	DCTCOEFF.7	L8	DCTCOEFF.1
B6	VSS	F11	UNSIGNED	K5	DCTCOEFF.5	L10	VDD

Note: All pins not shown are no connects.

L64735 Package Pin Information (100-Pin PQFP, by Signal Name)

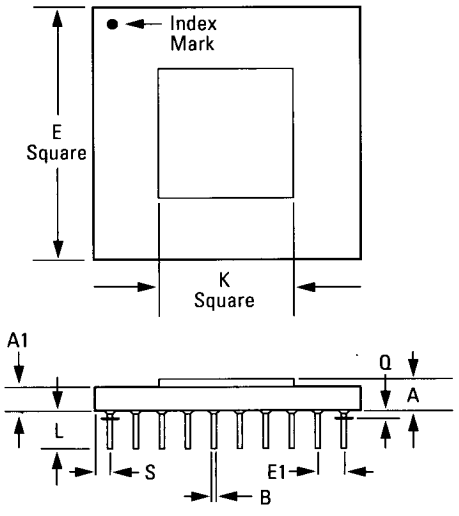
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
68	BYPASS	33	DCTCOEFF.7	85	PIX.5	51	VDD
63	CLK	32	DCTCOEFF.8	91	PIX.6	55	VDD
58	DBID	31	DCTCOEFF.9	92	PIX.7	75	VDD
57	DBS	65	FORWARD	93	PIX.8	79	VDD
48	DCTCOEFF.0	59	OE	66	RESET	87	VDD
47	DCTCOEFF.1	60	ORDERZZ	16	TESTO	13	VSS
29	DCTCOEFF.10	98	PBID	64	UNSIGNED	23	VSS
22	DCTCOEFF.11	96	PBS	100	VDD	36	VSS
46	DCTCOEFF.2	80	PIX.0	11	VDD	5	VSS
45	DCTCOEFF.3	81	PIX.1	24	VDD	56	VSS
42	DCTCOEFF.4	82	PIX.2	28	VDD	61	VSS
35	DCTCOEFF.5	83	PIX.3	39	VDD	71	VSS
34	DCTCOEFF.6	84	PIX.4	4	VDD	90	VSS

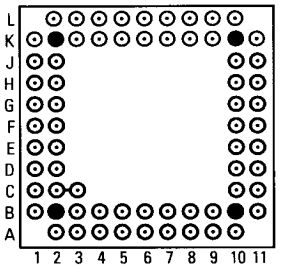
L64735 Package Pin Information (100-Pin PQFP, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
4	VDD	34	DCTCOEFF.6	58	DBID	81	PIX.1
5	VSS	35	DCTCOEFF.5	59	OE	82	PIX.2
11	VDD	36	VSS	60	ORDERZZ	83	PIX.3
13	VSS	39	VDD	61	VSS	84	PIX.4
16	TESTO	42	DCTCOEFF.4	63	CLK	85	PIX.5
22	DCTCOEFF.11	45	DCTCOEFF.3	64	UNSIGNED	87	VDD
23	VSS	46	DCTCOEFF.2	65	FORWARD	90	VSS
24	VDD	47	DCTCOEFF.1	66	RESET	91	PIX.6
28	VDD	48	DCTCOEFF.0	68	BYPASS	92	PIX.7
29	DCTCOEFF.10	51	VDD	71	VSS	93	PIX.8
31	DCTCOEFF.9	55	VDD	75	VDD	96	PBS
32	DCTCOEFF.8	56	VSS	79	VDD	98	PBID
33	DCTCOEFF.7	57	DBS	80	PIX.0	100	VDD

Note: All pins not shown are no connects.

68-Pin Plastic Pin Grid Array (PPGA) NB
68-Pin Ceramic Pin Grid Array (CPGA) FB



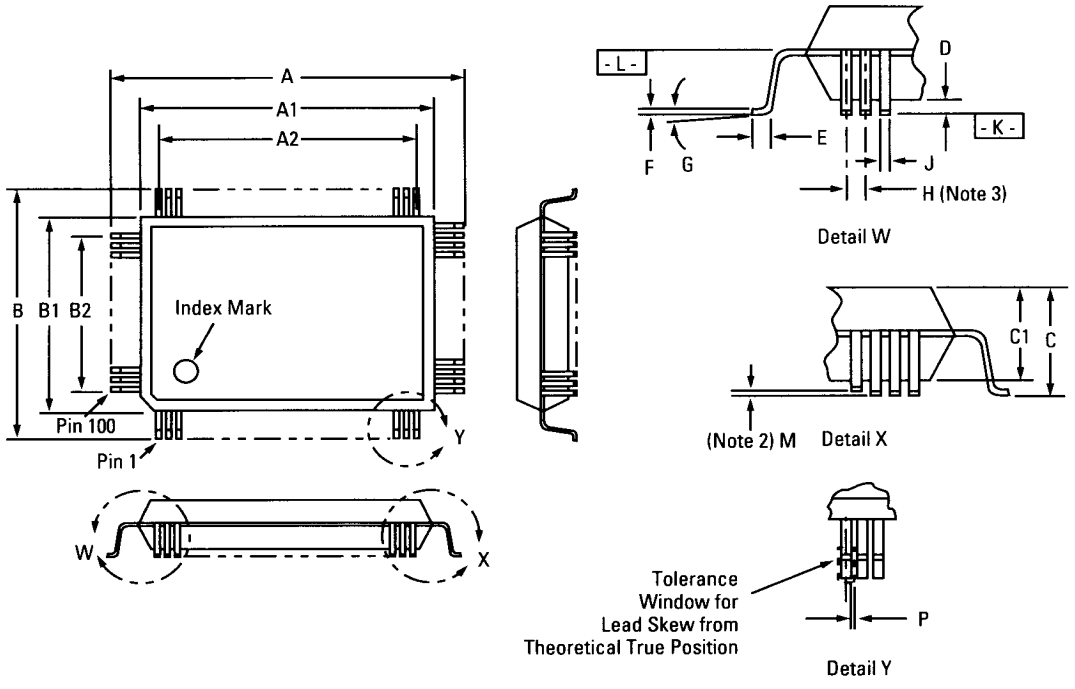


Plastic and Ceramic Pin Grid Array Dimensions

Dimensions		68-Pin	
		PPGA (NB)	CPGA (FB)
A	Max	0.139 (3.531)	0.117 (2.972)
A1	Ref	0.089 (2.261)	0.080 (2.032)
B	Min	0.016 (0.406)	0.016 (0.406)
	Max	0.020 (0.508)	0.020 (0.508)
E	Min	1.137 (28.88)	1.086 (27.58)
	Max	1.157 (29.39)	1.122 (28.50)
E1	Min	0.088 (2.235)	0.095 (2.413)
	Max	0.112 (2.845)	0.105 (2.667)
L	Min	0.187 (4.750)	0.175 (4.445)
	Max	0.207 (5.258)	0.185 (4.699)
Q	Ref	0.071 (1.803)	0.050 (1.270)
S	Ref	0.050 (1.270)	0.050 (1.270)
K	Ref	0.650 (16.51)	0.673 (17.09)

Notes:
1. Ceramic Packages are compliant to MIL-STD-38510, Rev H.
2. Controlling dimension-inch.

100-Pin Plastic Quad Flat Packs (PQFP) (Rectangular) (Gull Wing)



Plastic Quad Flat Pack (Gull Wing) Dimensions

Dimensions		100-Pin PQFP (Gull Wing)(PB)
A	Min	0.925 (23.50)
	Max	0.957 (24.30)
A1	Min	0.783 (19.90)
	Max	0.791 (20.10)
A2	Ref	0.742 (18.85)
B	Min	0.689 (17.50)
	Max	0.720 (18.30)
B1	Min	0.547 (13.90)
	Max	0.555 (14.10)
B2	Ref	0.486 (12.35)
C	Max	0.130 (3.30)
C1	Max	0.124 (3.15)

Dimensions		100-Pin PQFP (Gull Wing)(PB)
D	Max	0.012 (0.30)
E	Min	0.024 (0.060)
	Max	0.039 (1.00)
F	Min	0.004 (0.10)
	Max	0.010 (0.25)
G	Min	0°
	Max	10°
H	Nom	0.026 (0.65)
J	Min	0.008 (0.20)
	Max	0.016 (0.40)
M	Max	0.004 (0.10)
P	Max	0.002 (0.05)

Notes:
1. Controlling dimension - millimeter (in parenthesis).
2. Coplanarity of all leads shall be within 0.1 mm (0.004") (difference between highest and lowest lead with seating plane -K- as reference).
3. Lead pitch determined at datum -L-.

Ordering Information

L64735 G C -XX

- -XX: Speed MHz
- C: Temperature Range/Flow Option
  - C = Commericial (0°C to 70°C)
  - M = Military (-55°C to + 125°C) Processed to MIL-STD-883C Level B
- G: Package Code
  - G = 68-Pin Ceramic Grid Array
  - N = 68-Pin Plastic Grid Array
  - Q = 100-Pin Plastic Quad Flat Pack
- L64735: Device Type
  - Discrete Cosine Transform Processor

L64735
Discrete Cosine Transform Processor

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