

LH5316000

CMOS 16M (2M × 8 / 1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization (Byte mode)
1,048,576 × 16 bit organization (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
64-pin, 750-mil SDIP
64-pin, 14 × 20 mm² QFP
- X16 word-wide pinout

DESCRIPTION

The LH5316000 is a mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by an input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

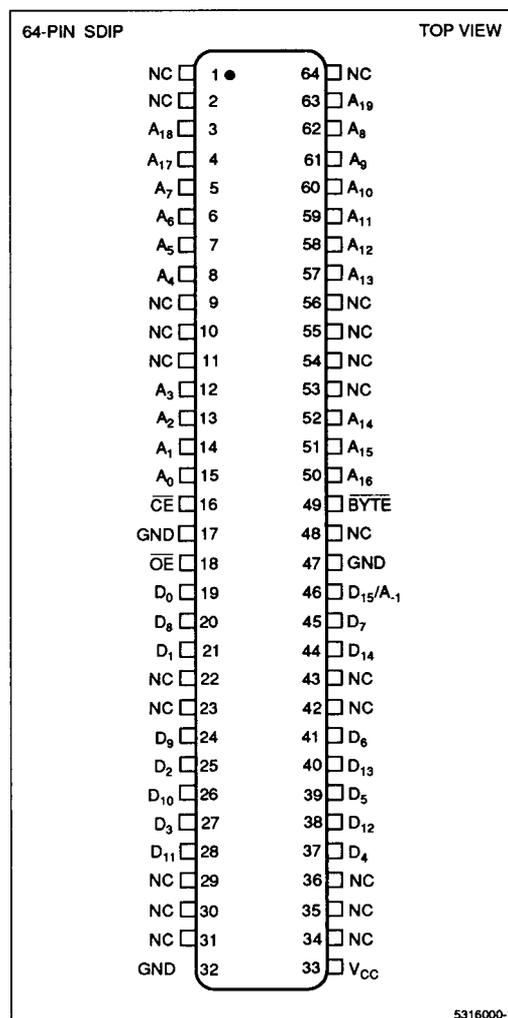


Figure 1. Pin Connections for SDIP Package

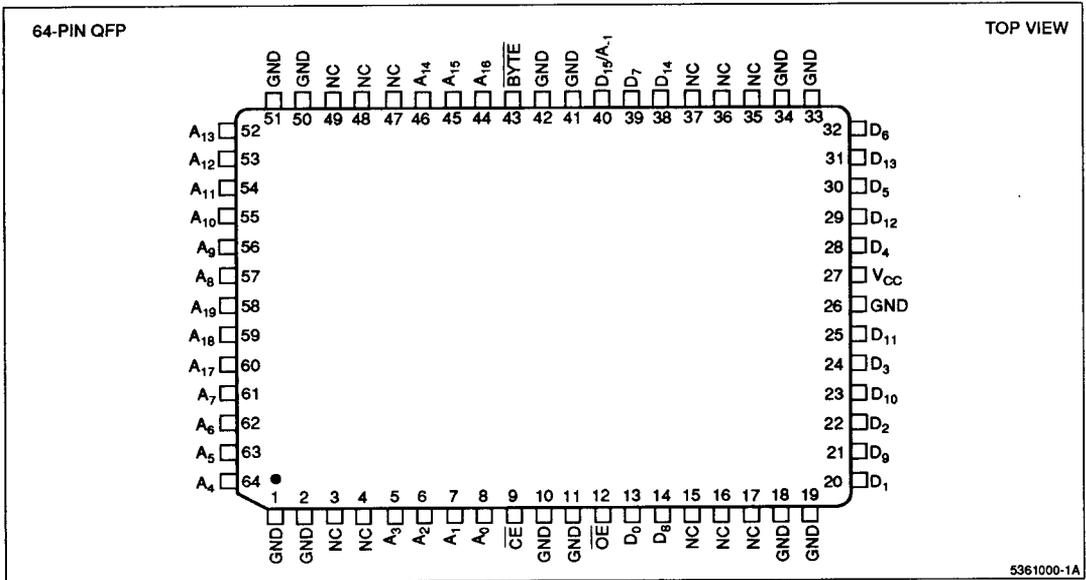


Figure 2. Pin Connections for QFP Package

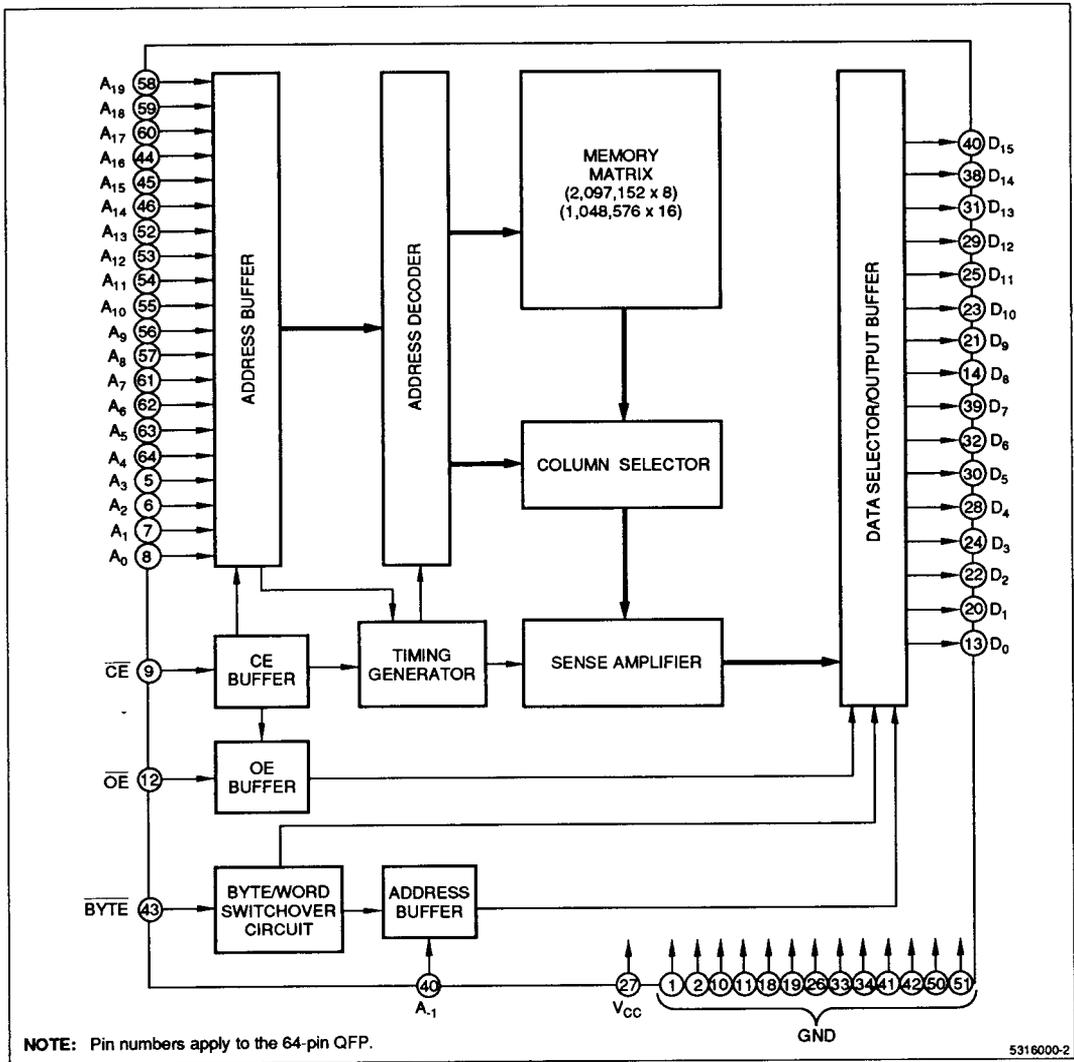


Figure 3. LH5316000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁	Address input (Byte Mode)	1
A ₀ - A ₁₉	Address input	
D ₀ - D ₁₅	Data output	
\overline{CE}	Chip Enable input	

SIGNAL	PIN NAME	NOTE
\overline{OE}	Output Enable input	
\overline{BYTE}	Byte/word switch	
V _{cc}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the bit configuration is set in byte mode, and data output (D₁₅) when in word mode. \overline{BYTE} input pin selects bit configuration.

TRUTH TABLE

\overline{CE}	\overline{OE}	BYTE	A ₁	MODE	D ₀ - D ₇	D ₈ - D ₁₅	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I _{SB})
L	H	X	X	Non selected	High-Z		Operating (I _{CC})
L	L	H	Inhibit	Word	D ₀ - D ₇	D ₈ - D ₁₅	Operating (I _{CC})
L	L	L	L	Byte	D ₀ - D ₇	High-Z	Operating (I _{CC})
L	L	L	H	Byte	D ₈ - D ₁₅	High-Z	Operating (I _{CC})

NOTE:

X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		-0.3	0.8	V	
Input "High" voltage	V _{IH}		2.2	V _{CC} +0.3	V	
Output "Low" voltage	V _{OL}	I _{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -400 μA	2.4		V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 200 ns		50	mA	2
	I _{CC2}	t _{RC} = 1 μs		40		
	I _{CC3}	t _{RC} = 200 ns		45	mA	3
	I _{CC4}	t _{RC} = 1 μs		35		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$		100		

NOTES:

1. $\overline{CE} / \overline{OE} = V_{IH}$.
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE} = V_{IL}$, outputs open.
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	200		ns	
Address access time	t _{AA}		200	ns	
Chip enable time	t _{ACE}		200	ns	
Output enable time	t _{OE}		80	ns	
Output hold time	t _{OH}	5		ns	
CE to output in High-Z	t _{CHZ}		70	ns	1
OE to output in High-Z	t _{OHZ}		70	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _{IN}			10	pF
Output capacitance	C _{OUT}			10	pF

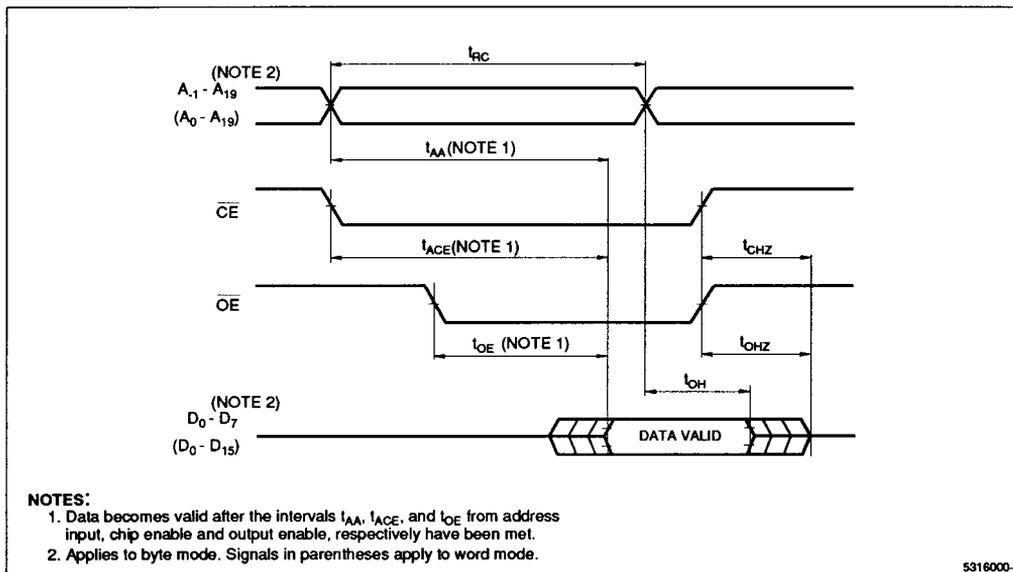


Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION

