

PF0040 Series

MOS FET Power Amplifier

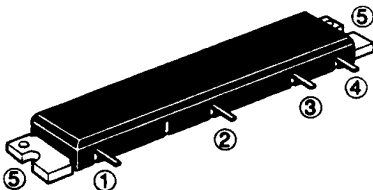
■ FEATURES

- High Stability: Load VSWR $\approx \infty$
- Low Power Control Current: 400 μ A
- Thin Package: 5 mm

■ ORDERING INFORMATION

Part No.	Operating Frequency	Application
PF0040	824 to 849 MHz	AMPS
PF0042	872 to 905 MHz	E-TACS

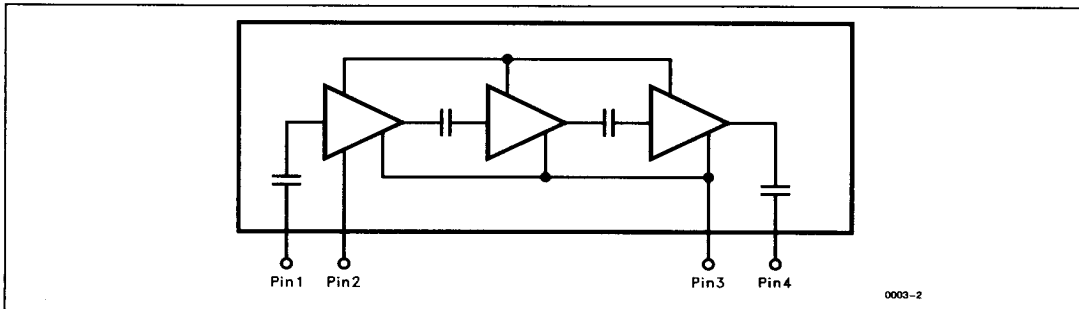
■ PIN OUT



0003-1

Pin No.	Pin Name
①	P_{in}
②	V_{APC}
③	V_{DD}
④	P_{out}
⑤	GND

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

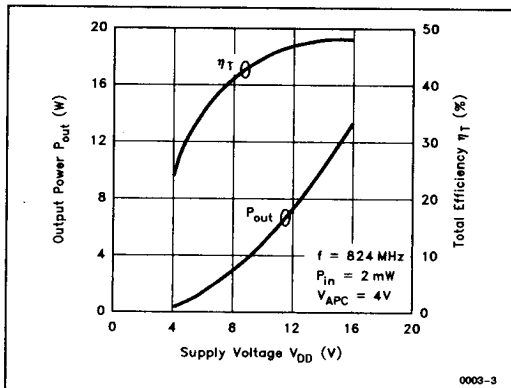
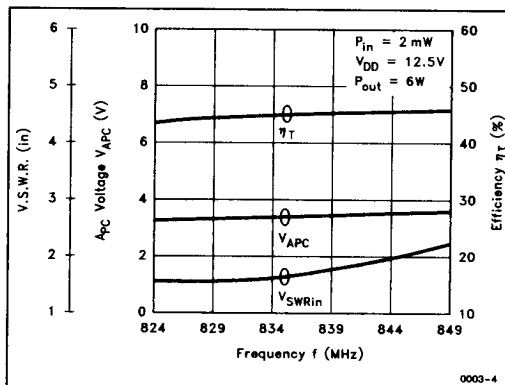
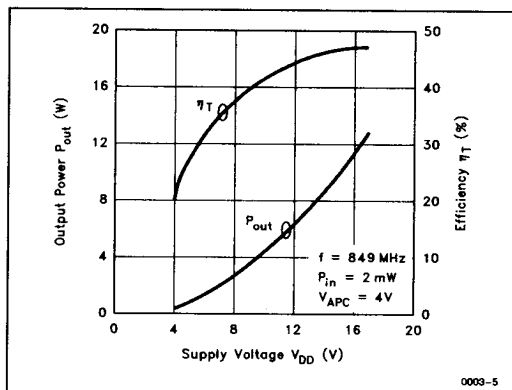
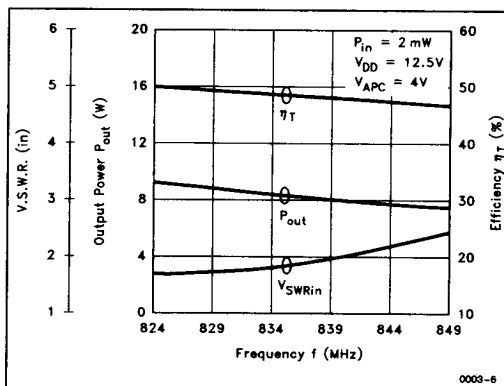
Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	17	V
Supply Current	I_{DD}	3	A
APC Voltage	V_{APC}	± 8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	- 30 to + 110	$^\circ\text{C}$
Storage Temperature	T_{stg}	- 40 to + 110	$^\circ\text{C}$

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain Cutoff Current	I_{DS}	—	—	500	μA	$V_{DD} = 17\text{V}$, $V_{APC} = 0\text{V}$
Total Efficiency	η_T	35	40	—	%	$P_{in} = 2\text{mW}$, $V_{DD} = 12.5\text{V}$, $P_{out} = 6\text{W}$ (at APC controlled), $Z_{in} = Z_{out} = 50\Omega$
2nd Harmonic Distortion	2nd H.D.	—	- 50	- 30	dB	
3rd Harmonic Distortion	3rd H.D.	—	- 50	- 30	dB	
Input VSWR	VSWR (in)	—	1.5	3	—	
Output VSWR	VSWR (out)	—	1.5	—	—	
Stability	—	No Parasitic Oscillation			—	$P_{in} = 2\text{mW}$, $V_{DD} = 12.5\text{V}$, $P_{out} = 6\text{W}$ (at APC controlled), $Z_{in} = Z_{out} = 50\Omega$, Output VSWR $\approx \infty$ All Phases, $t = 20\text{sec}$

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■ PF0040 STANDARD DATA

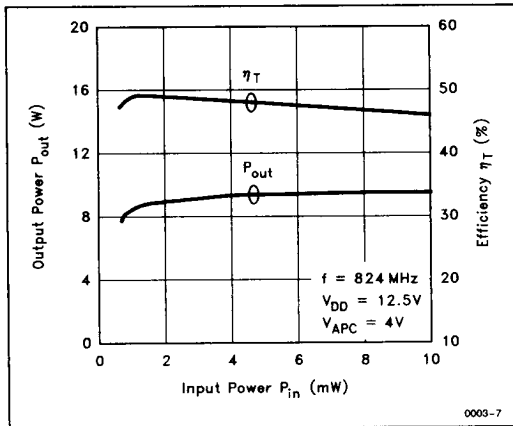
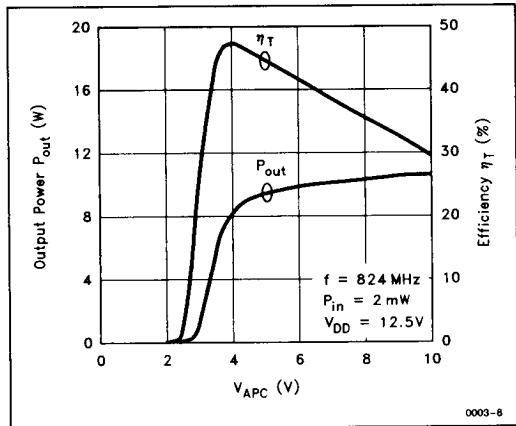
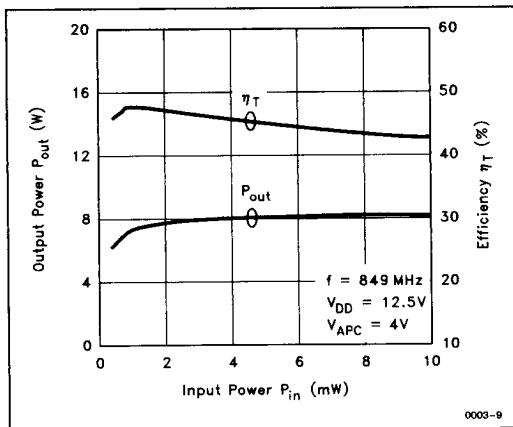
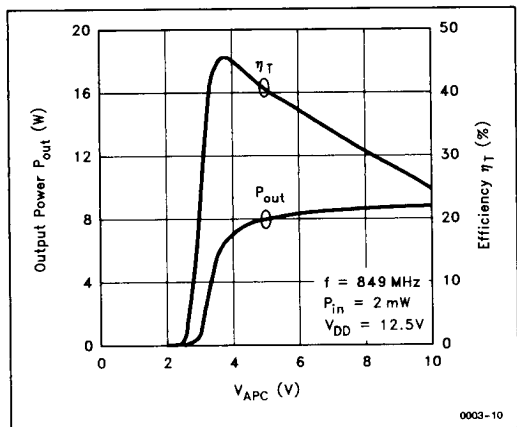
Figure 1. P_{out} , η_T vs. V_{DD} Figure 2. V_{APC} , η_T , VSWR (in) vs. FrequencyFigure 3. P_{out} , η_T vs. V_{DD} Figure 4. P_{out} , η_T , VSWR (in) vs. Frequency

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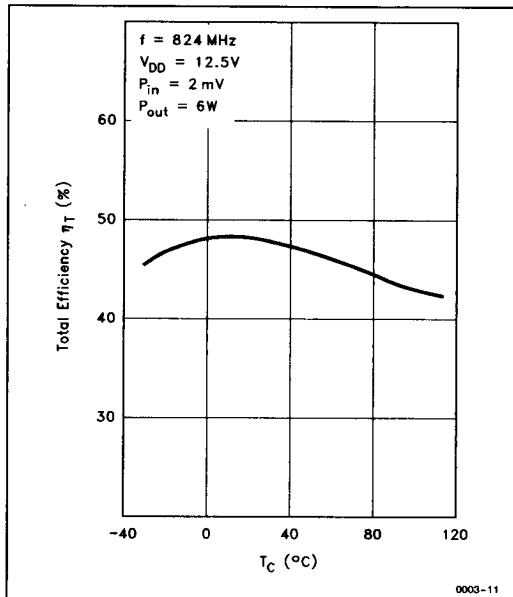
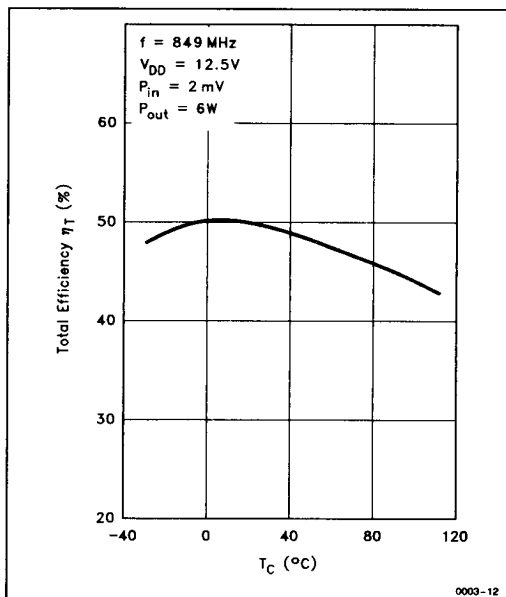
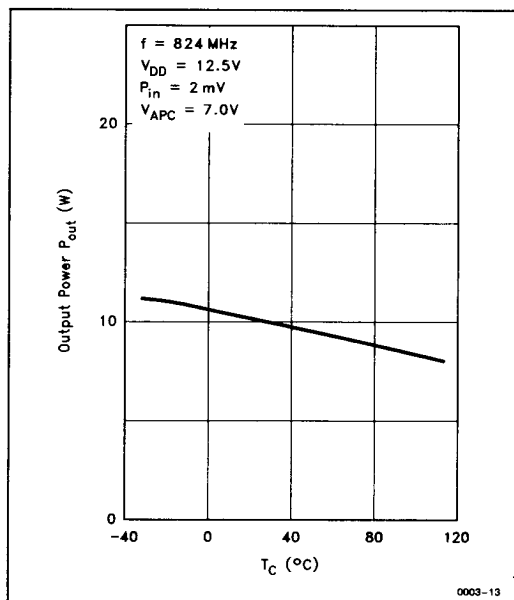
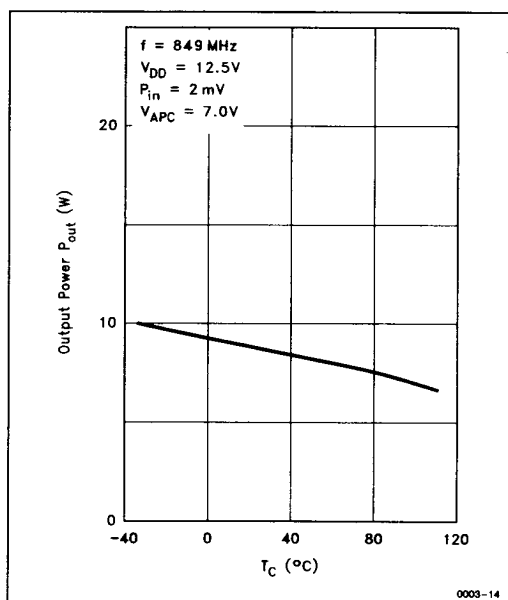
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■ PF0040 STANDARD DATA (cont.)

Figure 5. P_{out} , η_T vs. P_{in} Figure 6. P_{out} , η_T vs. V_{APC} Figure 7. P_{out} , η_T vs. P_{in} Figure 8. P_{out} , η_T vs. V_{APC}

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■ PF0040 STANDARD DATA (cont.)

Figure 9. η_T vs. T_C Figure 10. η_T vs. T_C Figure 11. P_{out} vs. T_C Figure 12. P_{out} vs. T_C

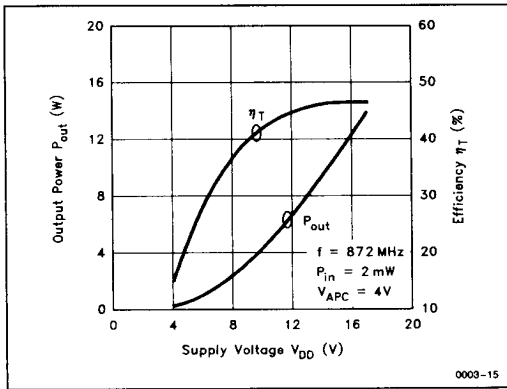
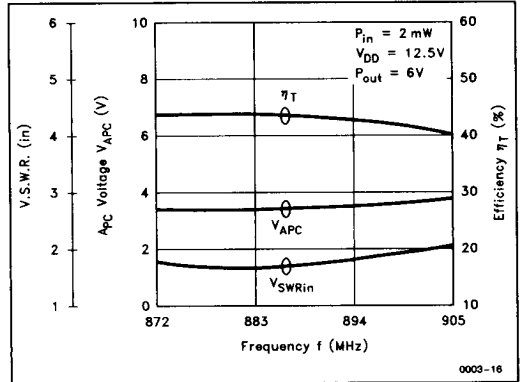
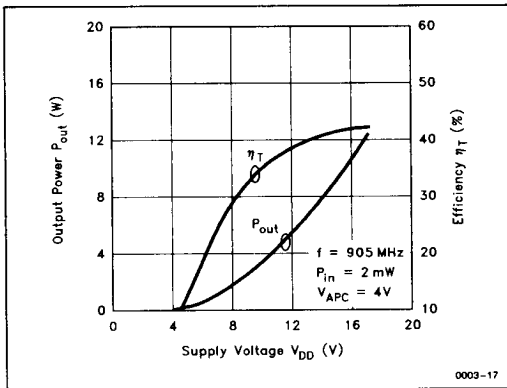
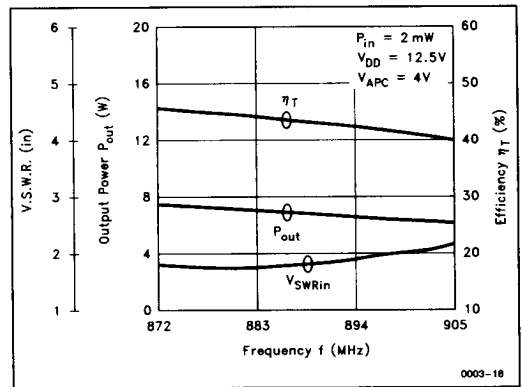
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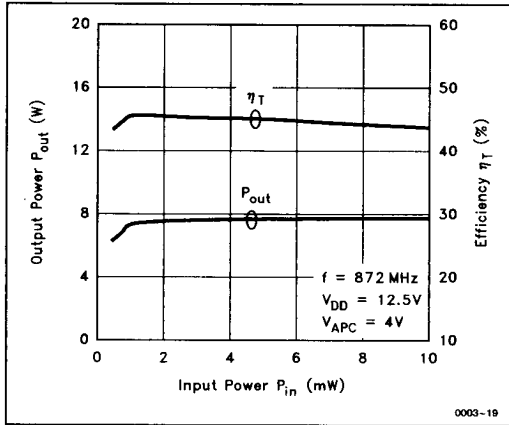
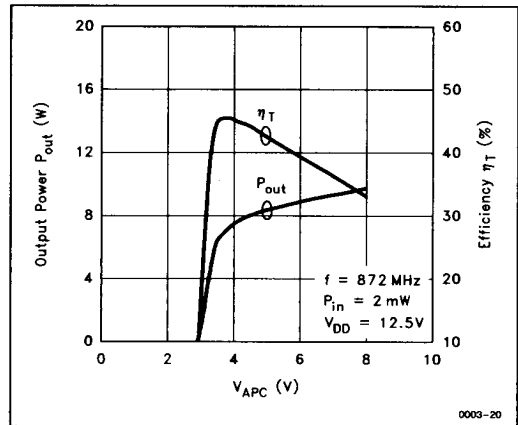
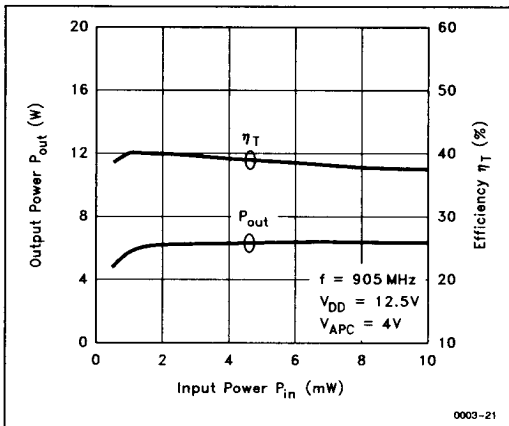
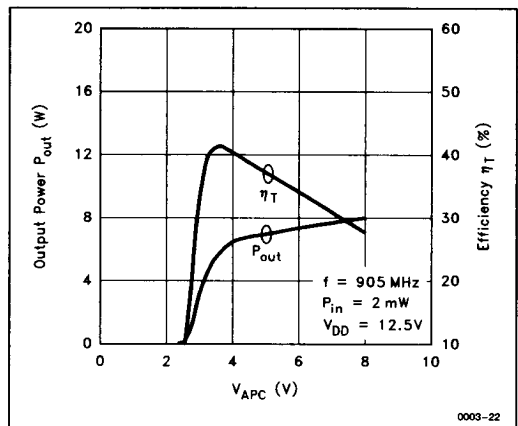
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■ PF0042 STANDARD DATA

Figure 13. P_{out} , η_T vs. V_{DD} Figure 14. V_{APC} , η_T , $V_{SWR}(in)$ vs. FrequencyFigure 15. P_{out} , η_T vs. V_{DD} Figure 16. P_{out} , η_T , $V_{SWR}(in)$ vs. Frequency

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■ PF0042 STANDARD DATA (cont.)

Figure 17. P_{out} , η_T vs. P_{in} Figure 18. P_{out} , η_T vs. V_{APC} Figure 19. P_{out} , η_T vs. P_{in} Figure 20. P_{out} , η_T vs. V_{APC}

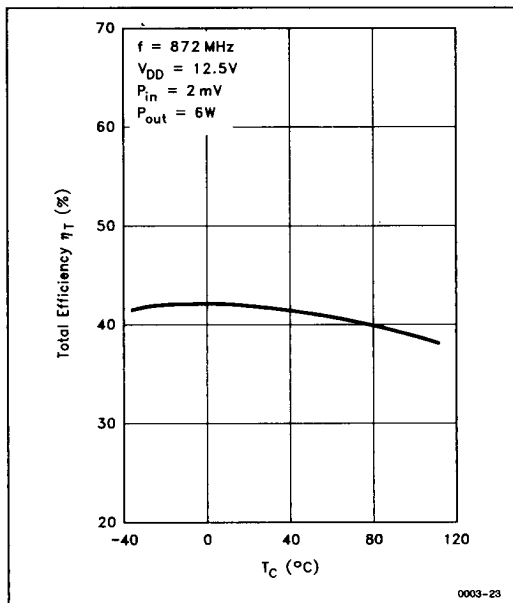
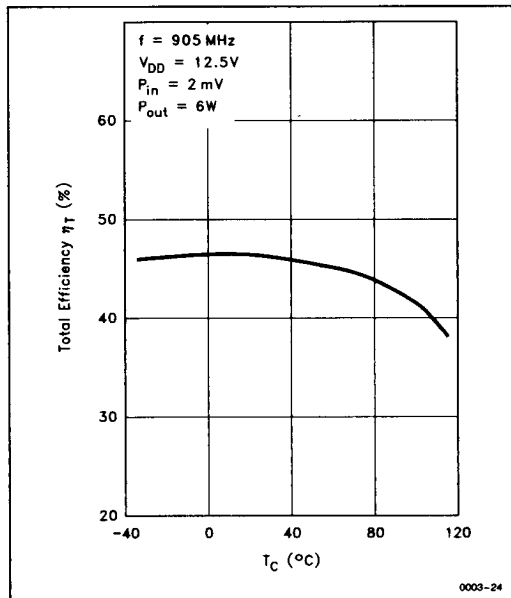
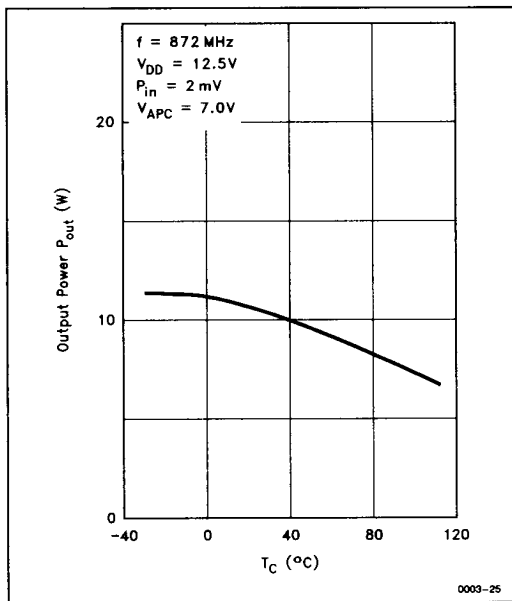
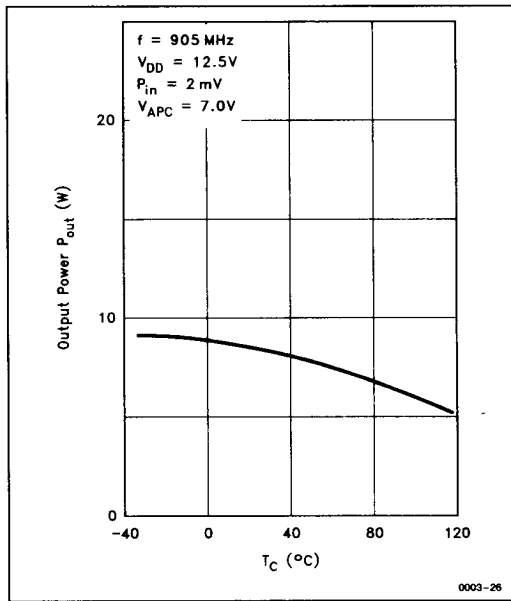
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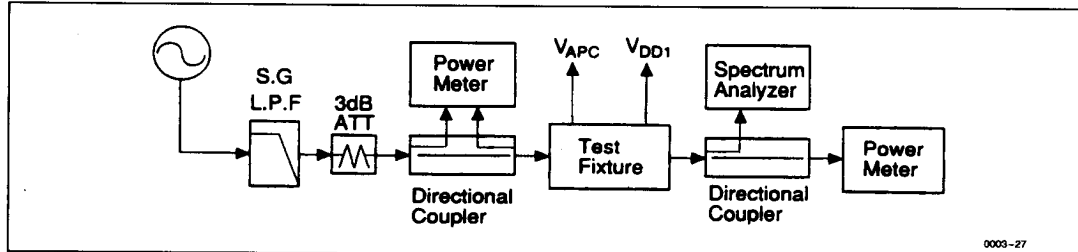
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■ PF0042 STANDARD DATA (cont.)

Figure 21. η_T vs. T_C Figure 22. η_T vs. T_C Figure 23. P_{out} vs. T_C Figure 24. P_{out} vs. T_C

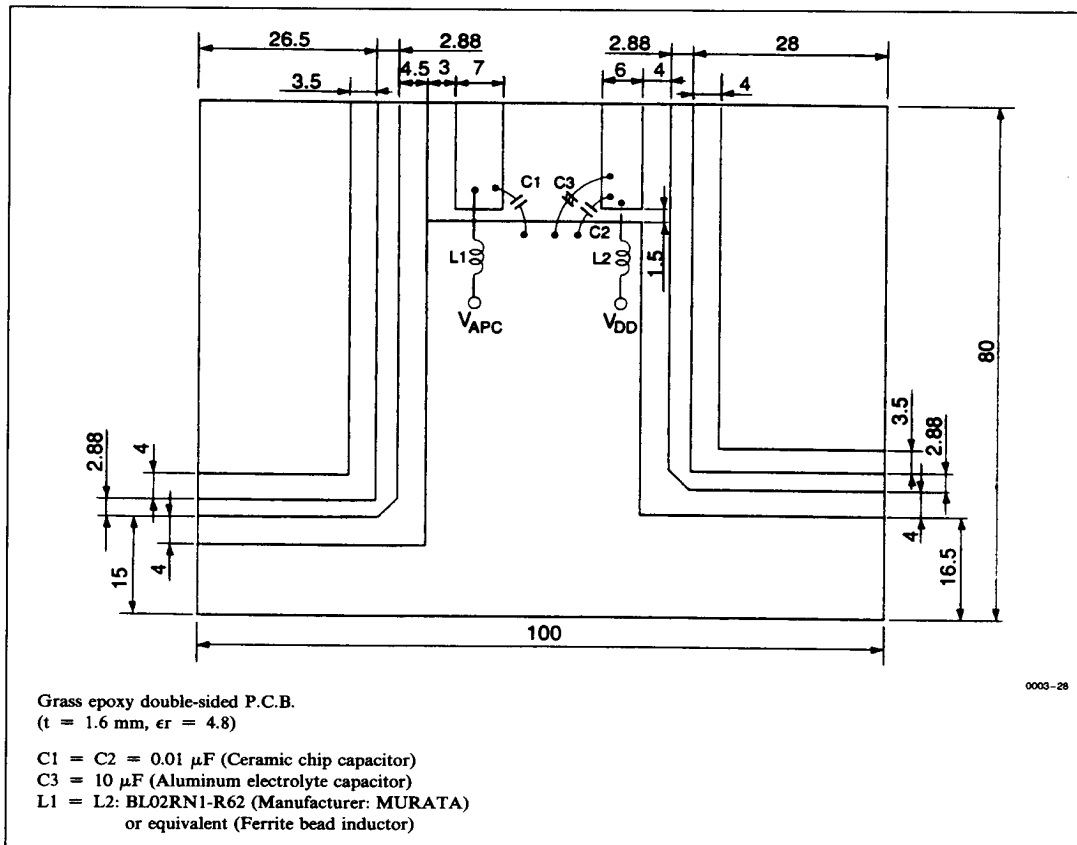
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■ TEST SYSTEM DIAGRAM



■ TEST FIXTURE PATTERN

Unit: mm



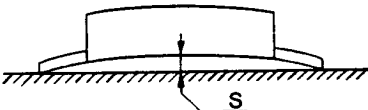
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MECHANICAL CHARACTERISTICS

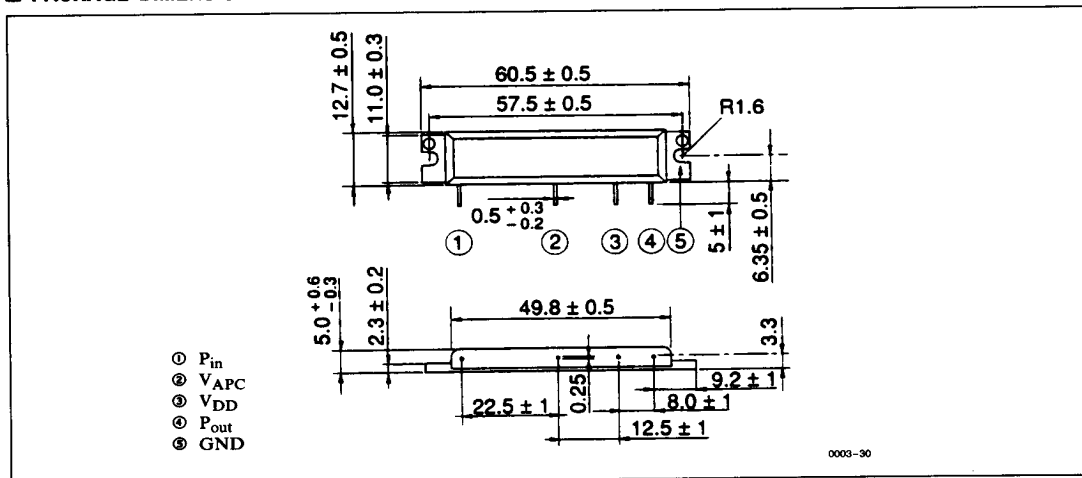
Item	Conditions	Spec.
Torque for screw up the heatsink flange	M3 Screw-Bolts	4–6 kg/cm
Warp size of the heatsink flange: S		S = 0 + 0.3 / - 0 mm

NOTES FOR USE

- Unevenness and distortion at the surface of the heatsink attached **module** should be less than 0.05 mm.
- There should not be any dust between **module** and heatsink.
- **Module** should be separated from PCB less than 1.5 mm.
- Soldering temperature and soldering time should be less than 230°C, 10 sec. (Soldering position spaced from the root point of the lead frame: 2mm)
- Recommendation of thermal joint compounds is TYPE G746 (Manufacturer: Shin-Etu Chemical, Co., Ltd.) or equivalent.
- To protect devices from electrostatic damage, soldering iron, measuring-equipment and human body, etc., they should be grounded.

PACKAGE DIMENSIONS

Unit: mm



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