DATA SHEET

NEC

BIPOLAR ANALOG + DIGITAL INTEGRATED CIRCUIT

μPB1003GS

REFERENCE FREQUENCY 18.414 MHz, 2nd IF FREQUENCY 1.023 MHz RF/IF FREQUENCY DOWNCONVERTER + PLL FREQUENCY SYNTHESIZER IC FOR GPS RECEIVER

DESCRIPTION

The μPB1003GS is a silicon monolithic integrated circuit for GPS receiver. This IC is designed as double conversion RF block integrated RF/IF frequency downconverter + PLL frequency synthesizer on 1 chip.

The μPB1003GS features shrink package, fixed prescaler and supply voltage. The 30-pin plastic SSOP package is suitable for high density surface mounting. The fixed division internal prescaler is needless to input serial counter data. Supply voltage is 3 V. Thus, the μPB1003GS can make RF block fewer components and lower power consumption.

This IC is manufactured using NEC's 20 GHz f_T NESAT™III silicon bipolar process. This process uses direct silicon nitride passivation film and gold electrodes. These materials can protect the chip surface from pollution and prevent corrosion/migration. Thus, this IC realizes excellent performance, uniformity and reliability.

FEATURES

- Double conversion : f_{REFin} = 18.414 MHz, $f_{2ndIFout}$ = 1.023 MHz
- Integrated RF block : RF/IF frequency downconverter + PLL frequency synthesizer
- High-density surface mountable : 30-pin plastic SSOP (10.11 × 6.1 × 2.0 mm)
- Needless to input counter data : fixed division internal prescaler
  - VCO side division : ÷ 168 (÷ 8, ÷ 7 and ÷ 3 serial prescalers)
  - Reference division : ÷ 2
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Low current consumption : I_{CC} = 37.5 mA$_{TYP.}$ @ 3 V
- Gain adjustable externally : Gain control voltage pin (control voltage up vs. gain down)

USAGE

- Consumer use GPS receiver of reference frequency 18.414 MHz, 2nd IF frequency 1.023 MHz

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPB1003GS-E1	30-pin plastic SSOP (300 mil)	Embossed tape 16 mm wide. QTY 2.5 kp/reel. Pin 1 is in tape pull-out direction.

Remarks To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPB1003GS)

Caution Electro-static sensitive devices

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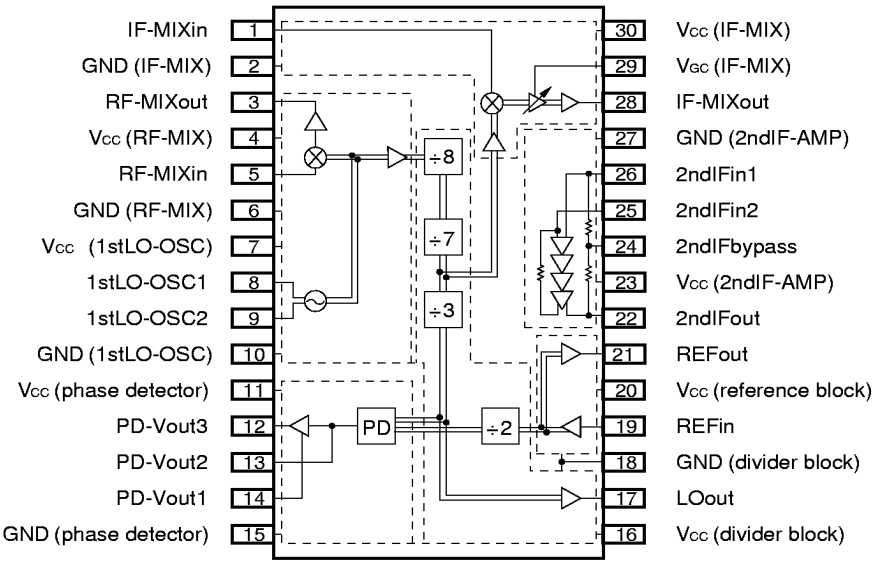
PIN CONNECTION AND INTERNAL BLOCK DIAGRAM



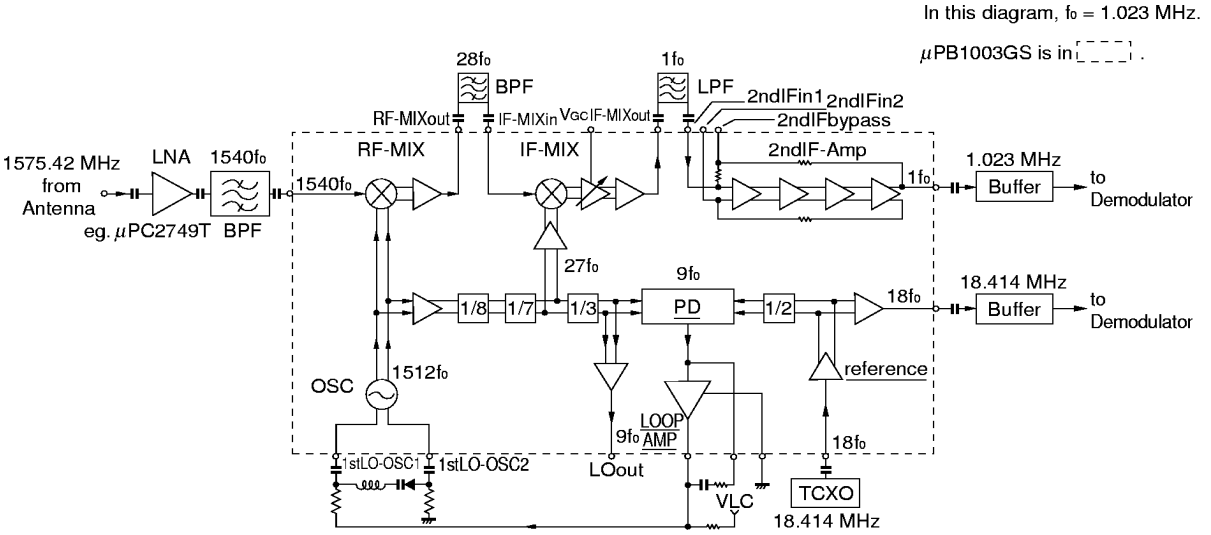
PRODUCT LINE-UP (T_A = +25 °C, V_{CC} = 3.0 V)

TYPE	PART NUMBER	FUNCTIONS (frequency unit: MHz)	V_{CC} (V)	I_{CC} (mA)	CG (dB)	PACKAGE
General purpose wideband separate IC	μPC2756T	RF downconverter with osc. Tr	2.7 to 3.3	6	14	6 pin mini mold
	μPC2753GR	IF downconverter with gain control amplifier	2.7 to 3.3	6.5	60 to 79	20 pin plastic SSOP (225 mil)
Clock frequency specific 1 chip IC	μPB1003GS	RF/IF downconverter + PLL synthesizer REF = 18.414/1stIF = 28.644/ 2ndIF = 1.023	2.7 to 3.3	37.5	72 to 92	30 pin plastic SSOP (300 mil)
	μPB1004GS	RF/IF downconverter + PLL synthesizer REF = 16.368/1stIF = 61.380/ 2ndIF = 4.092	2.7 to 3.3	37.5	72 to 92	30 pin plastic SSOP (300 mil)

Notice Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.
To know the associated products, please refer to their latest data sheets.

SYSTEM APPLICATION EXAMPLE

GPS receiver RF block diagram



Notice This diagram schematically shows only the μPB1003GR's internal functions on the system.
This diagram do not present the actual application circuits.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{CC}	T_A = +25 °C	3.6	V
Circuit current	I_{CC}	T_A = +25 °C	62	mA
Power dissipation	P_D	Mounted on double-sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB at T_A = +85 °C	433	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

RECOMMENDED OPERATING RANGE

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	–20	+25	+85	°C
RF input frequency	f_{RFin}	–	1575.42	–	MHz
1st LO oscillating frequency	$f_{1stLOin}$	1526.776	1546.776	1566.776	MHz
1st IF input frequency	$f_{1stIFin}$	–	28.644	–	MHz
2nd LO input frequency	$f_{2ndLOin}$	–	27.621	–	MHz
2nd IF input/output frequency	$f_{2ndIFin}$ $f_{2ndIFout}$	–	1.023	–	MHz
Reference input/output frequency	f_{REFin} f_{REFout}	–	18.414	–	MHz

ELECTRICAL CHARACTERISTICS (Unless otherwise specified; T_A = +25 °C, V_{CC} = 3.0 V)

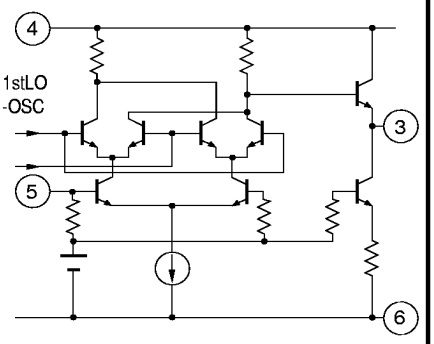
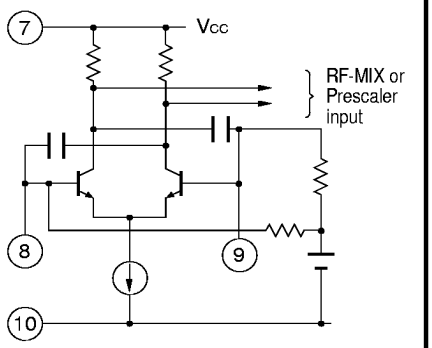
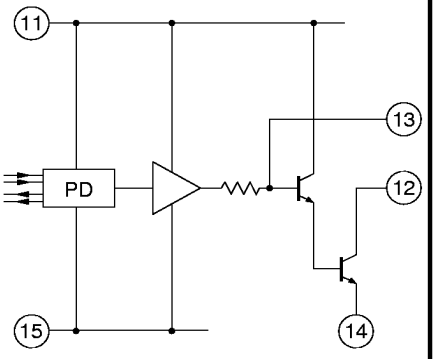
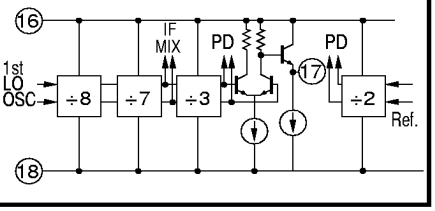
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Total Circuit Current	I_{CC}total	No Signals	27.1	37.5	52.7	mA
RF Downconverter block (f_{RFin} = 1575.42 MHz, $f_{1ndLOin}$ = 1546.776 MHz, P_{LOin} = –10 dBm, Z_L = Z_S = 50 Ω)						
Circuit Current 1	$I_{CC}1$	No Signals	7.2	10	12.1	mA
RF Conversion gain	CG_{RF}	P_{RFin} = –40 dBm	9.5	12.5	15.5	dB
RF·SSB Noise Figure	NF_{RF}	P_{RFin} = –40 dBm	–	12.5	15.5	dB
Maximum IF output	$P_{O(sat)RF}$	P_{RFin} = –10 dBm	–8	–5	–2	dBm
IF Downconverter block ($f_{1stIFin}$ = 28.644 MHz, $f_{2ndLOin}$ = 27.621 MHz, Z_S = 50 Ω, Z_L = 2 kΩ)						
Circuit Current 2	$I_{CC}2$	No Signals	2.7	3.8	4.7	mA
IF Conversion gain	CG_{IF}	at maximum gain, $P_{1stIFin}$ = –50 dBm	37	40	43	dB
IF·SSB Noise Figure	NF_{IF}	at maximum gain, $P_{1stIFin}$ = –50 dBm	12	15	18	dB
Maximum 2ndIF Output Level	$P_{O(sat)IF}$	at maximum gain, $P_{1stIFin}$ = –20 dBm	–3	0	+3	dBm
Gain control voltage	V_{GC}	Voltage at maximum gain of CG_{IF}	–	–	1.0	V
Gain control range	D_{GC}	$P_{1stIFin}$ = –20 dBm	20	–	–	dB
2nd IF Amplifier (f_{2ndIF} = 1.023 MHz, Z_S = 50 Ω, Z_L = 2 kΩ)						
Circuit Current 3	$I_{CC}3$	No Signals	1.2	1.7	2.3	mA
Gain $\|S_{21}\|$	$\|S_{21}\|$	Z_L = 1 MΩ//27 pF[Note]	37	40	43	dB
Output Voltage Swing	$V_{2ndIFout}$	Z_L = 1 MΩ//27 pF[Note]	600	–	–	mV_{P-P}
PLL synthesizer block						
Circuit Current 4	$I_{CC}4$	PLL all block operating	16	22	33.6	mA
Phase comparing frequency	f_{PD}	PLL loop	8.8	9.207	9.4	MHz
Reference input minimum level	V_{REFin}	Z_L = 10 kΩ//20 pF[Note]	200	–	–	mV_{P-P}
Loop filter Output Level (H)	$V_{LP(H)}$		2.8	–	–	V
Loop filter Output Level (L)	$V_{LP(L)}$		–	–	0.4	V
Reference output swing	V_{REFout}	Z_L = 1 MΩ//27 pF[Note]	1.0	–	–	V_{P-P}

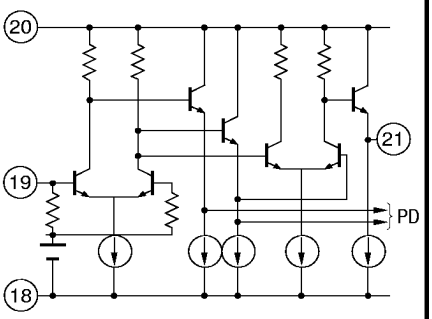
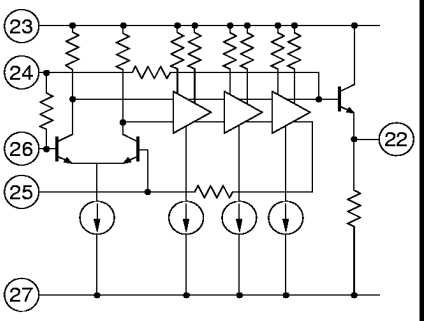
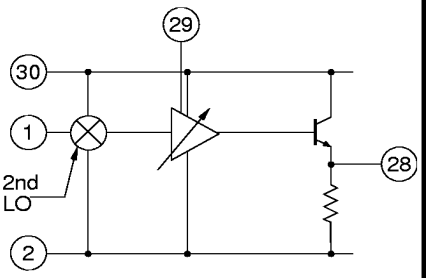
Note Impedance of measurement equipment

STANDARD CHARACTERISTICS (Unless otherwise specified T_A = +25 °C, V_{CC} = 3.0 V)

PARAMETERS	SYMBOL	CONDITIONS	REFERENCE	UNIT
RF Downconverter block ($P_{1stLOin}$ = –10 dBm, Z_L = Z_S = 50 Ω)				
LO leakage to IF pin	LO_{if}	$f_{1stLOin}$ = 1546.776 MHz	–30	dBm
LO leakage to RF pin	LOrf	$f_{1stLOin}$ = 1546.776 MHz	–30	dBm
Input 3rd order intercept point	IIP_3RF	$f_{RFin}1$ = 1600 MHz, $f_{RFin}2$ = 1605 MHz $f_{1stLOin}$ = 1570 MHz	–6	dBm
IF Downconverter block (1stLO oscillating, Z_S = 50 Ω, Z_L = 2 kΩ)				
LO leakage to 2nd IF	LO_{2ndif}	$f_{2ndLOin}$ = 27.621 MHz	–20	dBm
LO leakage to 1st IF	LO_{1stif}	$f_{2ndLOin}$ = 27.621 MHz	–40	dBm
Input 3rd order intercept point	IIP_3IF	$f_{1stIFin}1$ = 28.644 MHz, $f_{1stIFin}2$ = 28.744 MHz $f_{2ndLOin}$ = 27.621 MHz	–30	dBm

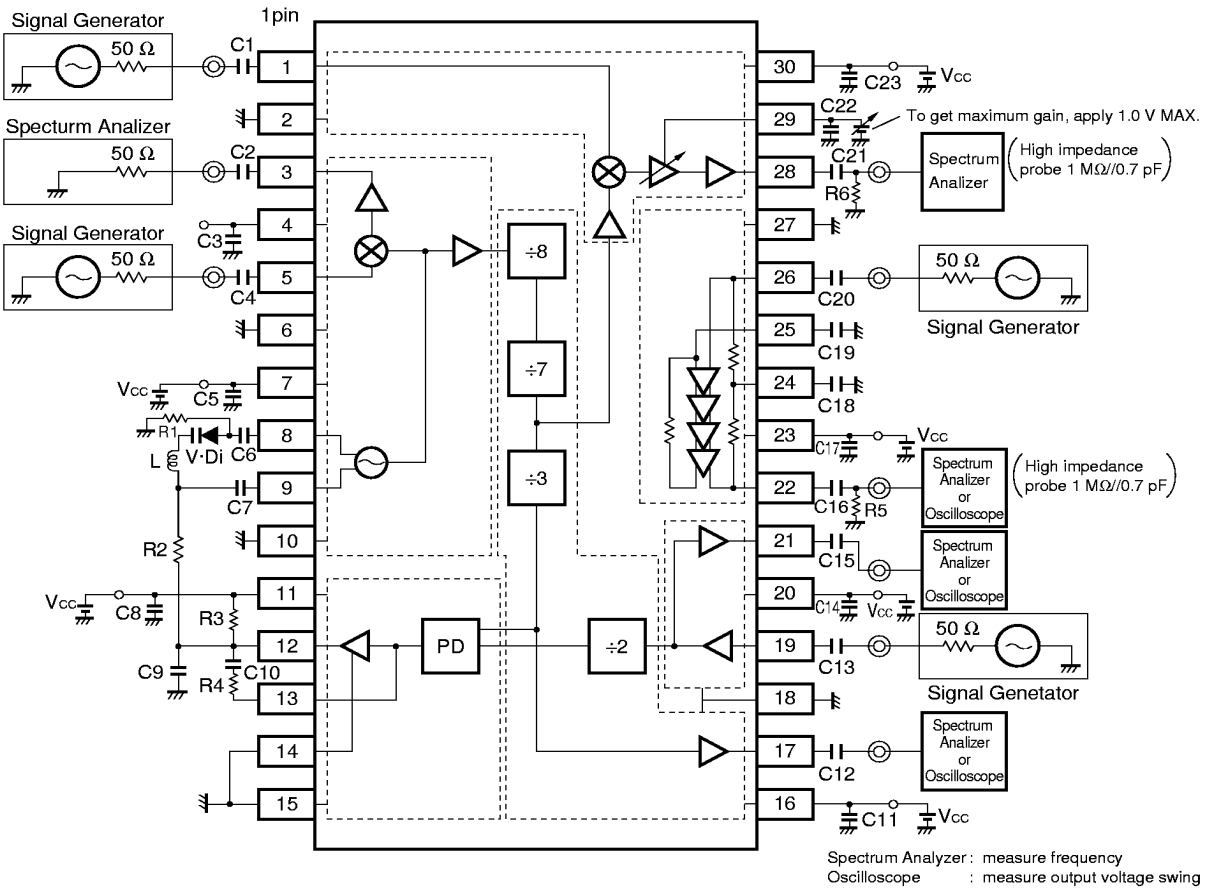
PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)	Function and Application	Internal Equivalent Circuit
3	RF-MIXout	–	1.68	Output pin of RF mixer. 1st IF filter must be inserted between pin 1 & 3.	
4	Vcc (RF-MIX)	2.7 to 3.3	–	Supply voltage pin of RF mixer block. This pin must be decoupled with capacitor (eg. 1 000 pF).	
5	RF-MIXin	–	1.20	Input pin of RF mixer. 1 575.42 MHz band pass filter must be inserted between pin 5 and external LNA.	
6	GND (RF-MIX)	0	–	Ground pin of RF mixer.	
7	Vcc (1stLO-OSC)	2.7 to 3.3	–	Supply voltage pin of differential amplifier for 1st LO oscillator circuit.	
8	1stLO-OSC1	–	1.75	Pin 8 & 9 are each base pin of differential amplifier for 1st LO oscillator. These pins should be equipped with LC and varactor to oscillate on 1546.776 MHz as VCO.	
9	1stLO-OSC2	–	1.75		
10	GND (1stLO-OSC)	0	–	Ground pin of differential amplifier for 1st LO oscillator circuit.	
11	Vcc (phase detector)	2.7 to 3.3	–	Supply voltage pin of phase detector and active loop filter.	
12	PD-Vout3	Pull-up with resistor	–	Pins of active loop filter for tuning voltage output. The active transistors configured with darlington pair are built on chip. Pin 14 should be pulled down with external resistor. Pin 12 to 13 should be equipped with external RC in order to adjust dumping factor and cutoff frequency. This tuning voltage output must be connected to varactor diode of 1st LO-OSC.	
13	PD-Vout2	–	Output in accordance with phase difference		
14	PD-Vout1	Pull-up with resistor			
15	GND (phase detector)	0	–	Ground pin of phase detector + active loop filter.	
16	Vcc (divider block)	2.7 to 3.3	–	Supply voltage pin of prescalers.	
17	LOout	–	1.98	Monitor pin of comparison frequency at phase detector.	
18	GND (divider block)	0	–	Ground pin of prescalers + LOout amplifier.	

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)	Function and Application	Internal Equivalent Circuit
19	REFin	–	1.97	Input pin of reference frequency. This pin should be equipped with external 18.414 MHz oscillator (e.g. TCXO).	
20	V_{CC} (reference block)	2.7 to 3.3	–	Supply voltage pin of input/output amplifiers in reference block.	
21	REFout	–	1.75	Output pin of reference frequency. The frequency from pin 19 can be took out as 1 V_{P-P} swing.	
22	2ndIFout	–	1.65	Output pin of 2nd IF amplifier. This pin output 1.023 MHz clipped sinewave. This pin should be equipped with external inverter to adjust level to next stage on user's system.	
23	V_{CC} (2ndIF-AMP)	2.7 to 3.3	–	Supply voltage pin of 2nd IF amplifier.	
24	2ndIF bypass	–	2.25	Bypass pin of 2nd IF amplifier input 1. This pin should be grounded through capacitor.	
25	2ndIFin2	–	2.25	Pin of 2nd IF amplifier input 2. This pin should be grounded through capacitor.	
26	2ndIFin1	–	2.25	Pin of 2nd IF amplifier input 1. 28.644 MHz IF filter can be inserted between pin 26 & 28.	
27	GND (2ndIF-AMP)	0	–	Ground pin of 2nd IF amplifier.	
28	IF-MIXout	–	1.80	Output pin from IF mixer. IF mixer output signal goes through gain control amplifier before this emitter follower output port.	
29	V_{GC} (IF-MIX)	0 to 3.3	–	Gain control voltage pin of IF mixer output amplifier. This voltage performs forward control (V_{GC} up → Gain down).	
30	V_{CC} (IF-MIX)	2.7 to 3.3	–	Supply voltage pin of IF mixer, gain control amplifier and emitter follower transistor.	
1	IF-MIXin	–	1.18	Input pin of IF mixer.	
2	GND (IF-MIX)	0	–	Ground pin of IF mixer.	

Note Ground pattern on the board must be formed as wide as possible to minimize ground impedance.

TEST CIRCUIT

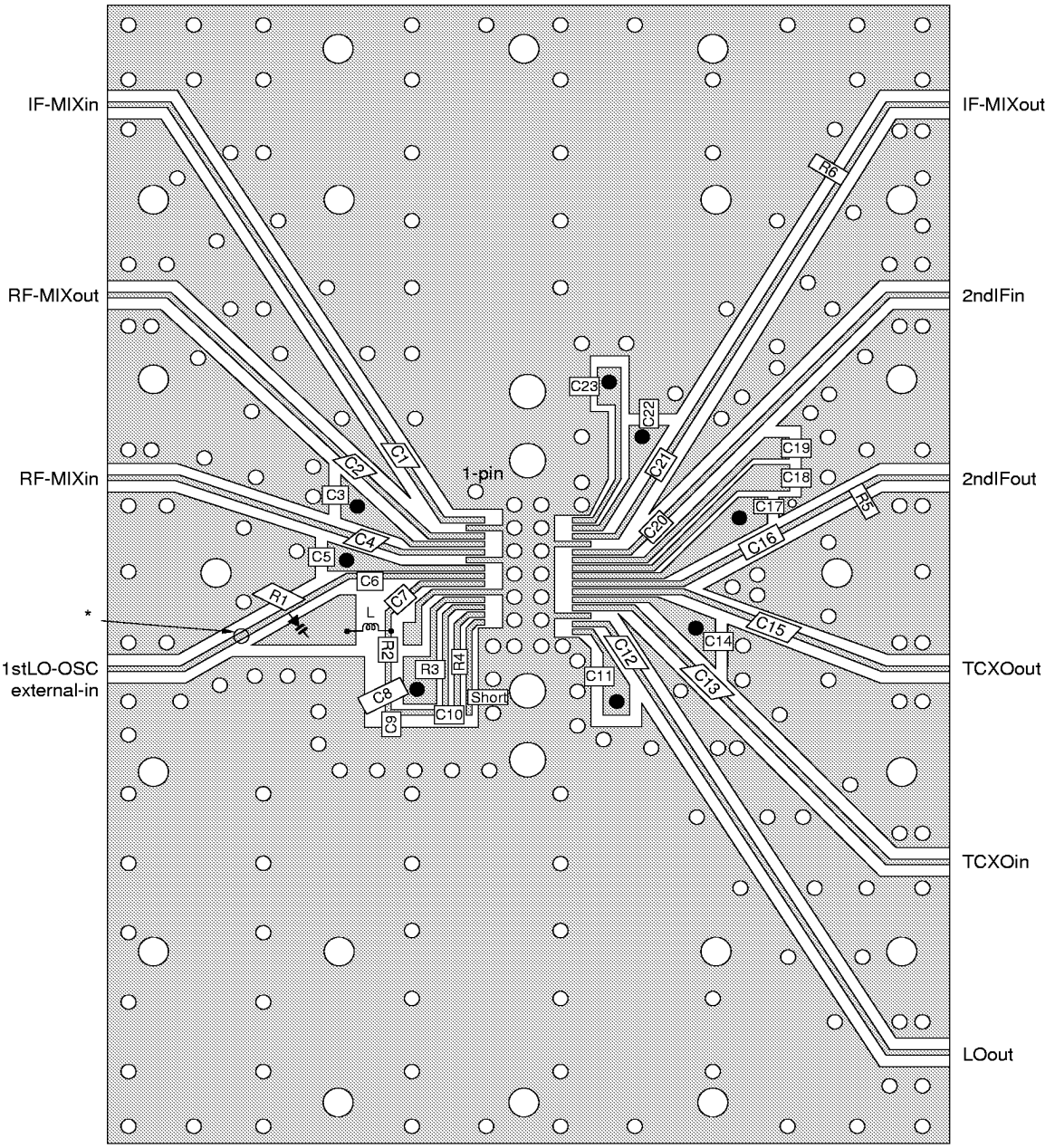


COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C1 to C5, C8, C11 to C15, C17, C18, C22, C23	1000 pF
	C6, C7	24 pF (UJ)
	C9	1800 pF
	C19	9900 pF
	C10	33 nF
Ceramic capacitor	C16, C20	0.1 μF
	C21	0.01 μF
Chip resistor	R1, R2	4.7 kΩ
	R3	6.2 kΩ
	R4	6.8 kΩ
	R5, R6	2 kΩ
Varactor Diode	V•Di	1SV210SS *
Chip inductor	L	3.3 nH

*ATTENTION NEC discontinues all the varactor diode products. Please contact the other company to buy varactor diode compatible to 1SV210SS.

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



Notes 1. 35 μm thick double-sided copper clad 63 × 100 × 0.4 mm polyimide board

2. Back side: GND pattern

3. ○ : Through holes

4. ● : Points for supplying voltage

5. *→ : In the case of internal oscillation, remove this point.

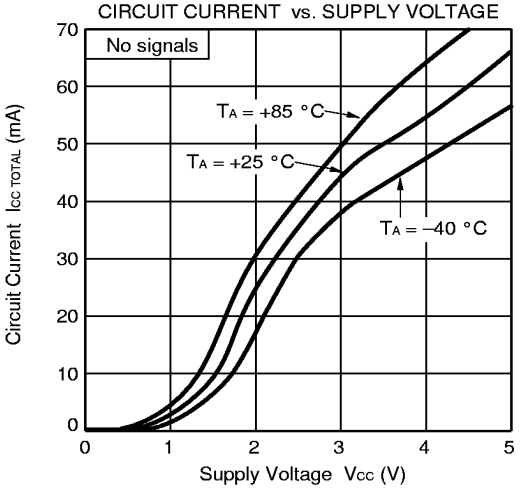
TEST CIRCUIT and print pattern in this sheet is for testing characteristics of IC. They are not an application circuit or recommended system circuit.

For application circuits, please refer to Application note of μPB1003GS and μPB1004GS. (Document No. P11977E)

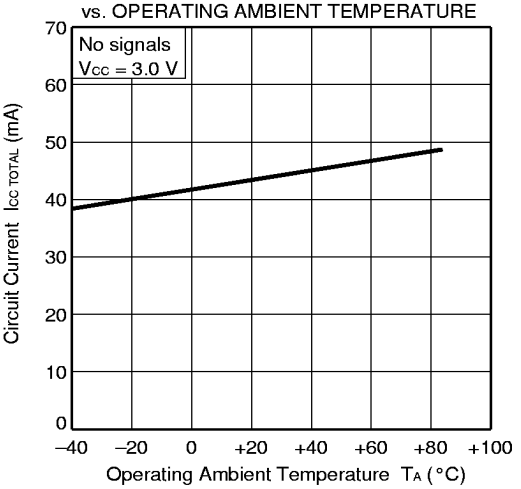
CHARACTERISTIC CURVES (T_A = +25 °C, V_{CC} = 3.0 V unless otherwise specified)

IC total

CIRCUIT CURRENT vs. SUPPLY VOLTAGE

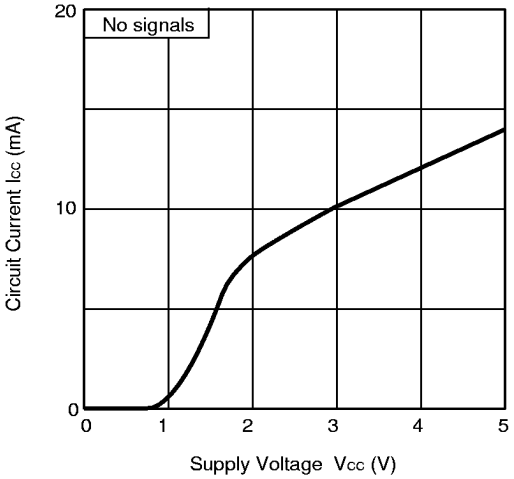


CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE

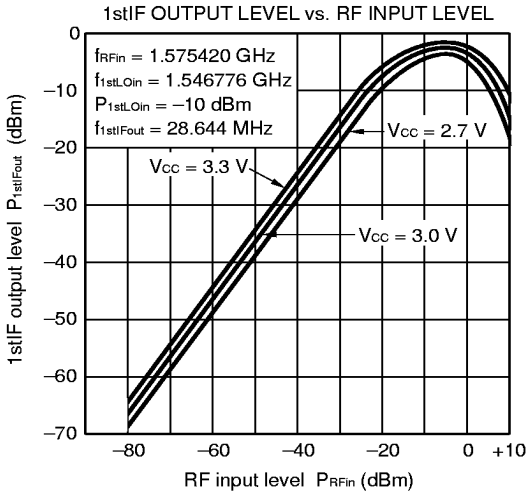


RF frequency downconverter block

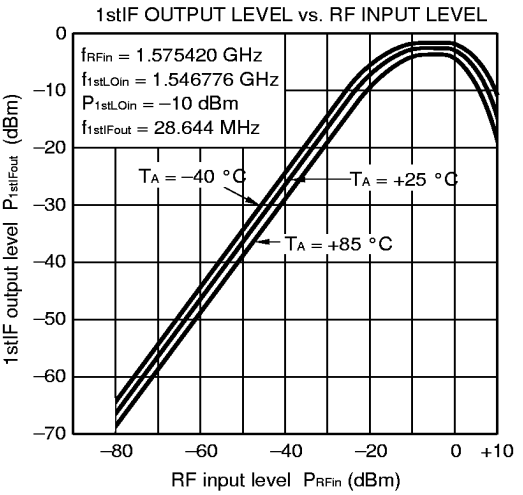
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



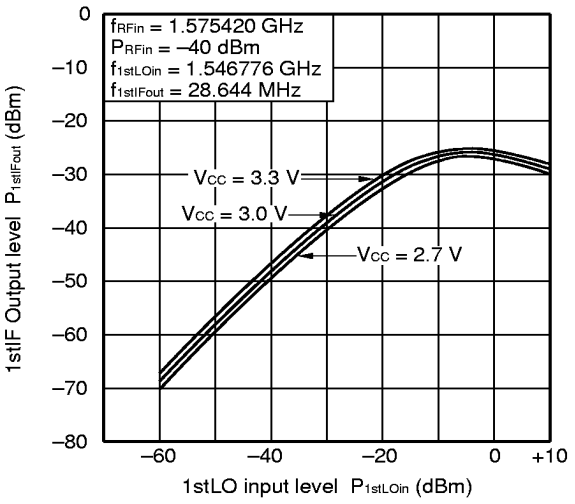
1stIF OUTPUT LEVEL vs. RF INPUT LEVEL



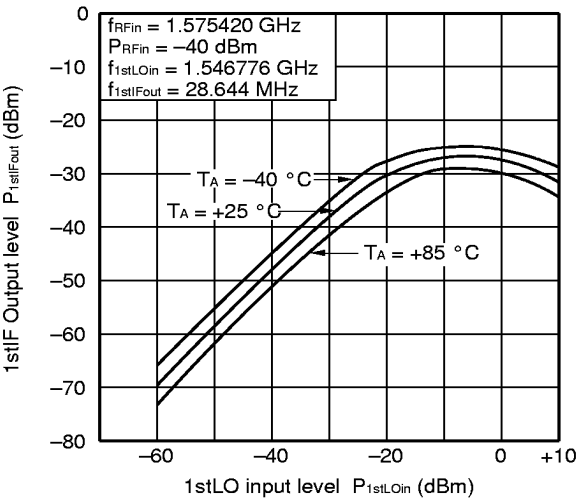
1stIF OUTPUT LEVEL vs. RF INPUT LEVEL



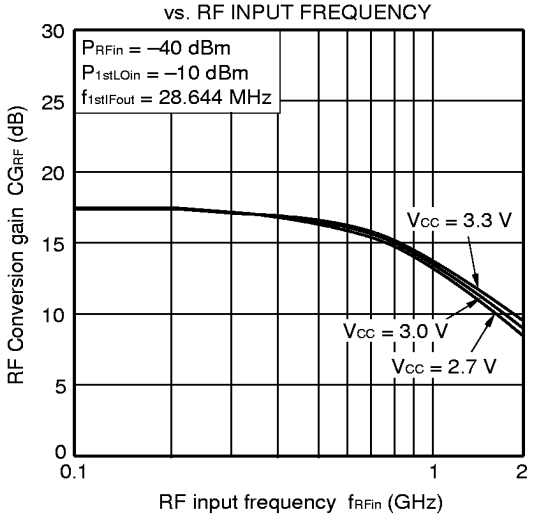
1stIF OUTPUT LEVEL
vs. 1stLOCAL INPUT LEVEL



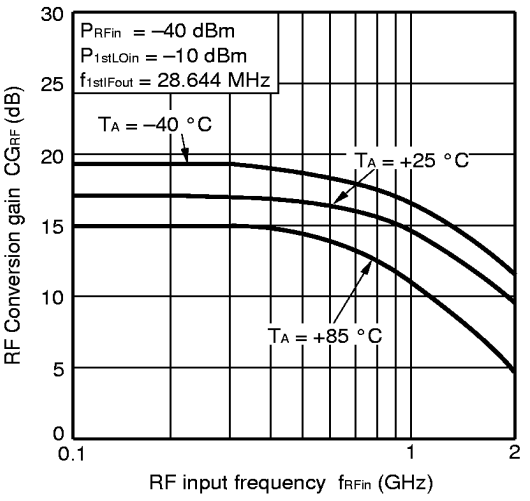
1stIF OUTPUT LEVEL
vs. 1stLOCAL INPUT LEVEL



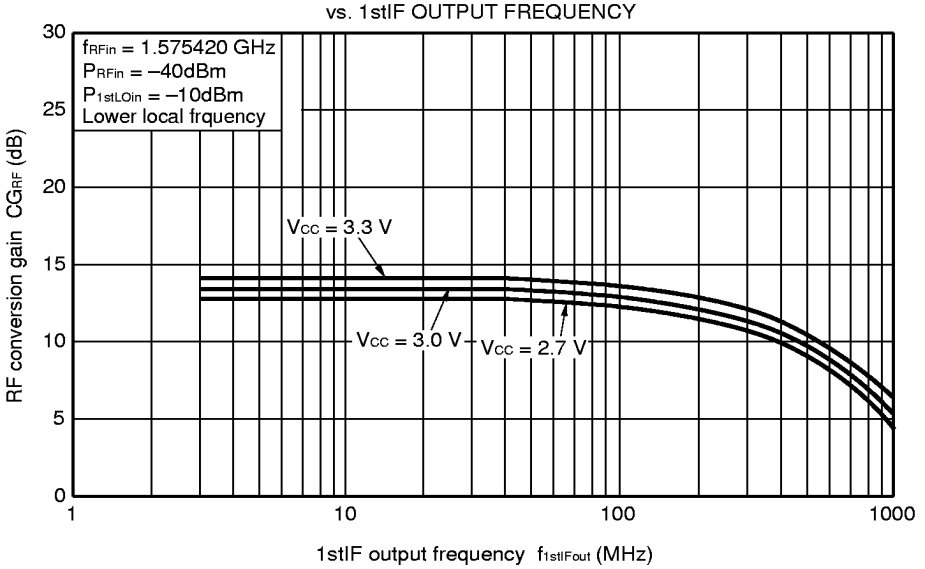
RF CONVERSION GAIN
vs. RF INPUT FREQUENCY



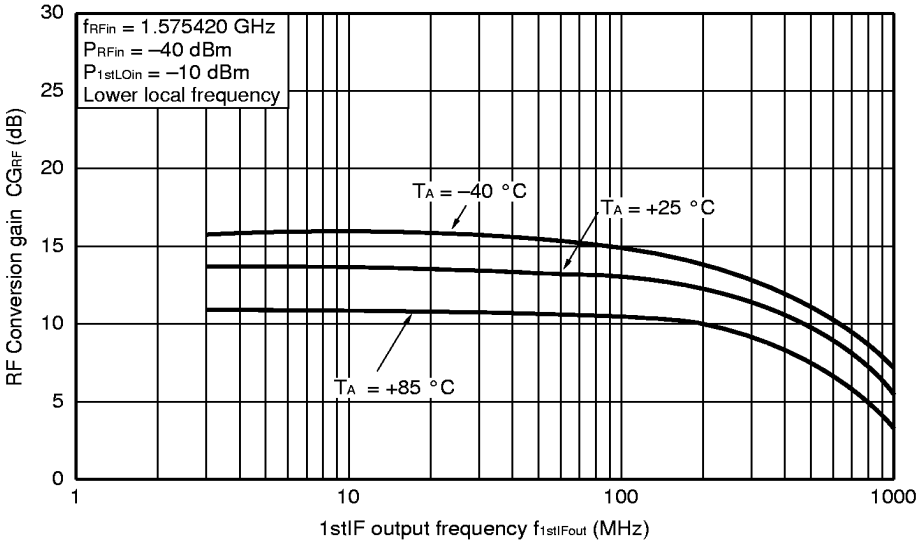
RF CONVERSION GAIN
vs. RF INPUT FREQUENCY



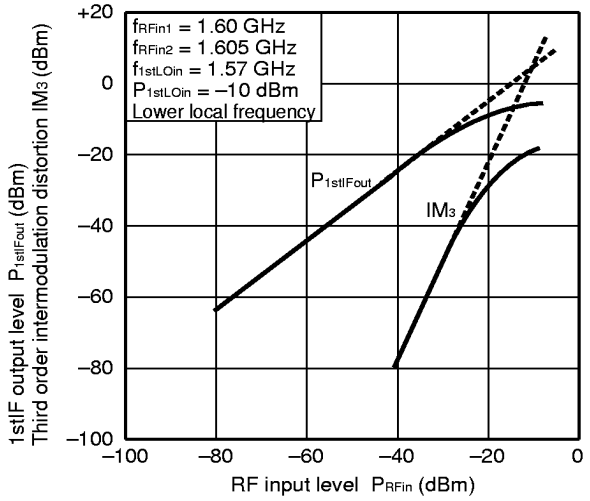
RF CONVERSION GAIN
vs. 1stIF OUTPUT FREQUENCY



RF CONVERSION GAIN
vs. 1stIF OUTPUT FREQUENCY

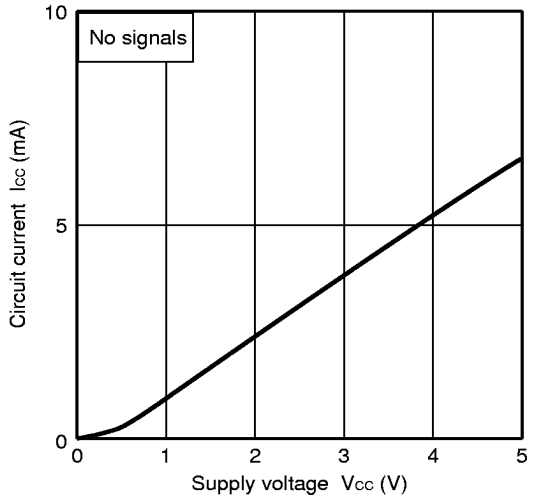


IM3 AND 1stIF OUTPUT LEVEL
vs. RF INPUT LEVEL

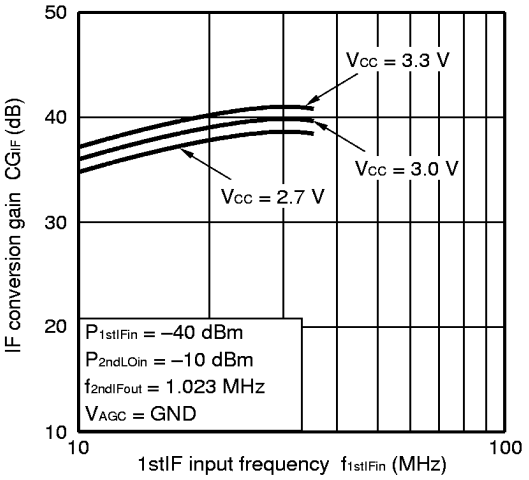


—— IF frequency downconverter block ——

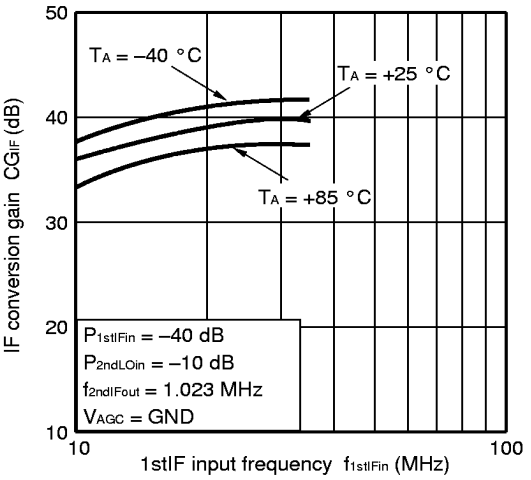
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



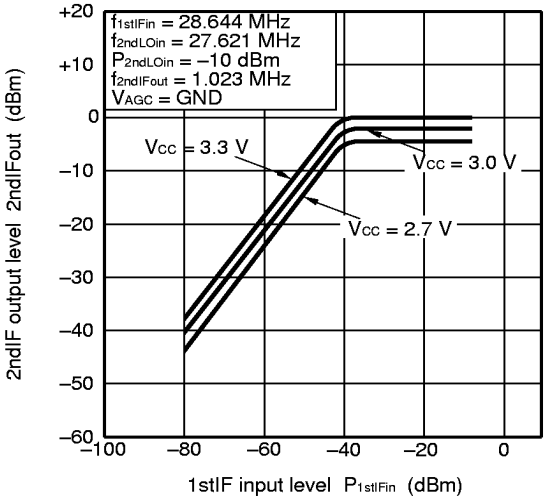
IF CONVERSION GAIN
vs. 1stIF INPUT FREQUENCY



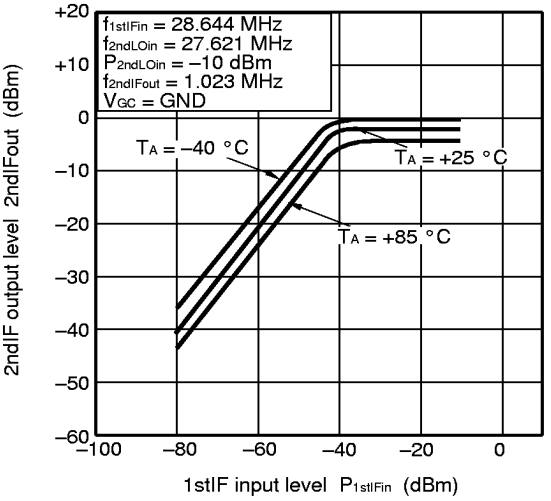
IF CONVERSION GAIN
vs. 1stIF INPUT FREQUENCY



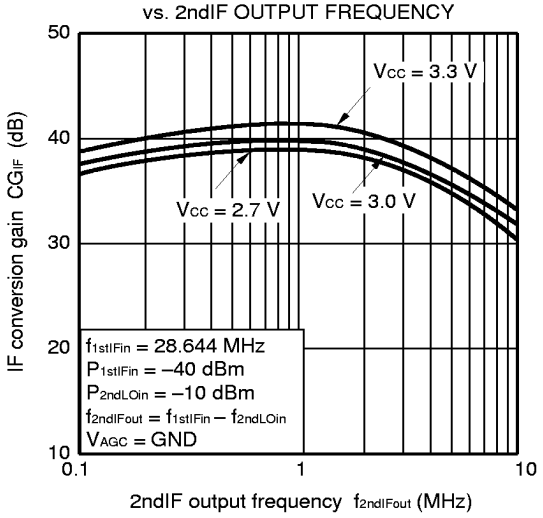
2ndIF OUTPUT LEVEL
vs. 1stIF INPUT LEVEL



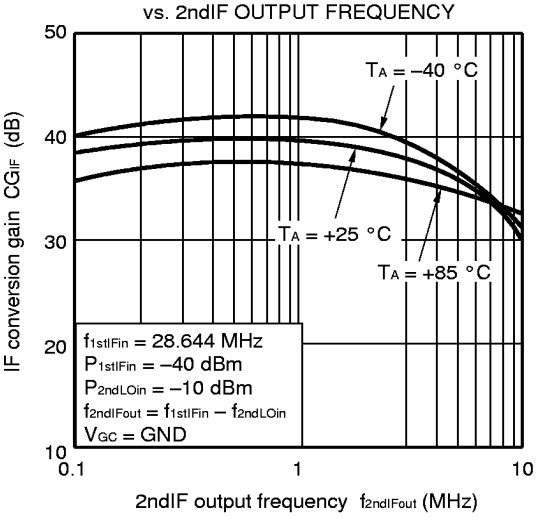
2ndIF OUTPUT LEVEL
vs. 1stIF INPUT LEVEL



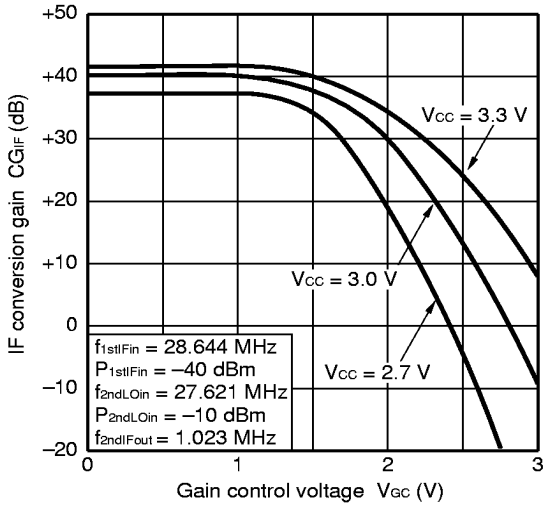
IF CONVERSION GAIN
vs. 2ndIF OUTPUT FREQUENCY



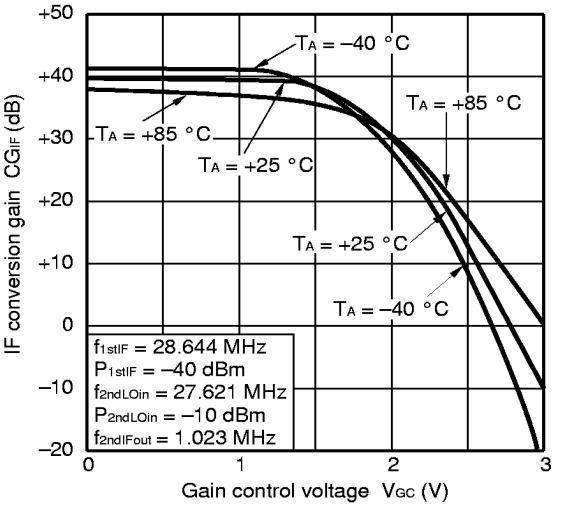
IF CONVERSION GAIN
vs. 2ndIF OUTPUT FREQUENCY



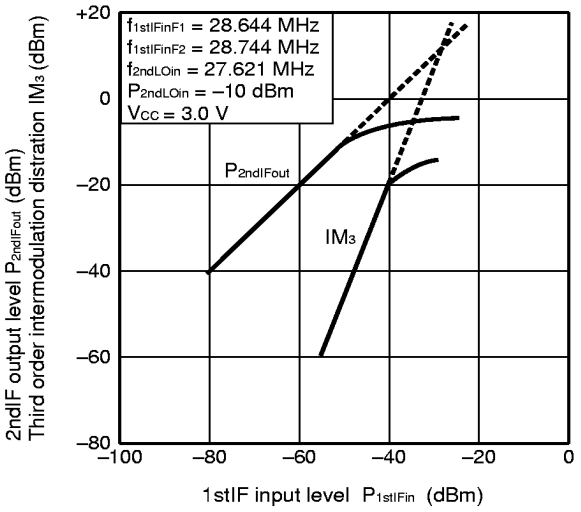
IF CONVERSION GAIN vs. GAIN CONTROL



IF CONVERSION GAIN vs. GAIN CONTROL

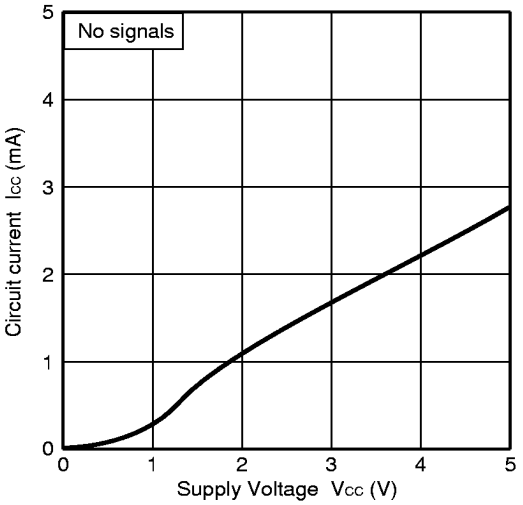


IM3 AND 2ndIF OUTPUT LEVEL vs. 1stIF INPUT LEVEL

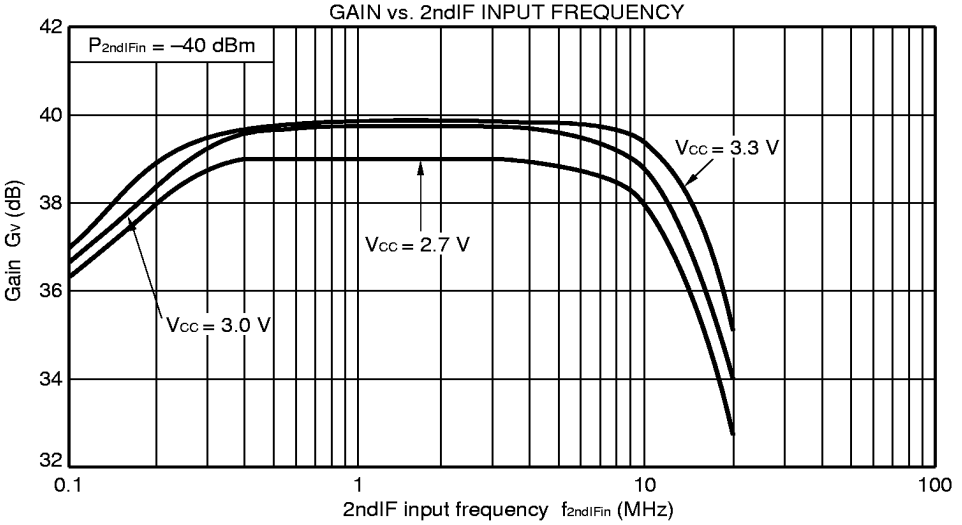


2ndIF amplifier block

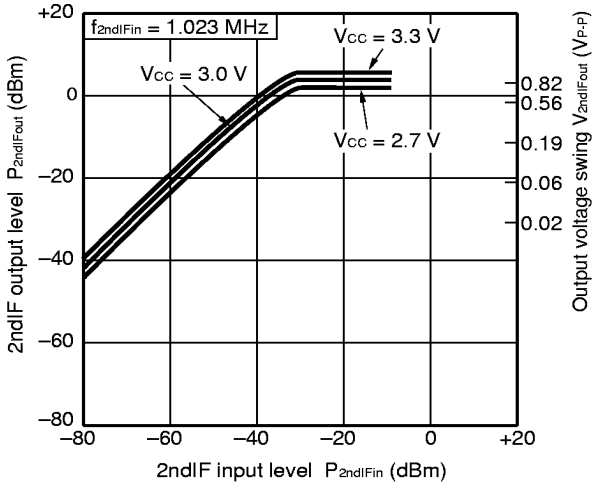
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



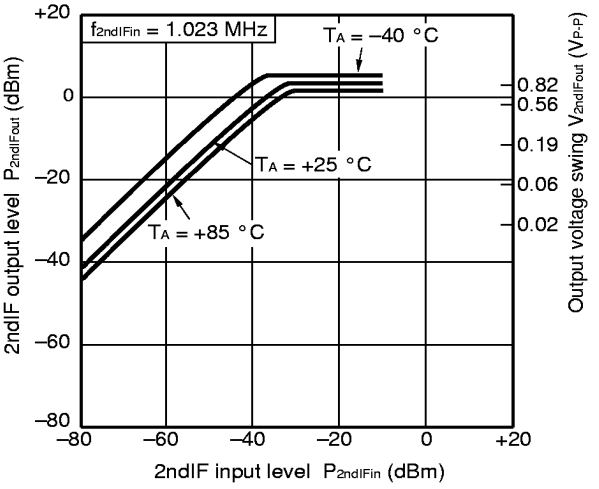
GAIN vs. 2ndIF INPUT FREQUENCY



2ndIF OUTPUT POWER LEVEL AND OUTPUT VOLTAGE SWING vs. 2ndIF INPUT LEVEL

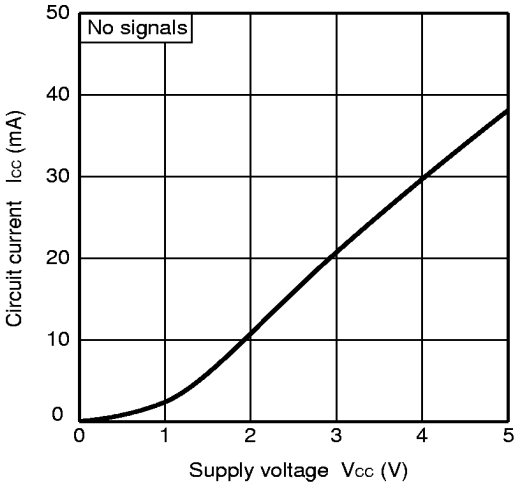


2ndIF OUTPUT POWER LEVEL AND OUTPUT VOLTAGE SWING vs. 2ndIF INPUT LEVEL

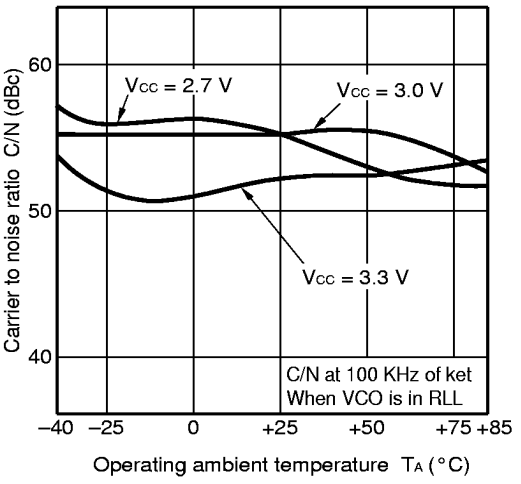


PLL frequency synthesizer block

CIRCUIT CURRENT vs. SUPPLY VOLTAGE

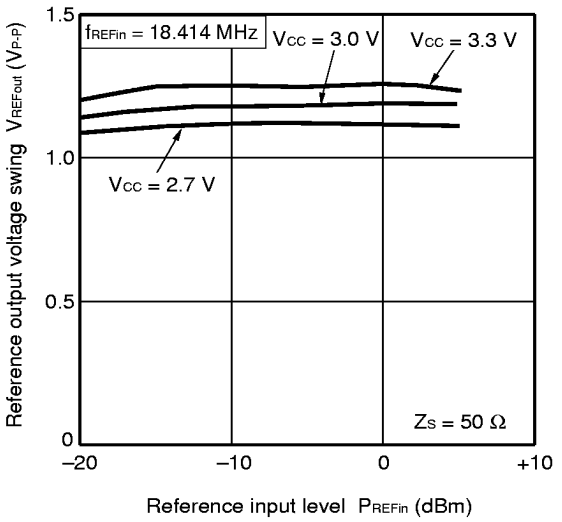


VCO CARRIER TO NOISE RATIO vs. OPERATING AMBIENT TEMPERATURE

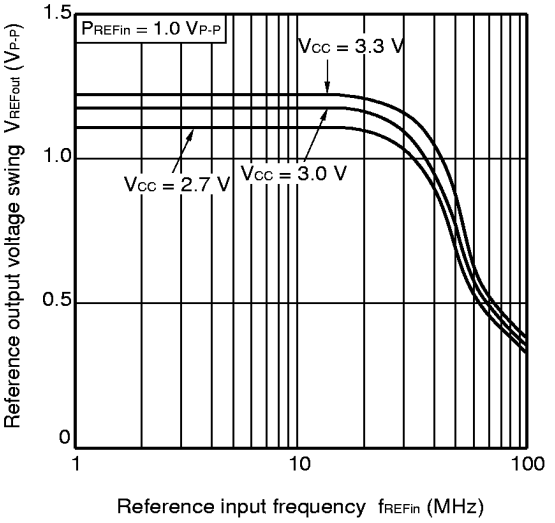


—— Reference block ——

REFERENCE OUTPUT VOLTAGE SWING VS. REFERENCE INPUT LEVEL

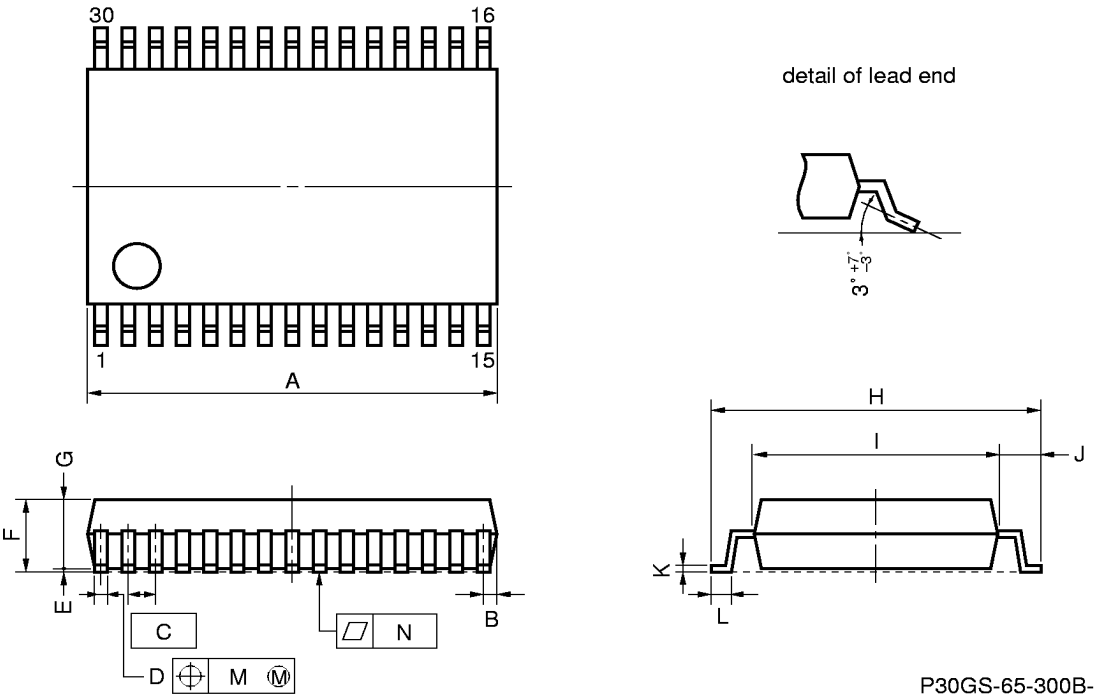


REFERENCE OUTPUT VOLTAGE SWING VS. REFERENCE INPUT FREQUENCY



PACKAGE DIMENSIONS

30 PIN PLASTIC SHRINK SSOP (300 mil)



P30GS-65-300B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.11 MAX.	0.398 MAX.
B	0.51 MAX.	0.020 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	$0.30^{+0.10}_{-0.05}$	$0.012^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	8.1±0.2	0.319±0.008
I	6.1±0.2	0.240±0.008
J	1.0 ± 0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004

NOTE CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
(3) Keep the wiring length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.
(5) Frequency signal input/output pins must be each coupled with capacitor (e.g. 1 000 pF) for DC cut.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPB1003GS

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 3 times, Limited days: no.*	IR35-00-3
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 3 times, Limited days: no.*	VP15-00-3
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s/pin. Limited days: no.*	

* It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Caution The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).