Z8340 Low Power Z80®L SIO Serial Input/Output

Zilog

AC and DC Characteristics

March 1985

ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND . . . . . −0.3V to +7.0V
Operating Ambient Temperature . . . . . See Ordering Information
Storage Temperature . . . . . −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

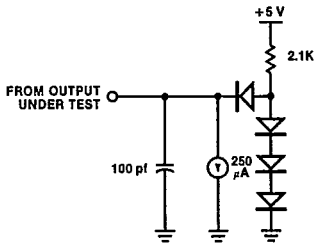
STANDARD TEST CONDITIONS

The DC characteristics listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:

- S = 0°C to +70°C, +4.75V ≤ V_{CC} ≤ +5.25V

The Ordering Information section lists package temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

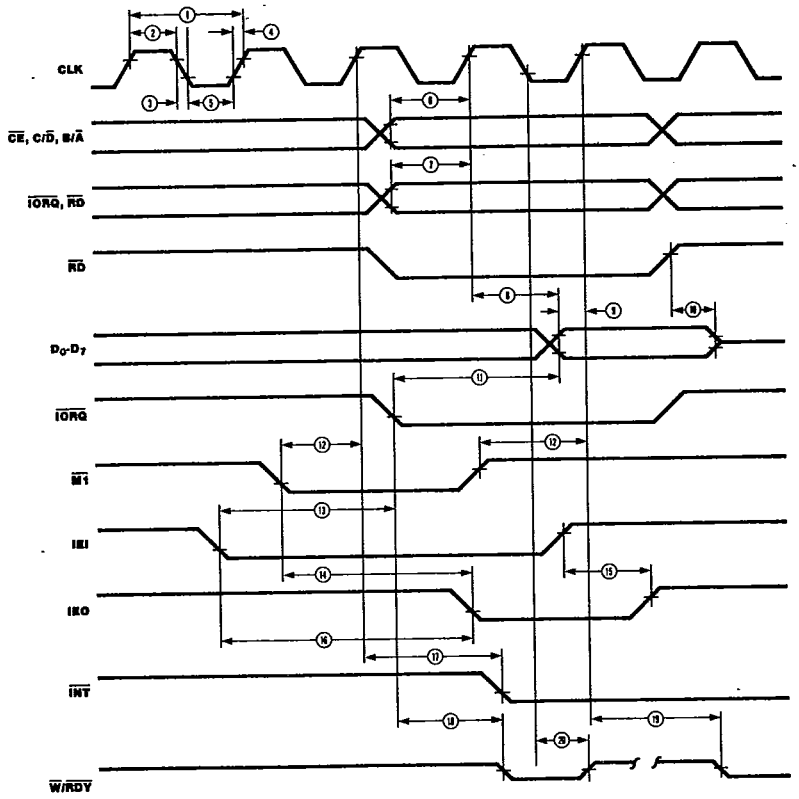


DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Typical	Unit	Condition
V_{ILC}	Clock Input Low Voltage	−0.3	+0.45		V	
V_{IHC}	Clock Input High Voltage	V_{CC} −0.6	V_{CC} +0.3		V	
V_{IL}	Input Low Voltage	−0.3	+0.8		V	
V_{IH}	Input High Voltage	+2.0	V_{CC}		V	
V_{OL}	Output Low Voltage		+0.4		V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4			V	I_{OH} = −250 µA
I_{LI}	Input Leakage Current		±10		µA	V_{IN} = 0 to V_{CC}
I_{LO}	3-State Output Leakage Current in Float		±10		µA	V_{OUT} = 0.4 to V_{CC}
$I_{L(SY)}$	SYNC Pin Leakage Current		+10/−40		µA	V_{IN} = 0 to V_{CC}
I_{CC}	Power Supply Current		30	20	mA	

Over specified temperature and voltage range.

AC CHARACTERISTICS

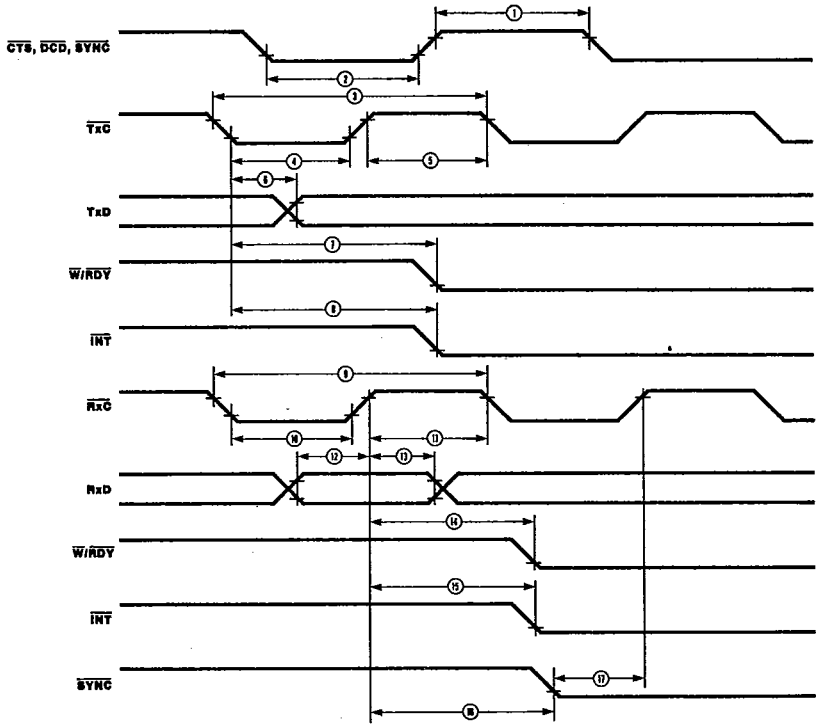


AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	Z8340-1† (1.0 MHz) Min	Z8340-1† (1.0 MHz) Max	Z8340-3† (2.5 MHz) Min	Z8340-3† (2.5 MHz) Max
1	TcC	Clock Cycle Time	1000	4000	400	4000
2	TwCh	Clock Width (High)	470	2000	170	2000
3	TfC	Clock Fall Time		30		30
4	TrC	Clock Rise Time		30		30
5	TwCl	Clock Width (Low)	470	2000	170	2000
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	410		160	
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup time	610		240	
8	TdC(DO)	Clock ↑ to Data Out Delay		610		240
9	TsDI(C)	Data In to Clock ↑ Setup (Write or $\overline{M1}$ Cycle)	140		50	
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		590		230
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		860		340
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	540		210	
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	510		200	
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before $\overline{M1}$)		760		300
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		380		150
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		380		150
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		510		200
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W}$/$\overline{RDY}$ ↓ Delay (Wait Mode)		760		300
19	TdC(W/RR)	Clock ↑ to $\overline{W}$/$\overline{RDY}$ ↓ Delay (Ready Mode)		310		120
20	TdC(W/RWz)	Clock ↓ to $\overline{W}$/$\overline{RDY}$ Float Delay (Wait Mode)		390		150
21	Th	Any unspecified Hold when Setup is specified	0		0	

† Units are nanoseconds unless otherwise specified;
timings are preliminary and subject to change.

AC CHARACTERISTICS (Continued)



Number	Symbol	Parameter	Z8340-1† (1.0 MHz) Min	Max	Z8340-3† (2.5 MHz) Min	Max	Notes
1	TwPh	Pulse Width (High)	500		200		
2	TwPl	Pulse Width (Low)	500		200		
3	TcTxC	$\overline{TxC}$ Cycle Time	1000	∞	400	∞	
4	TwTxCl	$\overline{TxC}$ Width (Low)	460	∞	180	∞	
5	TwTxCh	$\overline{TxC}$ Width (High)	460	∞	180	∞	
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		1000		400	
7	TdTxC(W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	Clk Periods*
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods*
9	TcRxC	$\overline{RxC}$ Cycle Time	1000	∞	400	∞	
10	TwRxCl	$\overline{RxC}$ Width (Low)	460	∞	180	∞	
11	TwRxCh	$\overline{RxC}$ Width (High)	460	∞	180	∞	
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		
13	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD Hold Time (x1 Mode)	360		140		
14	TdRxC(W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	Clk Periods*
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	Clk Periods*
16	TdRxC(SYNC)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4	7	4	7	Clk Periods*
17	TsSYNC(RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	100		100		

In all modes, the System clock rate must be at least five times the maximum data rate.
$\overline{RESET}$ must be active a minimum of one complete Clock Cycle.

* System Clock
† Units are nanoseconds unless otherwise specified; timings are preliminary and subject to change.

ORDERING INFORMATION

Z80L SIO, 1.0 MHz
40-pin DIP
Z8340-1 PS

Z80L SIO, 2.5 MHz
40-pin DIP
Z8340-3 PS

Codes
First letter is for package; second letter is for temperature.

C = Ceramic DIP
P = Plastic DIP
L = Ceramic LCC
V = Plastic PCC

R = Protopack
T = Low Profile Protopack
DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
PCC = Plastic Chip Carrier (Leaded)

TEMPERATURE
S = 0°C to +70°C
E = −40°C to +85°C
M*= −55°C to +125°C

FLOW
B = 883 Class B

†Available soon.
*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.