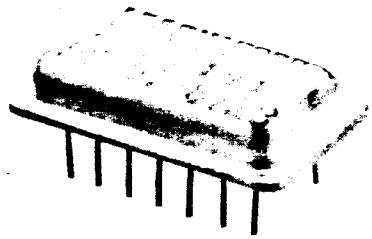
LEACH®
CONTROL PRODUCTS DIVISION

Single Line Driver
Model CSH-191

CSH-191



Description

The CSH-191 is a single channel, Tristate line driver, used on balanced lines to provide a digital interface circuit operating up to 10Mb/sec. Designed to meet the type III requirements in MIL-STD-188-114A, as well as the switching/load characteristics of EIA Standard RS-485. The device has high-current capability for driving balance lines such as twisted pairs, co-axial, or parallel-wire transmission lines, and provides a high impedance state. The device is ideal for use in secured audio, data, video communications networks and equipment applications.

Features

- Fast switching characteristics
  - 10ns rise and fall time
  - 15ns propagation delay
- +/ – 7V common mode range
- Dual +/– 5Vdc power supply operation
- High output impedance in power off condition or $\overline{OE}$ High
- TTL, ECL, compatible
- 100% screened to MIL-STD-883
- Compatible with LEACH family of Line Receivers

TRUTH TABLE

Inputs		Outputs	
$\overline{OE}$	DIN	Q	$\overline{Q}$
H	X	Z	Z
L	L	L	H
L	H	H	L

INPUTS: H > = VINH; L < = VINL; X = DON'T CARE

OUTPUTS: Z = HIGH IMPEDANCE; L < = – 1.0V; H > = 1.0V

ABSOLUTE MAXIMUM RATINGS AND FUNCTIONAL OPERATING LIMITS

Parameter	Absolute Limits Min	Absolute Limits Max	Operating Limits Min	Operating Limits Max	Units
– V (Negative Supply)	0	– 7	– 4.50	– 5.50	Volts
+ V (Positive Supply)	0	7	4.50	5.50	Volts
Vin (Input Voltage)	– 0.5	7.0	2.0	Vcc	Volts
fin (Input Frequency)	DC	100	0	25	Mhz
Ambient Temp. Range	– 65	+ 150	– 55	+ 125	°C

ELECTRICAL CHARACTERISTICS—STATIC

Parameter	Test Conditions (Note 1) Input Pins DIN	Input Pins OE	Power Supplies Pos	Power Supplies Neg	Limits Min	Limits Max	Units	Notes
Logic High Input Current (I_{IH})	2.4V	2.4V	4.5V	–4.5V	—	40	µA	2
Logic Low Input Current (I_{IL})	0.4V	0.4V	5.5V	–5.5V	—	–1	mA	2
Input Leakage (I_L)	5.5V	5.5V	5.5V	–5.5V	—	100	µA	2
Open Circuit Output Voltage (Vo)	2.0V / 0.8V	.08V / 0.8V	5.5V	–5.5V		I6.0I	V	2
Terminated Output Voltage (Vt)	0.8V / 0.8V	2.0V / 0.8V	4.5V	–4.5V	I2.5I	I6.0I	V	2
Vt Balance	—	—	—	—	—	I0.4I	V	2
Terminated Output Offset Voltage (Vos)	2.0V / 0.8V	0.8V / 2.0V	5.5V	–5.5V	—	I0.4I	V	2
Vos Balance	—	—	—	—	—	I0.4I	V	2 & 3
High Impedance Output Current (Ioz)	2.0V / 0.8V	2.0V / 2.0V	4.5V	–4.5V	–100	100	µA	2
Short Circuit Output Current (I_S)	2.0V / 0.8V	0.8V / 0.8V	5.5V	–5.5V	–150	150	mA	2
Power Off Output Current (Ix)	—	—	Gnd	Gnd	–100	100	µA	2
Positive Power Supply Current	5	5	5.5V	–5.5V		100	mA	2 & 5
Negative Power Supply Current	5	5	5.5V	–5.5V		100	mA	2 & 5
Output Drive	—	—	5.5V	–5.5V	25	50	mA	2 & 5

ELECTRICAL CHARACTERISTICS—SWITCHING (DYNAMIC)

Parameter	Power Supplies Pos	Power Supplies Neg	Limits Min	Limits Max	Units	Notes
Propagation Delay Time Enable (tpd$\overline{OE}$)	5.0V	–5.0V	—	15	nS	2
Output Rise Time (tr)	5.0V	–5.0V	—	10	nS	2
Output Fall Time (tf)	5.0V	–5.0V	—	10	nS	2
Propagation Delay Time Data (tpdD)	5.0V	–5.0V	—	15	nS	2

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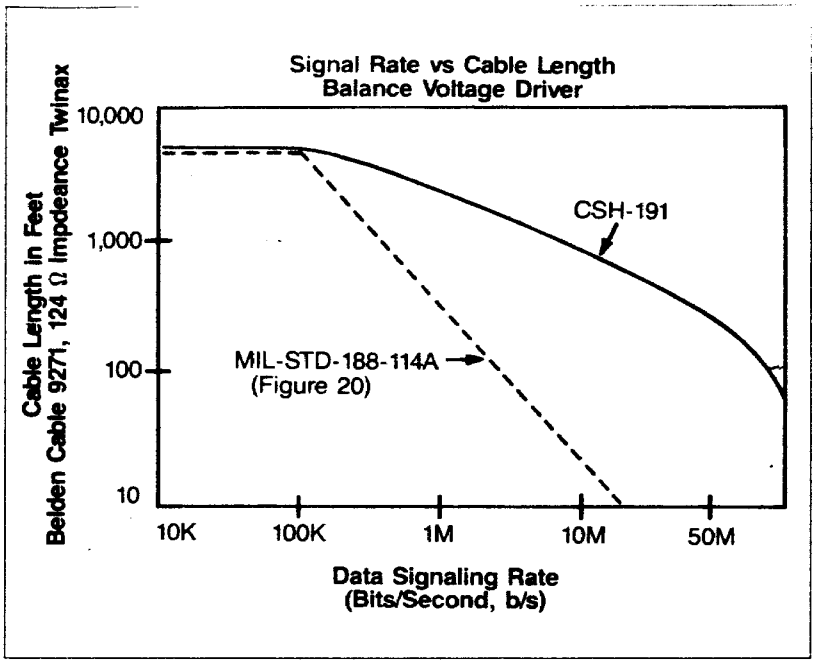
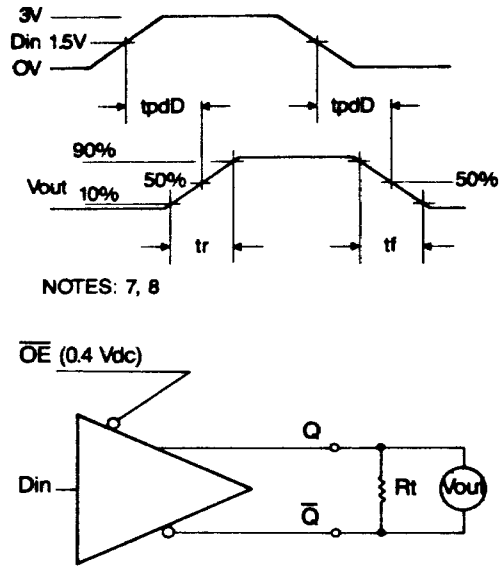
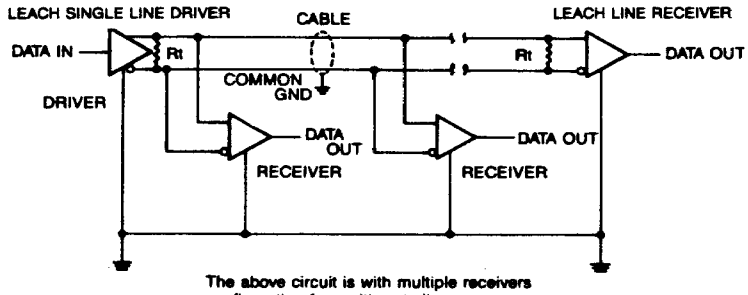


Input to Output Propagation Delay



NOTES: 7, 8

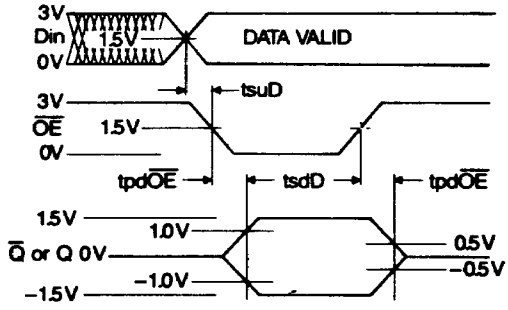
Typical Application



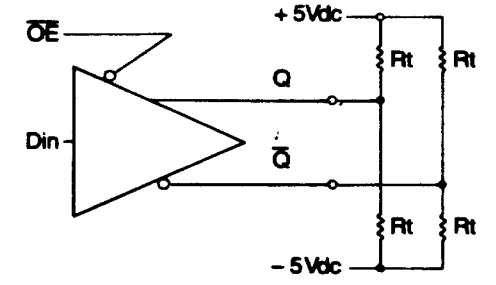
The above circuit is with multiple receivers configuration for multi-party lines.

NOTE: 6

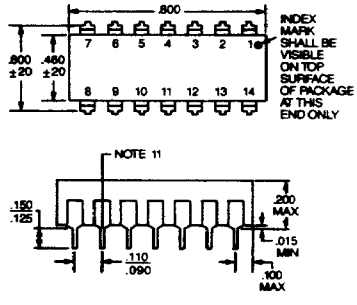
Output Enable Switching Times and Waveform Test Circuit

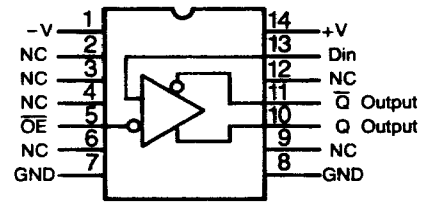


NOTES: 9, 10



Package Outline and Pin Connect





TOP VIEW

(Pins 2, 3, 4, 6, 9, 12, have no internal connection)

NOTES:

1. Unless otherwise specified, pins 7 and 8 shall be grounded. All voltages are specified with respect to ground. Currents entering a pin are specified as positive and currents out of a pin are specified as negative, and test conditions annotated by A — shall be open circuited.
2. Unless otherwise specified, minimum and maximums apply to the absolute value and the sign indicates polarity of voltage or current flow as specified in note 1
3. Output voltage balance shall be calculated from measured values V as follows: V Balance = ‖ V† ‖ − ‖ $\overline{V†}$ ‖
4. Output voltage offset shall be calculated from measured values of Vo as follows: Vo Balance = | Vos | − | $\overline{Vos}$ |
5. Power supply current shall be measured with a 100 ohm ± 10% resistor between the Q & $\overline{Q}$ pins and a 0 to 15 MHz (0 to 5 volt) square wave input to the DIN pins while the enable pin of each channel is separately brought low.
6. The terminated resistance should be carefully calculated for multi-party lines. Rt is proportional and in most cases equal to the characteristic impedance of the line.
7. For Din, tr = tf (10% to 90% points) ≤ 6.0 ns. Test frequency = 15 MHz.
8. Rt = Characteristic impedance of transmission line +/−10%.
9. For $\overline{OE}$, tr = tf (10% to 90% points) ≤ 6.0 ns. Test frequency ≤ 10 KHz.
10. Rt = Characteristic impedance of transmission line +/−10%.
11. Terminals shall be symmetrical about center line

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