

August 1997

Low Resistance, Single 8-Channel, and Differential 4-Channel, CMOS Analog Multiplexers

Features

- Signal Range+15V
- "ON" Resistance250Ω
- Input Leakage (Max)50nA
- Access Time350ns
- Power Consumption5mW
- DTL/TTL Compatible Address
- Operation-55°C to 125°C

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

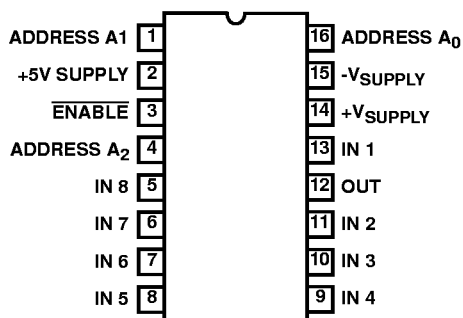
The HI-1818A and HI-1828A are monolithic, high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended, 8-Channel multiplexer, while the HI-1828A is a differential 4-Channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

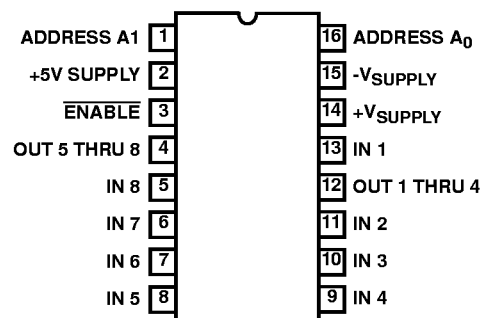
For MIL-STD-883 compliant parts, request the HI-1818A/883; HI-1828A/883 data sheet.

Pinouts

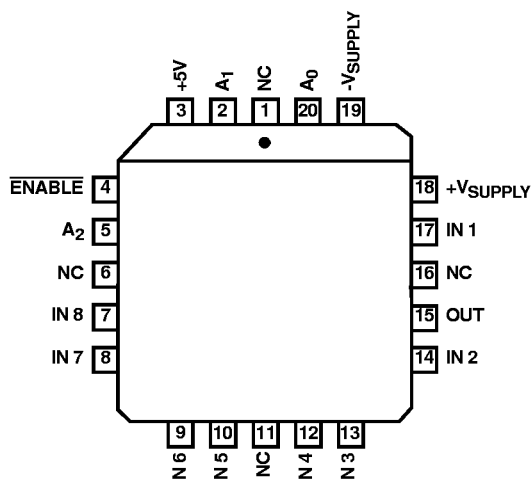
HI-1818A (CERDIP, PDIP)
TOP VIEW



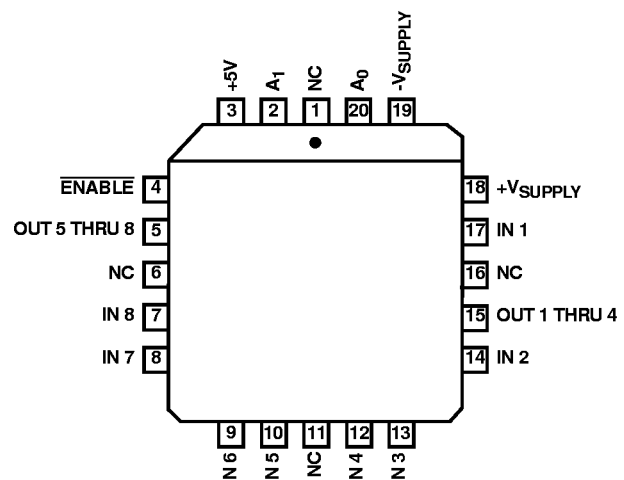
HI-1828A (CERDIP, PDIP)
TOP VIEW



HI-1818A (PLCC)
TOP VIEW



HI-1828A (CLCC, PLCC)
TOP VIEW



HI-1818A, HI1828A

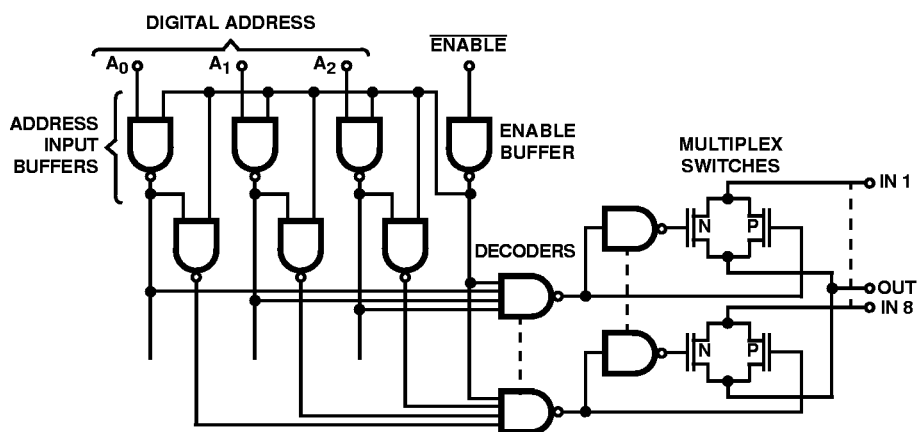
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI3-1818A-5	0 to 75	16 Ld PDIP	E16.3
HI1-1818A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-1818A-5	0 to 75	16 Ld CERDIP	F16.3
HI4P1818A-5	0 to 75	20 Ld PLCC	N20.35
HI1-1818A/883	-55 to 125	16 Ld CERDIP	F16.3
HI1-1828A-5	0 to 75	16 Ld CERDIP	F16.3

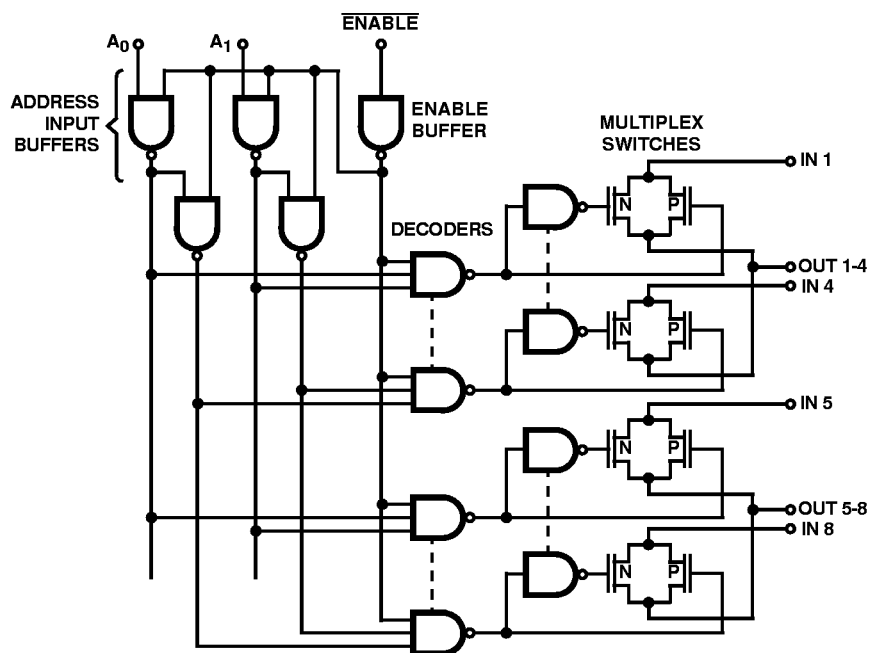
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-1828A-7	0 to 75 + 96 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-1828A-5	0 to 75	16 Ld PDIP	E16.3
HI1-1828A-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-1828A/883	-55 to 125	16 Ld CERDIP	F16.3
HI4-1828A/883	-55 to 125	20 Ld CLCC	J20.A

Functional Block Diagrams

HI-1818A

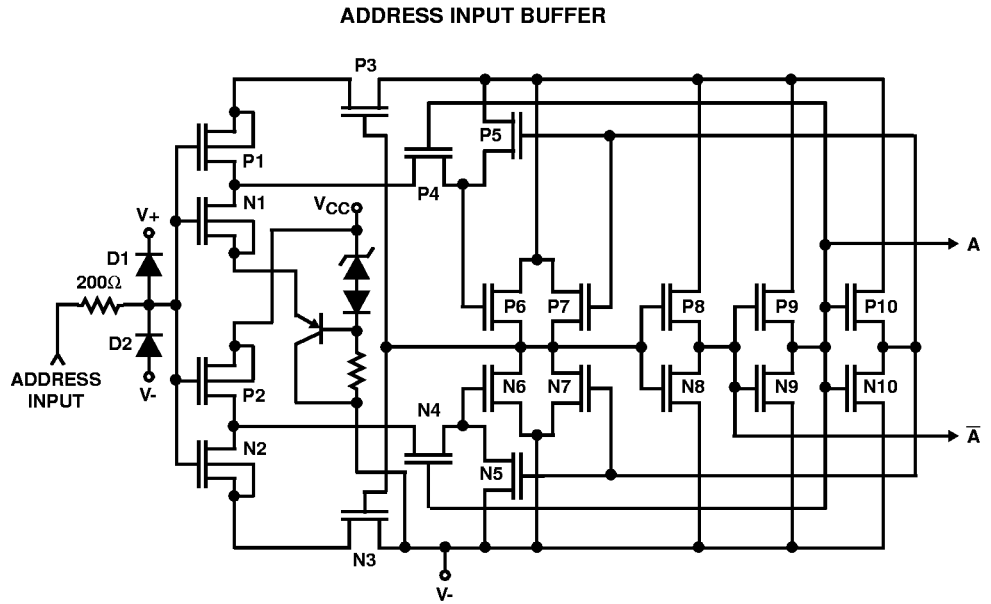


HI-1828A

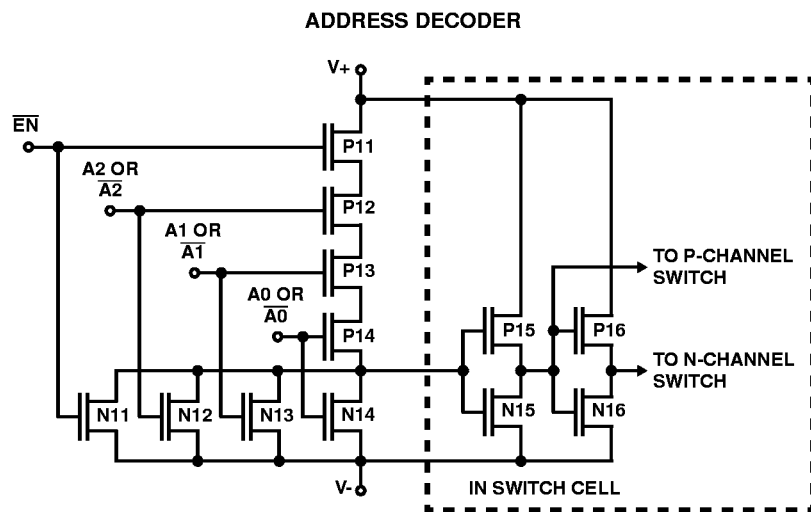


Schematic Diagrams

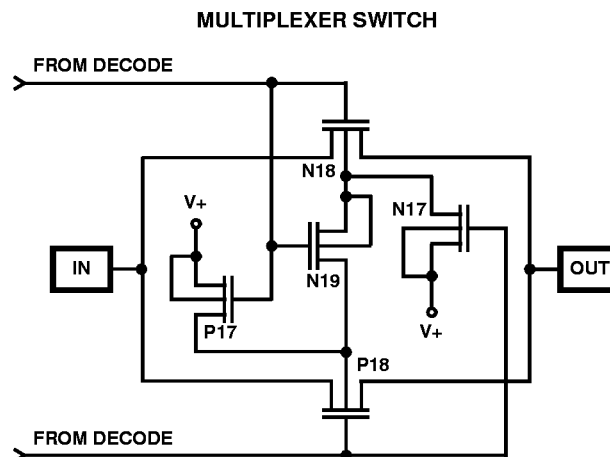
All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



All N-Channel Bodies to V-
All P-Channel Bodies to V+
A2 or A2 not used for
HI-1828A



All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



HI-1818A, HI1828A

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins	40.0V
Logic Supply Voltage	30.0V
Analog Input Voltage:	
+V _{IN}	+V _{SUPPLY} +2V
-V _{IN}	-V _{SUPPLY} -2V
Digital Input Voltage	-V _{SUPPLY} to +V _{SUPPLY}

Operating Conditions

Temperature Ranges

HI-1818A/HI-1828A-2	-55°C to 125°C
HI-1818A/HI-1828A-5, -7	0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	85	32
CLCC Package	80	28
PDIP Package	100	N/A
PLCC Package	80	N/A
Junction Temperature		
CERDIP, CLCC Packages		175°C
PDIP, PLCC Packages		150°C
Maximum Storage Temperature Range		
PDIP, PLCC Packages		-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)		300°C
(PLCC - Lead Tips Only)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-1818A/1828A -2, -8			HI-1818A/1828A -5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, T _A	(Note 4)	25	-	350	500	-	350	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay		25	-	25	-	-	100	-	ns
Settling Time		25	-	1.08	-	-	1.08	-	μs
0.1%		25	-	1.08	-	-	1.08	-	μs
0.025 %		25	-	2.8	-	-	2.8	-	μs
Channel Input Capacitance, C _{IN}		25	-	4	-	-	4	-	pF
Channel Output Capacitance, C _{OUT}		25	-	20	-	-	20	-	pF
HI-1818A		25	-	10	-	-	10	-	pF
HI-1828A		25	-	10	-	-	10	-	pF
Drain-To-Source Capacitance, C _{DS(OFF)}		25	-	0.6	-	-	0.6	-	pF
Digital Input Capacitance, C _D		25	-	5	-	-	5	-	pF
Enable Delay (ON), t _{ON(EN)}		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), t _{OFF(EN)}		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V _{AL}	(Note 3)	Full	-	-	0.4	-	-	0.4	V
Input High Threshold, V _{AH}		Full	4.0	-	-	4.0	-	-	V
Input Leakage Current, I _A		Full	-	-	1	-	-	1	μA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V _{IN}		Full	-15	-	+15	-15	-	+15	V
ON Resistance, r _{ON}	(Note 2)	25	-	250	400	-	250	400	Ω
		Full	-	-	500	-	-	500	Ω
Input Leakage Current, I _{S(OFF)}		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, I _{D(ON)}		Full	-	-	250	-	-	250	nA
HI-1818A		Full	-	-	125	-	-	125	nA
HI-1828A		Full	-	-	125	-	-	125	nA
Output Leakage Current, I _{D(OFF)}		Full	-	-	250	-	-	250	nA
HI-1818A		Full	-	-	125	-	-	125	nA
HI-1828A		Full	-	-	125	-	-	125	nA

HI-1818A, HI1828A

Electrical Specifications

Supplies = +15V, -15V, +5V; $V_{AL} = 0.4V$, $V_{AH} = 4.0V$, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-1818A/1828A -2, -8			HI-1818A/1828A -5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P _D		Full	-	-	27.5	-	-	27.5	mW
Current, I ₊		Full	-	-	0.5	-	-	0.5	mA
Current, I ₋		Full	-	-	1	-	-	1	mA
Current, I _L		Full	-	-	1	-	-	1	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = \pm 1mA$.
3. To drive from DTL/TTL circuits, $1k\Omega$ pull-up resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; $V_{OUT} = -5.0V$ to +5.0V, Digital Inputs = 0V to +4.0V.

Switching Waveforms

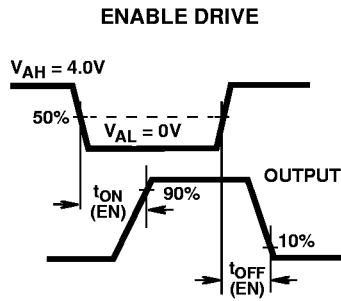


FIGURE 1A.

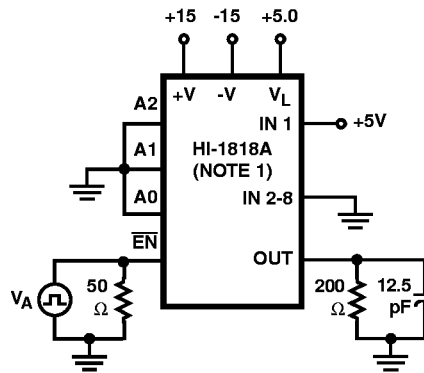


FIGURE 1B.

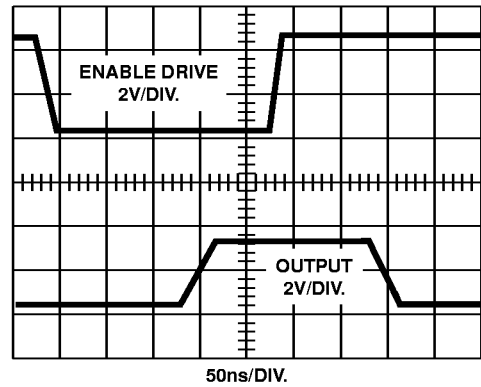


FIGURE 1C.

NOTE: 1. Similar connections for HI-1828A.

FIGURE 1. ENABLE DELAY, $t_{ON(EN)}$, $t_{OFF(EN)}$

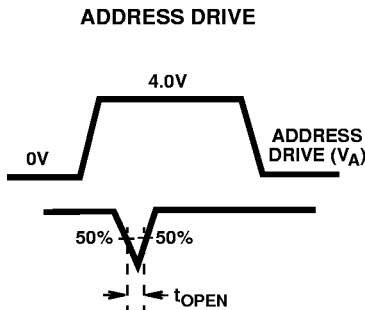


FIGURE 2A.

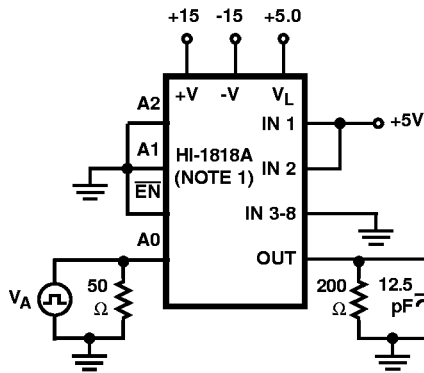


FIGURE 2B.

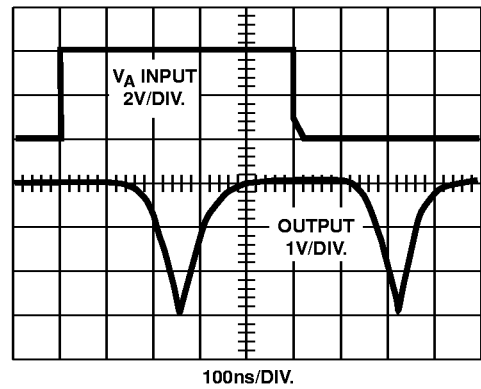


FIGURE 2C.

NOTE: 1. Similar connections for HI-1828A.

FIGURE 2. BREAK-BEFORE-MAKE DELAY, t_{OPEN}

HI-1818A, HI1828A

Truth Tables

HI-1818A TRUTH TABLE

ADDRESS				“ON” CHANNEL
A ₂	A ₁	A ₀	$\overline{\text{EN}}$	
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

HI-1828A TRUTH TABLE

ADDRESS			“ON” CHANNEL
A ₁	A ₀	$\overline{\text{EN}}$	
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	None

HI-1818A, HI1828A

Die Characteristics

DIE DIMENSIONS:

67.7 mils x 103.5 mils

METALLIZATION:

Type: CuAl

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

PASSIVATION:

Type: Nitride/Silox

Thickness: Silox: $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$, Nitride: $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$1.43 \times 10^5 \text{ A/cm}^2$ at 25mA

Metallization Mask Layout

