

SPEC No. | E L 0 6 8 1 0 9  
I S S U E: Jul. 18. 1995

To: \_\_\_\_\_

REQUEST FOR  
CONFIRMATION  
S P E C I F I C A T I O N S

Product Type 80 Output LCD Segment Driver

Model No. LH1542F

※This specifications contains 20 pages including the cover and appendix.  
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE: \_\_\_\_\_

BY: \_\_\_\_\_

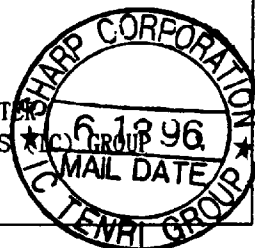
PRESENTED

BY: Y. Sano  
Y. SANO  
Dept. General Manager

Please return the enclosed document  
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ACCEPTANCE with in 15 days after  
its mail date.  
In case there is no CONFIRMATION  
OF ACCEPTANCE or COMMENT  
on it, it shall deem to be accepted  
without any objection.

REVIEWED BY: \_\_\_\_\_ PREPARED BY: \_\_\_\_\_  
H. Nishiohara K. Kurimura

ENGINEERING DEPARTMENT I  
LOGIC IC ENGINEERING CENTER  
TENRI INTEGRATED CIRCUITS  
SHARP CORPORATION



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    - Office electronics
    - Instrumentation and measuring equipment
    - Machine tools
    - Audiovisual equipment
    - Home appliances
    - Communication equipment other than for trunk lines
  - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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    - Mainframe computers
    - Traffic control systems
    - Gas leak detectors and automatic cutoff devices
    - Rescue and security equipment
    - Other safety devices and safety equipment, etc.
  - (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
    - Aerospace equipment
    - Communications equipment for trunk lines
    - Control equipment for the nuclear power industry
    - Medical equipment related to life support, etc.
  - (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.

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## 1. Summary

The LH1542F is a 80 output segment driver LSI suitable for driving black and white dot matrix LC panels.

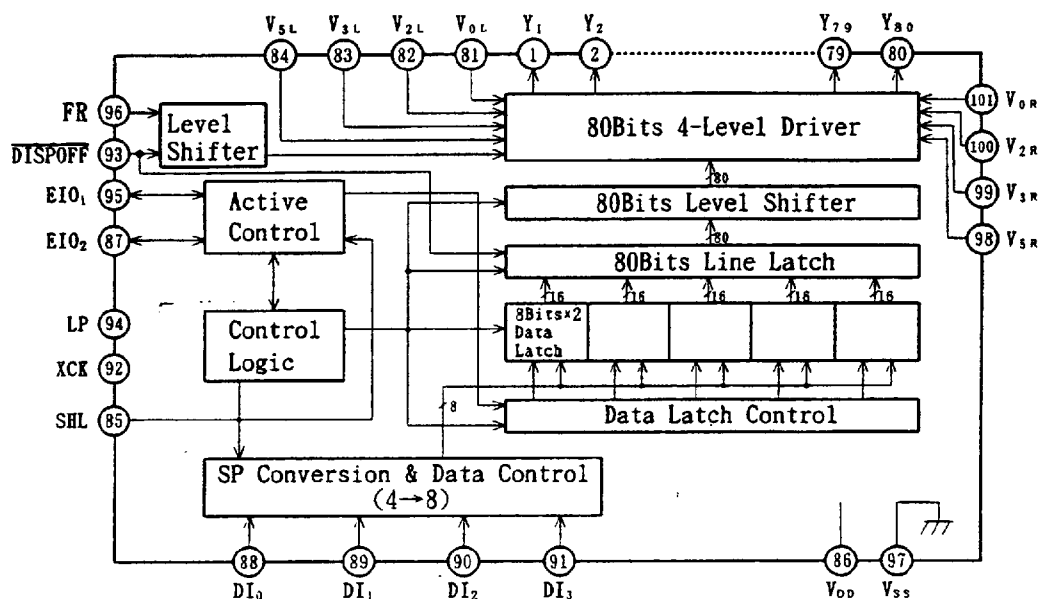
Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. The LH1542F is particularly well suited to driving black and white LC panels used for palmtop personal computers because of its low-voltage operation (Supply voltage for logic system : +2.5 to +5.5 V).

When combined with the LH1532F Common Driver, a low power consuming, high-precision LC panel display can be assembled.

## 2. Features

- Supply voltage for LC drive : +10.0 to +30.0 V
- Number of LC drive outputs : 80
- Supply voltage for the logic system : +2.5 to +5.5 V
- Low output impedance : 1.0 k $\Omega$  (Typ.)
- Shift Clock frequency : 8.0 MHz (Max.)
- Low power consumption
- Adopts a data bus system
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 80 of input data
- Line latch circuit reset function when DISPOFF active
- Supports high capacity LC panel display when combined with the LH1532F Common Driver
- CMOS process (P-type Silicon Substrate)
- Package : 101 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

## 3. Block Diagram

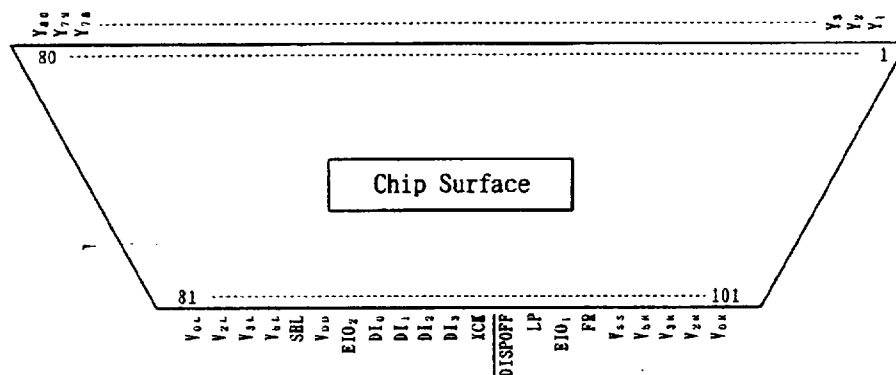


## 4. Functional Operations of Each Block

Block	Function
Active Control	Controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until-80 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
SP Conversion & Data Control	Data is retained until 8 bits have been completely input, after which they are put on the internal data bus 8 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 80 bits of data are read in 10 sets of 8 bits.
Line Latch	All 80 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

Block	Function
Level Shifter	The logic voltage signal is level-shifted to the LC driver voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the latch data, selecting one of 4 levels ( $V_0$ , $V_2$ , $V_3$ , $V_5$ ) based on the FR and <u>DISPOFF</u> signals.
Control Logic	Controls the operation of each block. When a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 80 bits of data are read in, and the chip is deselected.

## 5. Pin Configuration



## 6. Pin Descriptions

## 6-1. Pin Designations

Pin No.	Symbol	I/O	Designation
1 to 80	$Y_1 - Y_{80}$	0	LC drive output
81, 101	$V_{0L}, V_{0R}$	-	Power supply for LC drive
82, 100	$V_{2L}, V_{2R}$	-	Power supply for LC drive
83, 99	$V_{3L}, V_{3R}$	-	Power supply for LC drive
84, 98	$V_{5L}, V_{5R}$	-	Power supply for LC drive
85	SHL	I	Display data shift direction selection
86	$V_{DD}$	-	Power supply for logic system (+2.5 to +5.5 V)
87, 95	$EIO_2, EIO_1$	I/O	Input/Output for chip select
88 to 91	$DI_0 - DI_3$	I	Display data input
92	XCK	I	Display data shift clock input
93	DISPOFF	I	Control input for deselect output level
94	LP	I	Display data latch pulse input
96	FR	I	AC-converting signal input for LC drive waveform
97	$V_{SS}$	-	Ground(0 V)

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## 6-2. Input/Output Circuits

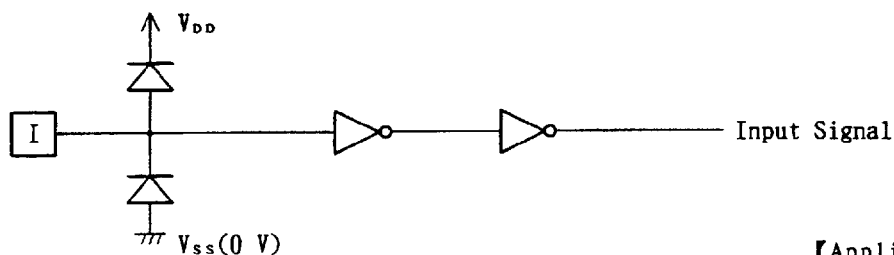


Fig.1 Input Circuit

【Applicable pins】  
 $DI_0-3, XCK, LP, FR$   
 $SHL, DISPOFF$

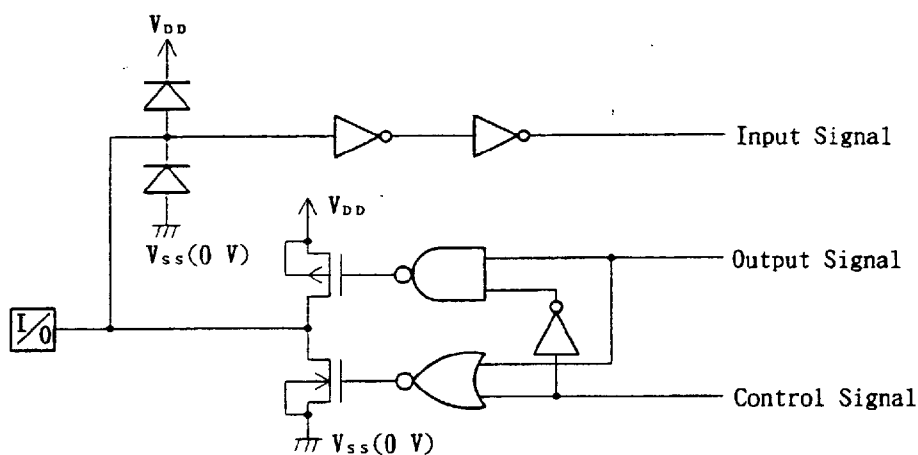


Fig.2 Input/Output Circuit

【Applicable pins】  
 $EIO_1, EIO_2$

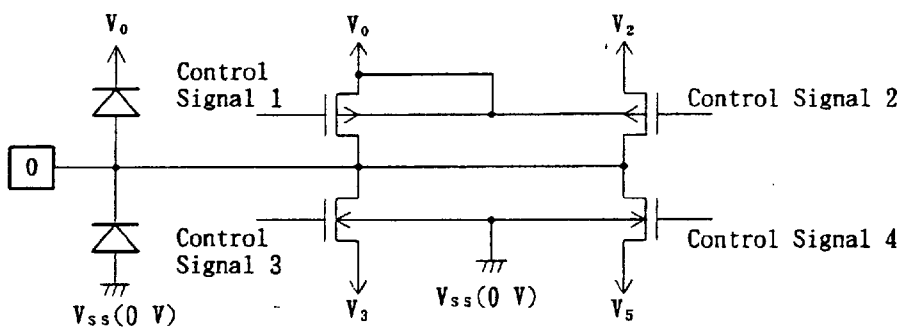


Fig.3 LC Drive Output Circuit

【Applicable pins】  
 $Y_1-Y_{80}$

## 7. Description of Functional Operations

## 7-1. Pin Functions

Symbol	Function
$V_{DD}$	Logic system power supply pin connects to +2.5 to +5.5 V
$V_{SS}$	Ground pin connects to 0 V
$V_{0R}, V_{0L}$ $V_{2R}, V_{2L}$ $V_{3R}, V_{3L}$ $V_{5R}, V_{5L}$	Power supply pin for LC driver voltage bias. <ul style="list-style-type: none"> <li>• Normally, the bias voltage used is set by a resistor divider.</li> <li>• Ensure that voltages are set such that <math>V_{SS} \leq V_5 &lt; V_3 &lt; V_2 &lt; V_0</math>.</li> <li>• To further reduce the difference between the output waveforms of LC driver output pins <math>Y_1</math> and <math>Y_{80}</math>, externally connect <math>V_{1R}</math> and <math>V_{1L}</math> (<math>i=0, 2, 3, 5</math>).</li> </ul>
$DI_0-DI_3$	Input Pin for display data Input data into the 4 pins $DI_0-DI_3$ . <ul style="list-style-type: none"> <li>• The relationship between the display data and driver output pins is shown in 7-2-2.</li> </ul>
XCK	Clock input pin for taking display data <ul style="list-style-type: none"> <li>• Data is read on the falling edge of the clock pulse.</li> </ul>
LP	Latch pulse input pin for display data <ul style="list-style-type: none"> <li>• Data is latched on the falling edge of the clock pulse.</li> </ul>
SHL	Direction selection pin for reading display data <ul style="list-style-type: none"> <li>• When set to <math>V_{SS}</math> level "L", data is read sequentially from <math>Y_{80}</math> to <math>Y_1</math>.</li> <li>• When set to <math>V_{DD}</math> level "H", data is read sequentially from <math>Y_1</math> to <math>Y_{80}</math>.</li> </ul>
DISPOFF	Control input pin for output deselect level <ul style="list-style-type: none"> <li>• The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>• When set to <math>V_{SS}</math> level "L", the LC driver output pins (<math>Y_1-Y_{160}</math>) are set to level <math>V_5</math>.</li> <li>• While set to "L", the contents of the line latch are reset, display data is read in the data latch no relation with <u>DISPOFF</u>.</li> </ul> After <u>DISPOFF</u> is reset, the deselect level ( $V_2$ or $V_3$ ) is output, and the contents of the line latch is output on the falling edge of the next LP signal. That time, if <u>DISPOFF</u> removal time can not keep regulation what is shown AC characteristics, the reading data is not correctly output.
FR	AC signal input for LC driving waveform <ul style="list-style-type: none"> <li>• The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>• Normally, inputs a frame inversion signal.</li> <li>• The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal.</li> </ul> Table of truth values is shown in 7-2-1.

Symbol	Function
EIO <sub>1</sub> EIO <sub>2</sub>	Input/Output pin for chip selection •When SHL input is at V <sub>ss</sub> level "L", EIO <sub>1</sub> is set for output, and EIO <sub>2</sub> is set for input. •When SHL input is at V <sub>DD</sub> level "H", EIO <sub>1</sub> is set for input, and EIO <sub>2</sub> is set for output. •During output, set to "H" while LP* $\overline{\text{XCK}}$ is "H" and after 80 bits of data have been read set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". •During input, after the LP signal is input, the chip is selected while EI is set to "L". After 80-bits of data have been read, the chip is deselected.
Y <sub>1</sub> -Y <sub>80</sub>	LC driver output pins •Corresponding directly to each bit of the data latch, one level (V <sub>0</sub> , V <sub>2</sub> , V <sub>3</sub> , or V <sub>5</sub> ) is selected and output.

## 7-2. Functional Operations

### 7-2-1. Truth Table

FR	Latch Data	DISPOFF	Driver Output Voltage Level (Y <sub>1</sub> -Y <sub>80</sub> )
L	L	H	V <sub>3</sub>
L	H	H	V <sub>5</sub>
H	L	H	V <sub>2</sub>
H	H	H	V <sub>0</sub>
x	x	L	V <sub>5</sub>

Here,  $V_{ss} \leq V_5 < V_3 < V_2 < V_0$ , H: V<sub>DD</sub> (+2.5 to +5.5 V), L: V<sub>ss</sub> (0 V), x: Don't care

**[Note]** "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin.

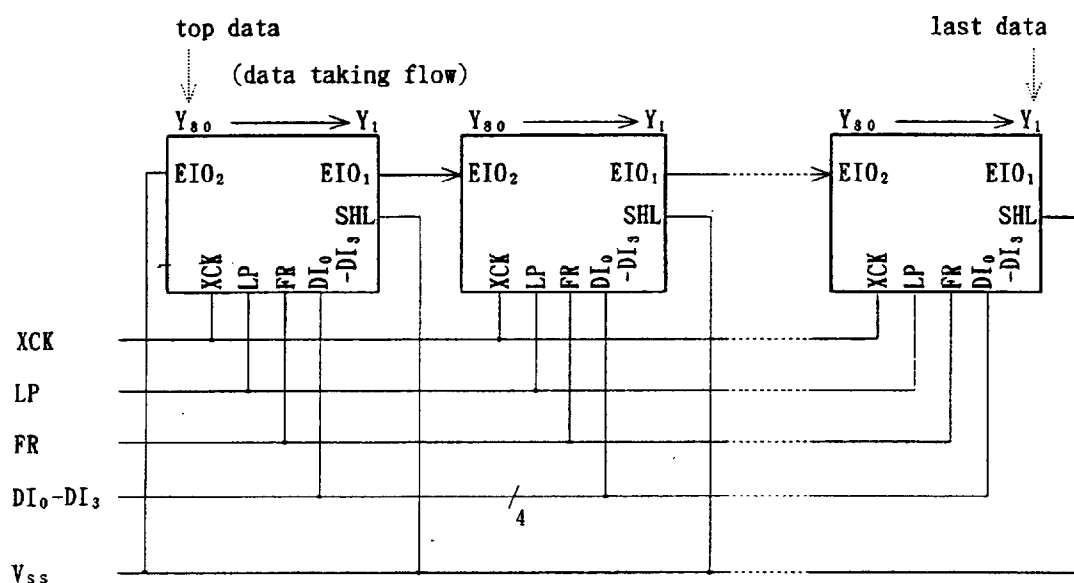
### 7-2-2. Relationship between the Display Data and Driver Output pins

SHL	EIO <sub>1</sub>	EIO <sub>2</sub>	Data Input	Figure of Clock						
				20clock	19clock	18clock	...	3clock	2clock	1clock
L	Output	Input	DI <sub>0</sub>	Y <sub>1</sub>	Y <sub>5</sub>	Y <sub>9</sub>	...	Y <sub>80</sub>	Y <sub>79</sub>	Y <sub>77</sub>
			DI <sub>1</sub>	Y <sub>2</sub>	Y <sub>6</sub>	Y <sub>10</sub>	...	Y <sub>70</sub>	Y <sub>74</sub>	Y <sub>78</sub>
			DI <sub>2</sub>	Y <sub>3</sub>	Y <sub>7</sub>	Y <sub>11</sub>	...	Y <sub>71</sub>	Y <sub>75</sub>	Y <sub>79</sub>
			DI <sub>3</sub>	Y <sub>4</sub>	Y <sub>8</sub>	Y <sub>12</sub>	...	Y <sub>72</sub>	Y <sub>74</sub>	Y <sub>80</sub>
H	Input	Output	DI <sub>0</sub>	Y <sub>80</sub>	Y <sub>78</sub>	Y <sub>72</sub>	...	Y <sub>12</sub>	Y <sub>8</sub>	Y <sub>4</sub>
			DI <sub>1</sub>	Y <sub>79</sub>	Y <sub>75</sub>	Y <sub>71</sub>	...	Y <sub>11</sub>	Y <sub>7</sub>	Y <sub>3</sub>
			DI <sub>2</sub>	Y <sub>78</sub>	Y <sub>74</sub>	Y <sub>70</sub>	...	Y <sub>10</sub>	Y <sub>6</sub>	Y <sub>2</sub>
			DI <sub>3</sub>	Y <sub>77</sub>	Y <sub>73</sub>	Y <sub>69</sub>	...	Y <sub>9</sub>	Y <sub>5</sub>	Y <sub>1</sub>

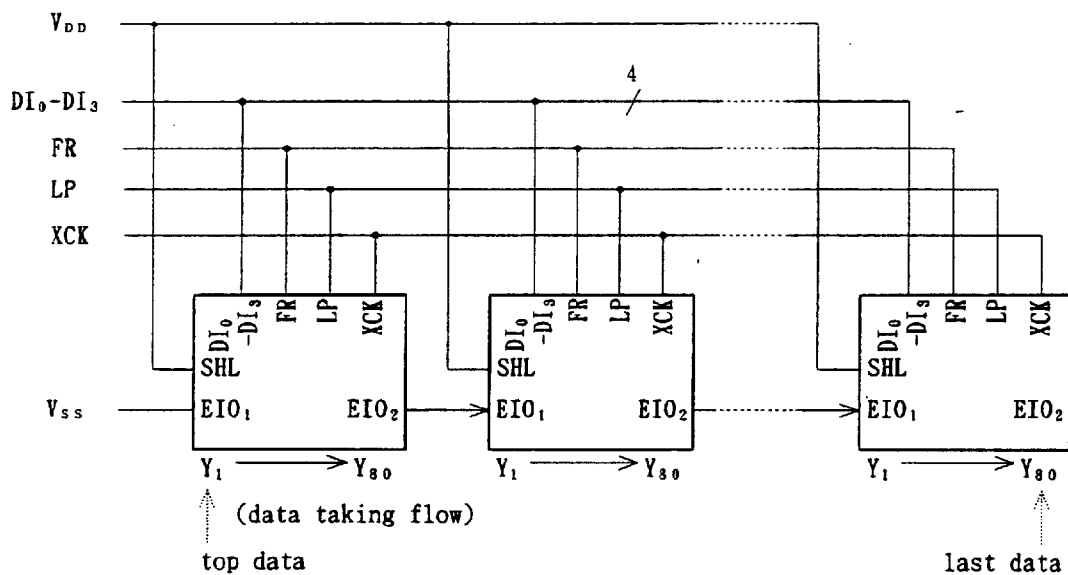
Here, H: V<sub>DD</sub> (+2.5 to +5.5 V), L: V<sub>ss</sub> (0 V)

## 7-2-3. Connection Examples of Plural Segment Drivers

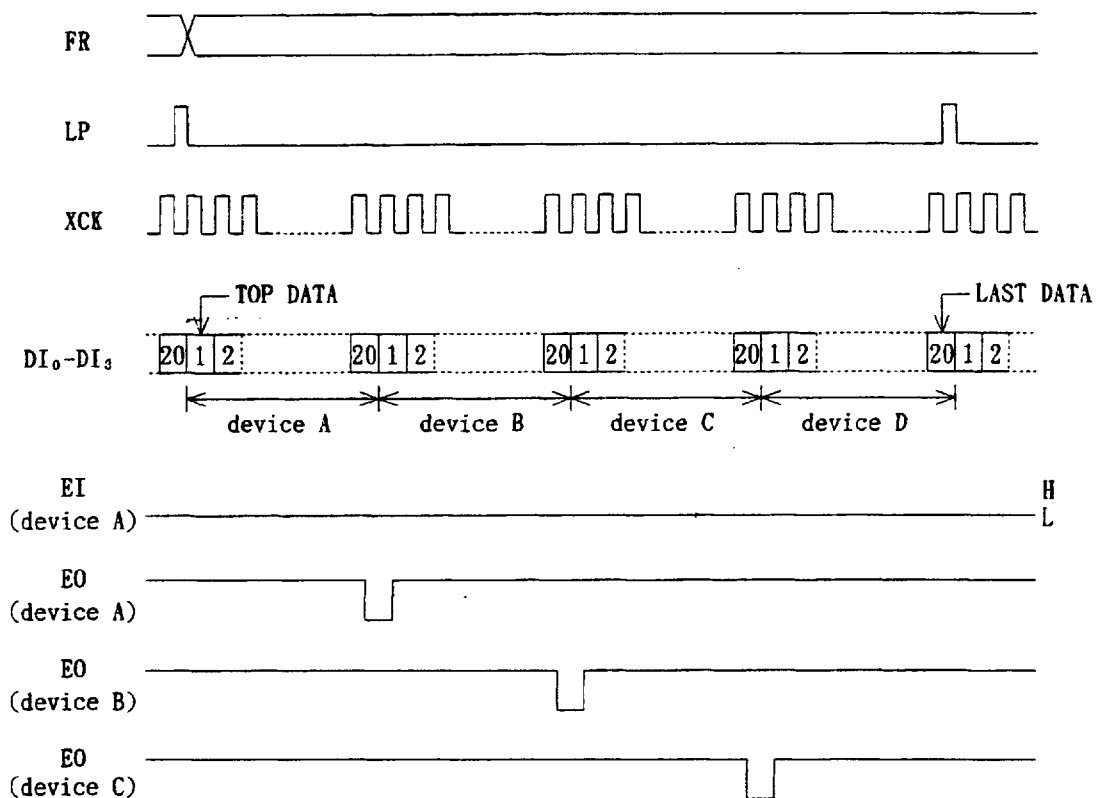
(a) Case of SHL="L"



(b) Case of SHL="H"



7-2-4. Timing Chart of 4-Device cascade Connection



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## 8. Precaution

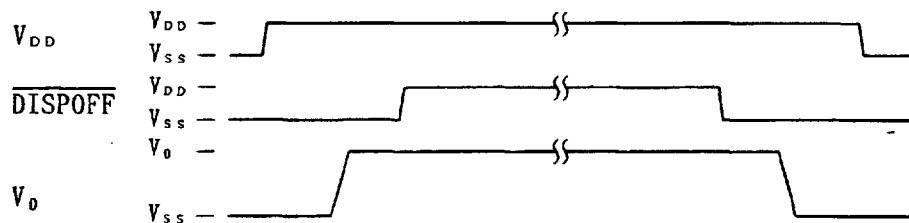
## ○Precaution when connecting or disconnecting the power

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LC driver voltage after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC driver voltage.
- We recommend you connecting the serial resistor (50~100  $\Omega$ ) to the LC driver voltage  $V_0$  of the system as a current limiter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on DISPOFF function. After that, cancel the DISPOFF function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level  $V_S$  on DISPOFF function. After that, disconnect the logic system power after disconnecting the LC drive power.

When connecting the power supply, show the following recommend sequence.



## 9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	$V_{DD}$	$T_a=25\text{ }^{\circ}\text{C}$	$V_{DD}$	-0.3 to +7.0	V
Supply voltage (2)	$V_0$	Referenced to $V_{SS}(0\text{ V})$	$V_{0L}, V_{0R}$	-0.3 to +32.0	V
	$V_2$		$V_{2L}, V_{2R}$	-0.3 to $V_0+0.3$	V
	$V_3$		$V_{3L}, V_{3R}$	-0.3 to $V_0+0.3$	V
	$V_5$		$V_{5L}, V_{5R}$	-0.3 to $V_0+0.3$	V
Input voltage	$V_I$		$DI_{0-3}, XCK, LP, SHL, FR$ $EIO_1, EIO_2, DISPOFF$	-0.3 to $V_{DD}+0.3$	V
Storage temperature	$T_{stg}$			-45 to +125	$^{\circ}\text{C}$

## 10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	$V_{DD}$	Referenced	$V_{DD}$	+2.5		+5.5	V
Supply voltage (2)	$V_0$	to $V_{SS}(0\text{ V})$	$V_{0L}, V_{0R}$	+10.0		+30.0	V
Operating temperature	$T_{opr}$			-20		+85	$^{\circ}\text{C}$

## 11. Electrical Characteristics

## 11-1. DC Characteristics

(V<sub>SS</sub>=V<sub>S</sub>=0 V, V<sub>DD</sub>=+2.5 to +5.5 V, V<sub>0</sub>=+10.0 to +30.0 V, T<sub>a</sub>=-20 to +85  $^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	$V_{IH}$		$DI_{0-3}, XCK, LP, SHL, FR$	0.8V <sub>DD</sub>			V
	$V_{IL}$		$EIO_1, EIO_2, DISPOFF$			0.2V <sub>DD</sub>	V
Output voltage	$V_{OH}$	$I_{OH}=-0.4\text{ mA}$	$EIO_1, EIO_2$	$V_{DD}-0.4$			V
	$V_{OL}$	$I_{OL}=+0.4\text{ mA}$				+0.4	V
Input leakage current	$I_{LI}$	$V_{SS} \leq V_I \leq V_{DD}$	All input pins		-	$\pm 10.0$	$\mu\text{A}$
I/O leakage current	$I_{LI/O}$	$V_{SS} \leq V_I \leq V_{DD}$	$EIO_1, EIO_2$			$\pm 10.0$	$\mu\text{A}$
Output resistance	$R_{ON}$	*1 $V_0=+30\text{ V}$	$Y_1-Y_{40}$		1.0	1.5	k $\Omega$
		$V_0=+20\text{ V}$			1.5	2.0	
		$V_0=+10\text{ V}$			2.0	3.0	
Stand-by current	$I_{STB}$	*2	$V_{SS}$			50.0	$\mu\text{A}$
Consumed current (1) (Deselection)	$I_{DD1}$	$V_{DD}=+3.0\text{ V}$ *3	$V_{DD}$			0.6	mA
		$V_{DD}=+5.0\text{ V}$ *3				1.0	mA
Consumed current (2) (Selection)	$I_{DD2}$	$V_{DD}=+3.0\text{ V}$ *3	$V_{DD}$			3.0	mA
		$V_{DD}=+5.0\text{ V}$ *3				5.0	mA
Consumed current (3)	$I_0$	*4	$V_{0L}, V_{0R}$			1.0	mA

## 【Note】

\*1:  $|\Delta V_{ON}|=0.5\text{ V}$ \*2:  $V_{DD}=+5.0\text{ V}$ ,  $V_0=+30.0\text{ V}$ ,  $V_{IH}=V_{DD}$ ,  $V_{IL}=V_{SS}$ \*3:  $V_0=+30.0\text{ V}$ ,  $f_{XCK}=6.15\text{ MHz}$ , No-load

The input data is turned over by data taking clock(4-bit parallel input mode)

\*4:  $V_{DD}=+5.0\text{ V}$ ,  $V_0=+30.0\text{ V}$ ,  $f_{XCK}=6.15\text{ MHz}$ ,  $f_{LP}=19.2\text{ kHz}$ ,  $f_{FR}=80\text{ Hz}$ , No-load

The input data is turned over by data taking clock(4-bit parallel input mode)

## 11-2. AC Characteristics

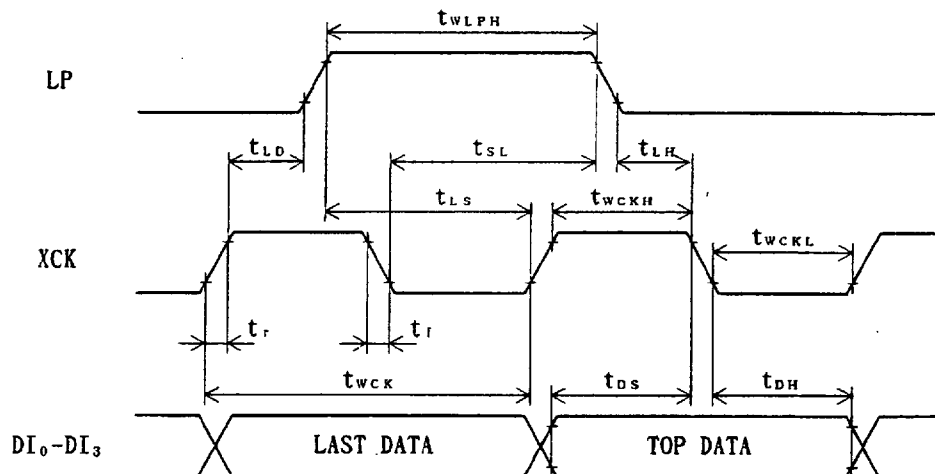
(V<sub>SS</sub>=V<sub>S</sub>=0 V, V<sub>DD</sub>=+2.5 to +5.5 V, V<sub>O</sub>=+10.0 to +30.0 V, T<sub>a</sub>=-20 to +85 °C)

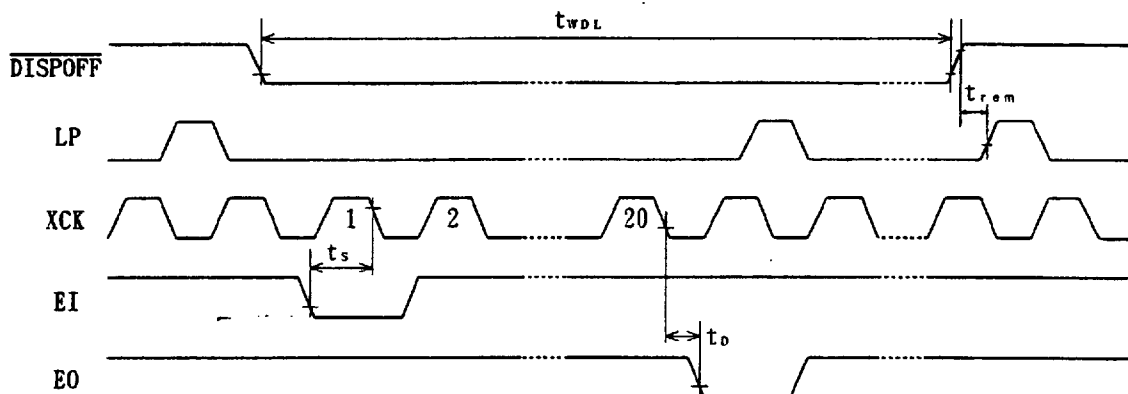
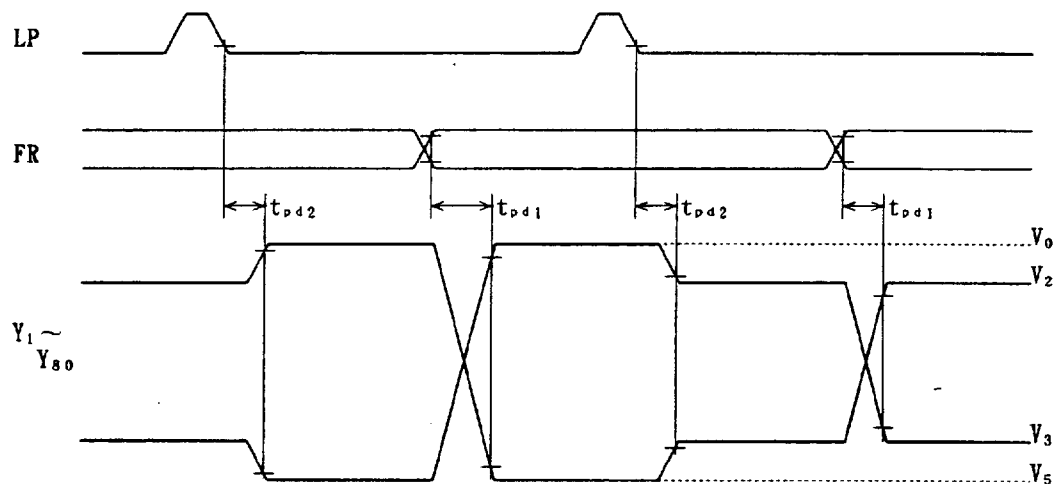
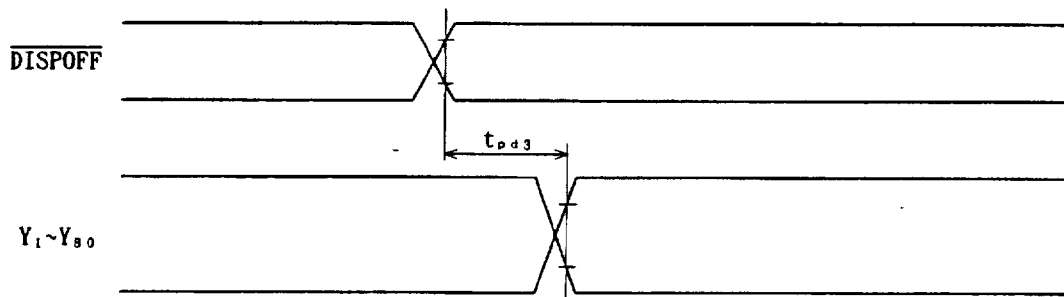
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t <sub>WCK</sub>	t <sub>r</sub> , t <sub>f</sub> ≤ 11 ns	125			ns
Shift clock "H" pulse width	t <sub>WCKH</sub>		51			ns
Shift clock "L" pulse width	t <sub>WCKL</sub>		51			ns
Data setup time	t <sub>DS</sub>		40			ns
Data hold time	t <sub>DH</sub>		30			ns
Latch pulse "H" pulse width	t <sub>WLPH</sub>		51			ns
Shift clock rise to Latch pulse rise time	t <sub>LD</sub>		0			ns
Shift clock fall to Latch pulse fall time	t <sub>SL</sub>		51			ns
Latch pulse rise to Shift clock rise time	t <sub>LS</sub>		51			ns
Latch pulse fall to Shift clock fall time	t <sub>LH</sub>		51			ns
Enable setup time	t <sub>S</sub>		30			ns
DISPOFF "L" pulse width	t <sub>WDL</sub>		1.2			μs
DISPOFF removal time	t <sub>ram</sub>		100			ns
Input signal rise time	t <sub>r</sub>	Note			50	ns
Input signal fall time	t <sub>f</sub>				50	ns
Output delay time (1) XCK to EIO <sub>1</sub> , EIO <sub>2</sub>	t <sub>D</sub>	C <sub>L</sub> =15 pF			80	ns
Output delay time (2) FR to Y <sub>1</sub> -Y <sub>80</sub>	tpd <sub>1</sub>				1.2	μs
Output delay time (3) LP to Y <sub>1</sub> -Y <sub>80</sub>	tpd <sub>2</sub>				1.2	μs
Output delay time (4) DISPOFF to Y <sub>1</sub> -Y <sub>80</sub>	tpd <sub>3</sub>				1.2	μs

【Note】 (t<sub>WCK</sub>-t<sub>WCKH</sub>-t<sub>WCKL</sub>)/2 is maximum in the case of high speed operation.

## 11-3. Timing Diagrams

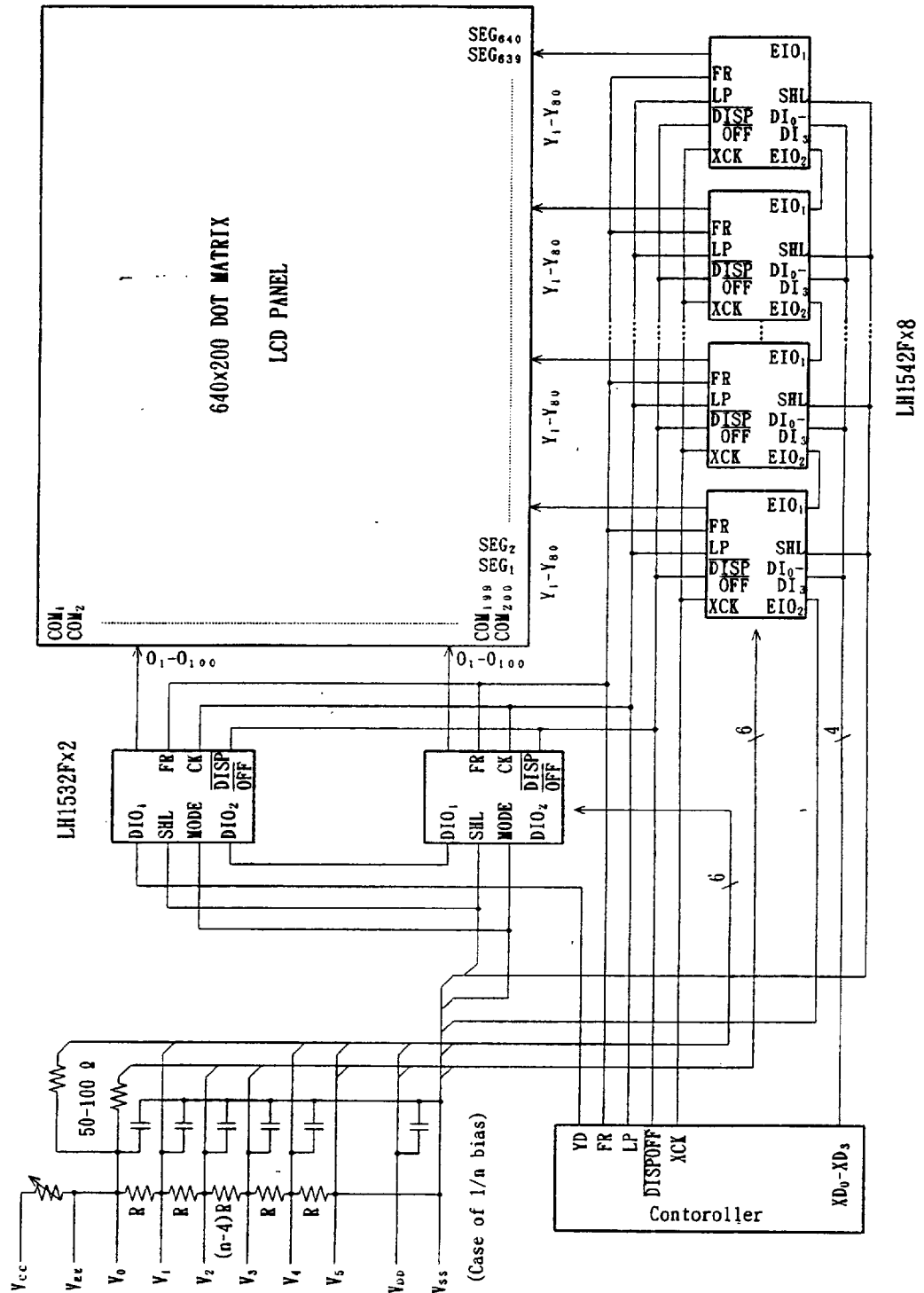
## Input Timing Characteristics



Input/Output Timing Characteristics 1Input/Output Timing Characteristics 2Input/Output Timing Characteristics 3

8180798 0027691 091

## 12. Example of System Configuration



## 13. Example of Typical Characteristic

Parameter	Conditions	Min.	Typ.	Max.	Unit
Typical Fundamental Rating	Ta=+25 °C, V <sub>SS</sub> =0 V, V <sub>DD</sub> =+5.0 V		10		ns
Propagation Delay Time					

## 14. PACKAGE AND PACKING SPECIFICATION

## 1. Package Outline Specification

Refer to drawing No. SPN2201-00

## 2. Markings

The meanings of the device code printed on each tape carrier package are as follows.

(1) Date code (example) :  $\frac{4}{a)} \frac{37}{b)} \frac{0}{c)}$ 

a) denotes the last figure of Anno Domini (of production)

b) denotes the week (of production)

c) denotes the number of times of alteration

## 3. Packing Specifications

## (1) Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 $\mu$ mt)	Protects device and prevents ESD (Electro Static Discharge)
Laminated aluminium bag	(520 $\times$ 600mm)	Keeping dry.
Adhesive tape paper		Fixing of tape carrier package and separator.
Carton	Cardboard(420x420x50mm)	Contains a reel.
Label	Paper	Indicates production name, lot.No. and quantity.
Desiccant	Silica gel	Drying of device

## (2) Packing Form

a) Tape carrier package(TCP)is wound on a reel with separators 1 and 2 and the ends of them are fixed with adhesive tape.

b) A label indicating production name, lot no. and quantity is stuck on one side of the reel.

c) The reel and silica gel is put in a laminated aluminium bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the carton.

## \* Specification of label

TYPE	
	PRODUCTION NAME LOT NO.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPING DATE

## 4. Miscellaneous

(1) The length of the tape carrier is 34 ~ 46 meters maximum per reel, and depends on shipping quantity.

(2) Before unpacking, prepare a work bench equipped with anti-static devices. Also, the operator should wear anti-static wrist bands.

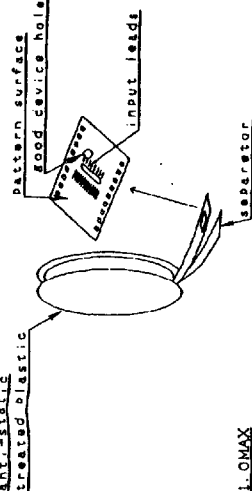
(3) The device, once unpacked, should be stored in a nitrogen gas, room temperature atmosphere and used within 1 week.

ISSUE DATE	AUG.24.1994	APPROVE	CHECK	DESIGN	(NOTE)
ISSUE NUMBER	H6807	A. Suzuki	Y. Honda	T. Kidozuchi	
S/C NUMBER					

■ 8180798 0027694 8T0 ■

SHARP

## NOTES: 1. REEL WINDING

anti-static  
treated plastic

DUMMY Y80  
DUMMY Y81

20.3 (E.L.)  
19.0 ± 0.05  
16.976 ± 0.05  
17.01 x 0.980 = 16.976  
pitch: 0.25, lead width 0.105, 82 leads

2. RESIN AREA OF FRONT AND BACK SURFACE IS 13.8 x 3.3mm (MAX).
3. E.L. MEANS ASSUMED EXCISING LINE.
4. SL MEANS DIMENSION OF PUNCHING HOLE AND ITS TOLERANCE IS ± 0.05mm.
5. SR MEANS DIMENSION OF SOLDER RESIST AND ITS TOLERANCE IS ± 0.3mm.

3.4 ± 0.05  
2.0 (hole)  
0.5 (E.L.)

2-±0.6 (P.L.)  
2-±0.5 (P.L.)

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