SHARP

SPEC No.	EL068109
ISSUE:	Jul. 18. 1995

To; _____

REQUEST FOR
CONFIRMATION

SPECIFICATIONS

Product Type 80 Output LCD Segment Driver

Model No. LH1542F

※This specifications contains 20 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

Please return the enclosed document with your CONFIRMATION OF ACCEPTANCE within 45 days after its mail date.
In case there is no CONFIRMATION OF ACCEPTANCE or COMMENT on it, it shall deem to be accepted without any objection.

PRESENTED

BY: Y. Sano
Y. SANO
Dept. General Manager

REVIEWED BY: H. Nishioka

PREPARED BY: K. Kurimoto

ENGINEERING DEPARTMENT I
LOGIC IC ENGINEERING CENTER
TENRI INTEGRATED CIRCUITS I.C. GROUP
SHARP CORPORATION

SHARP CORPORATION ★ I.C. TENRI GROUP ★
6.13.96
MAIL DATE

8180798 0027676 885

●Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

		Page
1.	Summary	2
2.	Features	2
3.	Block Diagram	3
4.	Functional Operations of Each Block	3
5.	Pin Configuration	5
6.	Pin Descriptions	5
7.	Description of Functional Operations	7
8.	Precaution	11
9.	Absolute Maximum Ratings	12
10.	Recommended Operating Conditions	12
11.	Electrical Characteristics	12
12.	Example of System Configuration	15
13.	Example of Typical Characteristic	16
14.	Package and Packing Specification	17

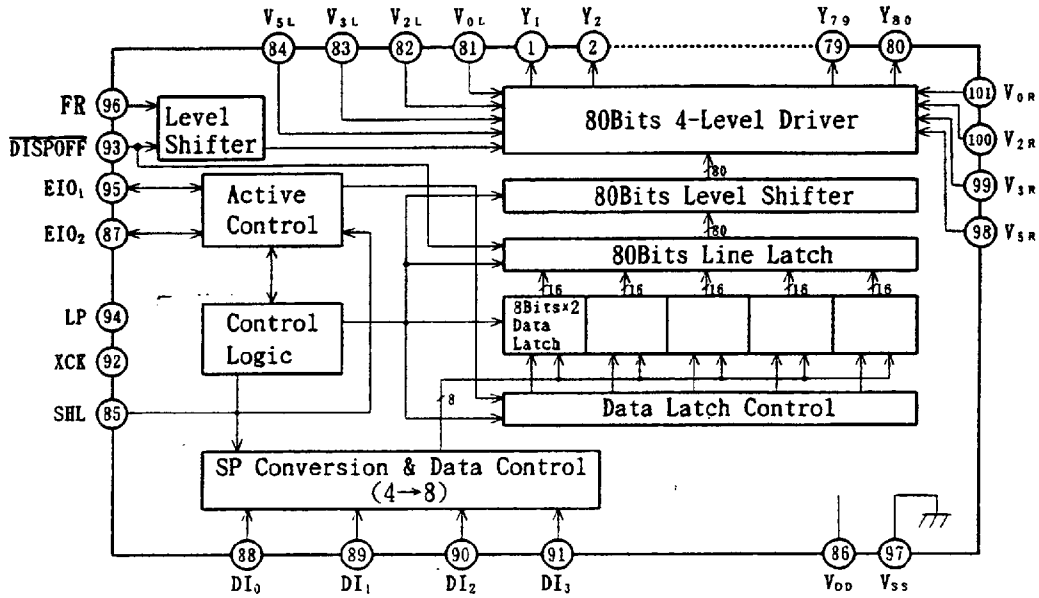
1. Summary

The LH1542F is a 80 output segment driver LSI suitable for driving black and white dot matrix LC panels.
Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module.
The LH1542F is particularly well suited to driving black and white LC panels used for palmtop personal computers because of its low-voltage operation (Supply voltage for logic system : +2.5 to +5.5 V).
When combined with the LH1532F Common Driver, a low power consuming, high-precision LC panel display can be assembled.

2. Features

- Supply voltage for LC drive : +10.0 to +30.0 V
- Number of LC drive outputs : 80
- Supply voltage for the logic system : +2.5 to +5.5 V
- Low output impedance : 1.0 kΩ (Typ.)
- Shift Clock frequency : 8.0 MHz (Max.)
- Low power consumption
- Adopts a data bus system
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 80 of input data
- Line latch circuit reset function when $\overline{\text{DISPOFF}}$ active
- Supports high capacity LC panel display when combined with the LH1532F Common Driver
- CMOS process (P-type Silicon Substrate)
- Package : 101 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

3. Block Diagram

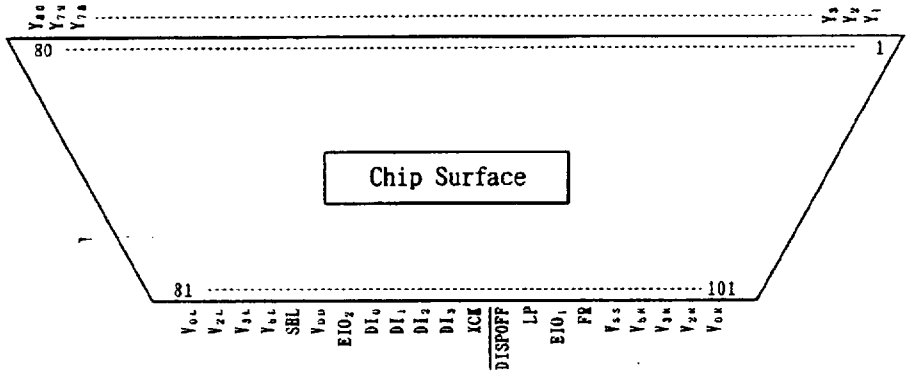


4. Functional Operations of Each Block

Block	Function
Active Control	Controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until 80 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
SP Conversion & Data Control	Data is retained until 8 bits have been completely input, after which they are put on the internal data bus 8 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 80 bits of data are read in 10 sets of 8 bits.
Line Latch	All 80 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

Block	Function
Level Shifter	The logic voltage signal is level-shifted to the LC driver voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the latch data, selecting one of 4 levels (V_0, V_2, V_3, V_5) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the operation of each block. When a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 80 bits of data are read in, and the chip is deselected.

5. Pin Configuration

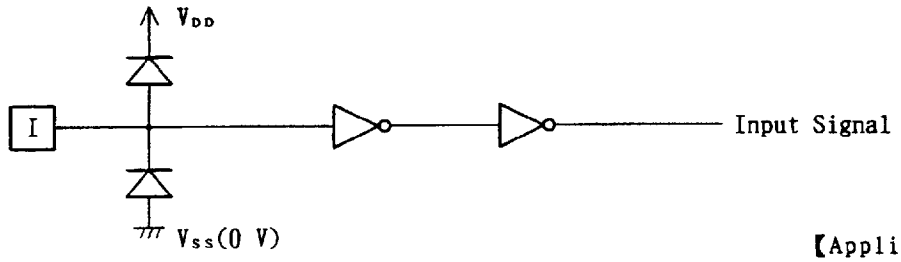


6. Pin Descriptions

6-1. Pin Designations

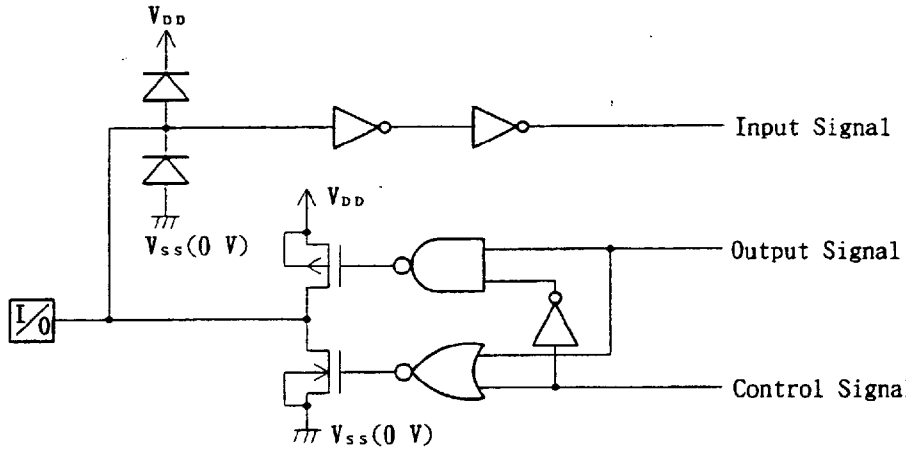
Pin No.	Symbol	I/O	Designation
1 to 80	Y_1 - Y_{80}	O	LC drive output
81, 101	V_{0L}, V_{0R}	-	Power supply for LC drive
82, 100	V_{2L}, V_{2R}	-	Power supply for LC drive
83, 99	V_{3L}, V_{3R}	-	Power supply for LC drive
84, 98	V_{5L}, V_{5R}	-	Power supply for LC drive
85	SHL	I	Display data shift direction selection
86	V_{DD}	-	Power supply for logic system (+2.5 to +5.5 V)
87, 95	EIO_2, EIO_1	I/O	Input/Output for chip select
88 to 91	DI_0-DI_3	I	Display data input
92	XCK	I	Display data shift clock input
93	$\overline{\text{DISPOFF}}$	I	Control input for deselect output level
94	LP	I	Display data latch pulse input
96	FR	I	AC-converting signal input for LC drive waveform
97	V_{SS}	-	Ground(0 V)

6-2. Input/Output Circuits



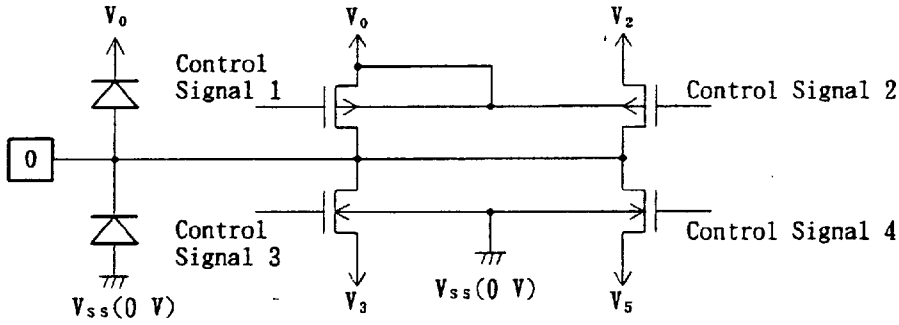
【Applicable pins】
DI_{0-3}, XCK, LP, FR
SHL, $\overline{DISPOFF}$

Fig.1 Input Circuit



【Applicable pins】
$EI\Theta_1$, EIO_2

Fig.2 Input/Output Circuit



【Applicable pins】
Y_1-Y_{80}

Fig.3 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{2R}, V_{2L} V_{3R}, V_{3L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. •Normally, the bias voltage used is set by a resistor divider. •Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$. •To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{80}, externally connect V_{iR} and V_{iL} ($\bar{i}$=0, 2, 3, 5).
DI_0-DI_3	Input Pin for display data Input data into the 4 pins DI_0-DI_3. •The relationship between the display data and driver output pins is shown in 7-2-2.
XCK	Clock input pin for taking display data •Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data •Data is latched on the falling edge of the clock pulse.
SHL	Direction selection pin for reading display data •When set to V_{SS} level "L", data is read sequentially from Y_{80} to Y_1. •When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{80}.
$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •When set to V_{SS} level "L", the LC driver output pins(Y_1-Y_{160}) are set to level V_5. •While set to "L", the contents of the line latch are reset, display data is read in the data latch no relation with $\overline{DISPOFF}$. After $\overline{DISPOFF}$ is reset, the deselect level(V_2 or V_3) is output, and the contents of the line latch is output on the falling edge of the next LP signal. That time, if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics, the reading data is not correctly output.
FR	AC signal input for LC driving waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •Normally, inputs a frame inversion signal. •The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in 7-2-1.

Symbol	Function
EIO_1 EIO_2	Input/Output pin for chip selection •When SHL input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. •When SHL input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. •During output, set to "H" while LP*$\overline{XCK}$ is "H" and after 80 bits of data have been read set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". •During input, after the LP signal is input, the chip is selected while EI is set to "L". After 80-bits of data have been read, the chip is deselected.
Y_1-Y_{80}	LC driver output pins •Corresponding directly to each bit of the data latch, one level (V_0, V_2, V_3, or V_5) is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1-Y_{80})
L	L	H	V_3
L	H	H	V_5
H	L	H	V_2
H	H	H	V_0
x	x	L	V_5

Here, $V_{SS} \leq V_5 < V_3 < V_2 < V_0$, H : V_{DD}(+2.5 to +5.5 V), L : V_{SS}(0 V), x : Don't care

【Note】 "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin.

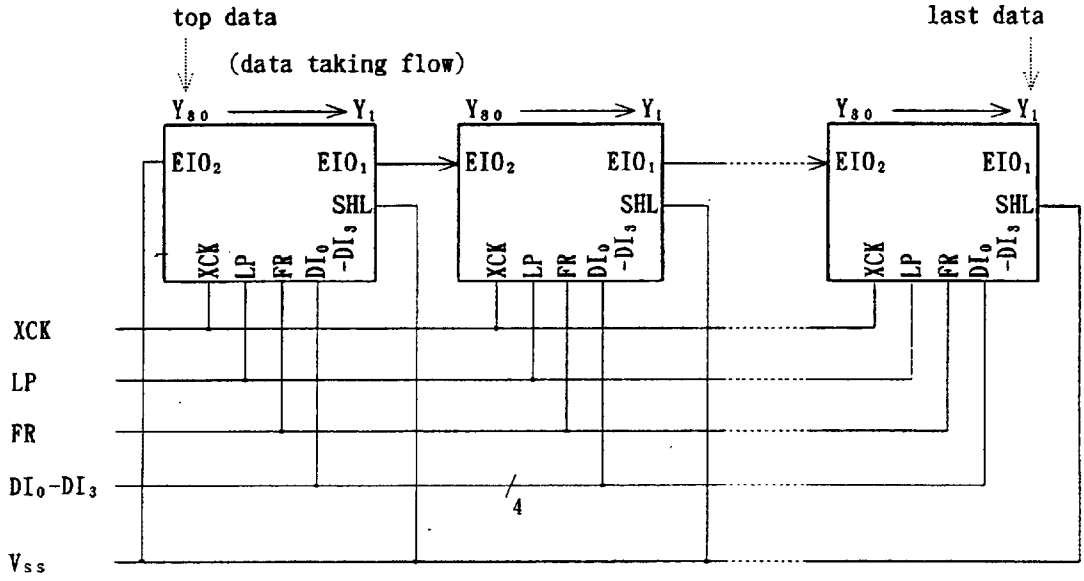
7-2-2. Relationship between the Display Data and Driver Output pins

SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
				20clock	19clock	18clock	···	3clock	2clock	1clock
L	Output	Input	DI_0	Y_1	Y_5	Y_9	···	Y_{80}	Y_{79}	Y_{77}
			DI_1	Y_2	Y_6	Y_{10}	···	Y_{70}	Y_{74}	Y_{78}
			DI_2	Y_3	Y_7	Y_{11}	···	Y_{71}	Y_{75}	Y_{79}
			DI_3	Y_4	Y_8	Y_{12}	···	Y_{72}	Y_{74}	Y_{80}
H	Input	Output	DI_0	Y_{80}	Y_{76}	Y_{72}	···	Y_{12}	Y_8	Y_4
			DI_1	Y_{79}	Y_{75}	Y_{71}	···	Y_{11}	Y_7	Y_3
			DI_2	Y_{78}	Y_{74}	Y_{70}	···	Y_{10}	Y_6	Y_2
			DI_3	Y_{77}	Y_{73}	Y_{69}	···	Y_9	Y_5	Y_1

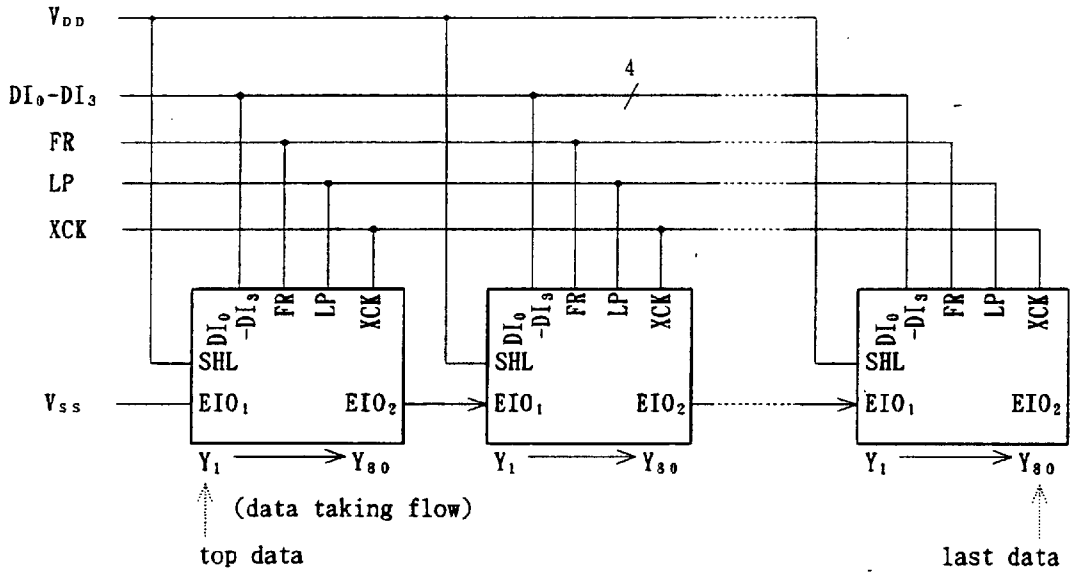
Here, H:V_{DD}(+2.5 to +5.5 V), L:V_{SS}(0 V)

7-2-3. Connection Examples of Plural Segment Drivers

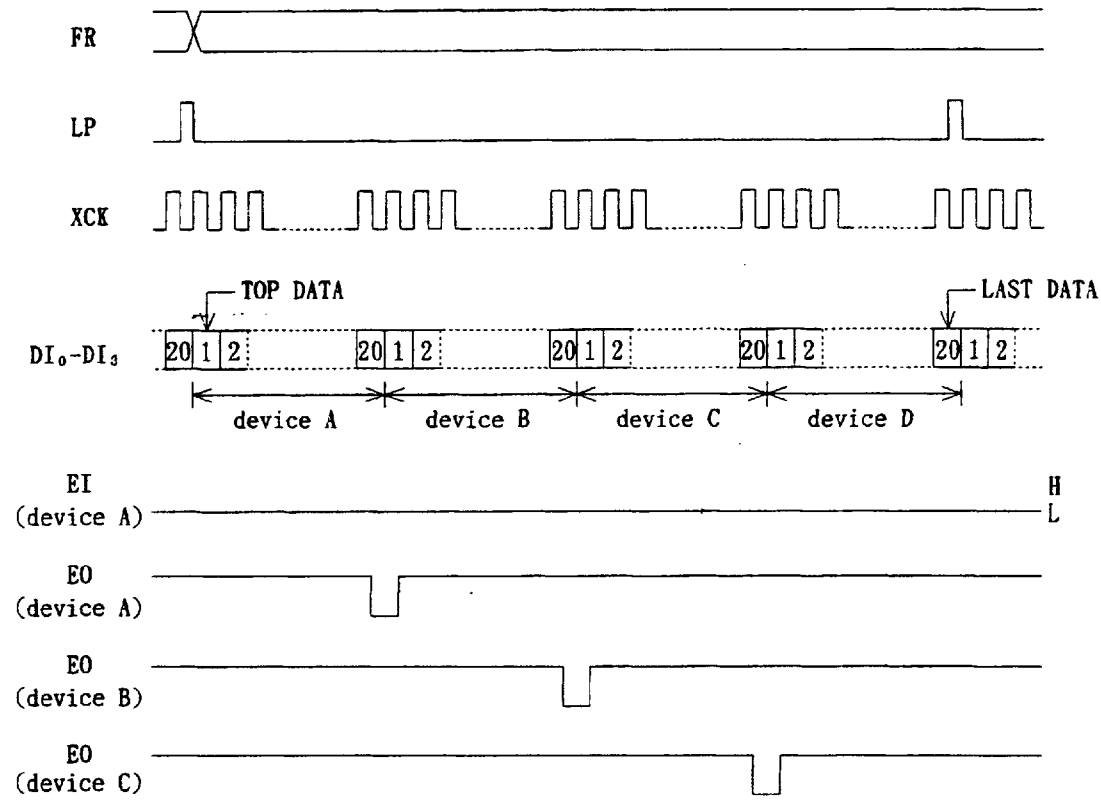
(a) Case of SHL="L"



(b) Case of SHL="H"



7-2-4. Timing Chart of 4-Device cascade Connection

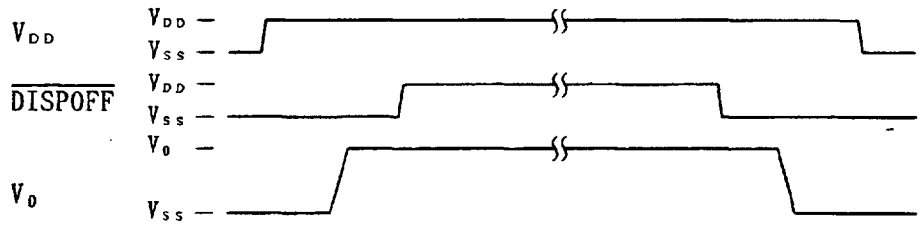


8. Precaution

○Precaution when connecting or disconnecting the power
This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC driver voltage after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC driver voltage.
- We recommend you connecting the serial resistor(50~100 Ω) to the LC driver voltage V_0 of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_S on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0	Referenced to V_{SS}(0 V)	V_{0L}, V_{0R}	-0.3 to +32.0	V
	V_2		V_{2L}, V_{2R}	-0.3 to V_0+0.3	V
	V_3		V_{3L}, V_{3R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-3}, XCK, LP, SHL, FR EIO_1, EIO_2, $\overline{DISPOFF}$	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS}(0 V)	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+10.0		+30.0	V
Operating temperature	T_{opr}			-20		+85	℃

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=V_5=0 V, V_{DD}=+2.5 to +5.5 V, V_0=+10.0 to +30.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DI_{0-3}, XCK, LP, SHL, FR	0.8V_{DD}			V
	V_{IL}		EIO_1, EIO_2, $\overline{DISPOFF}$			0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LI}	$V_{SS}\leqq V_I \leqq V_{DD}$	All input pins		-	±10.0	μA
I/O leakage current	$I_{LI/O}$	$V_{SS}\leqq V_I \leqq V_{DD}$	EIO_1, EIO_2			±10.0	μA
Output resistance	R_{ON}	*1 V_0=+30 V	Y_1-Y_{80}		1.0	1.5	kΩ
		V_0=+20 V			1.5	2.0	
		V_0=+10 V			2.0	3.0	
Stand-by current	I_{STB}	*2	V_{SS}			50.0	μA
Consumed current (1) (Deselection)	I_{DD1}	V_{DD}=+3.0 V *3	V_{DD}			0.6	mA
		V_{DD}=+5.0 V *3				1.0	mA
Consumed current (2) (Selection)	I_{DD2}	V_{DD}=+3.0 V *3	V_{DD}			3.0	mA
		V_{DD}=+5.0 V *3				5.0	mA
Consumed current (3)	I_0	*4	V_{0L}, V_{0R}			1.0	mA

【Note】

*1 : $|\Delta V_{ON}|$=0.5 V

*2 : V_{DD}=+5.0 V, V_0=+30.0 V, V_{IH}=V_{DD}, V_{IL}=V_{SS}

*3 : V_0=+30.0 V, f_{XCK}=6.15 MHz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

*4 : V_{DD}=+5.0 V, V_0=+30.0 V, f_{XCK}=6.15 MHz, f_{LP}=19.2 kHz, f_{FR}=80 Hz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

11-2. AC Characteristics

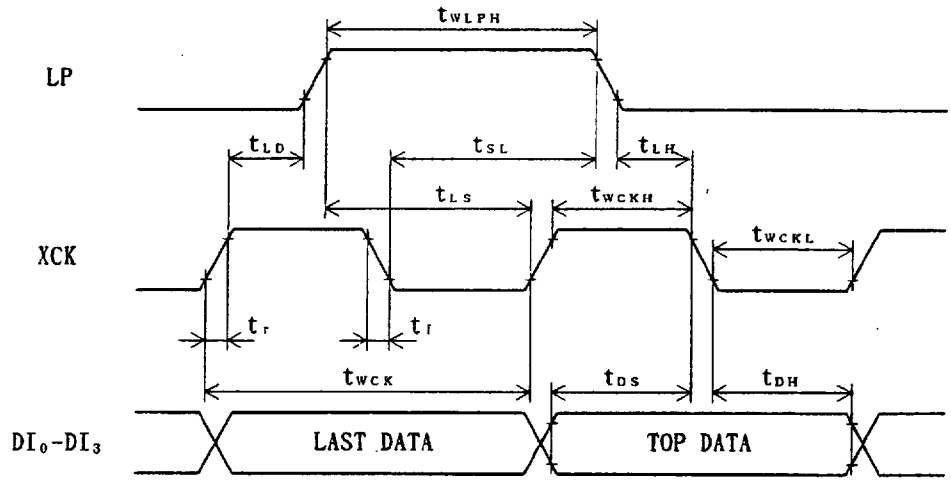
(V_{SS}=V_5=0 V, V_{DD}=+2.5 to +5.5 V, V_0=+10.0 to +30.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t_{WCK}	t_r, t_f≦11 ns	125			ns
Shift clock "H" pulse width	t_{WCKH}		51			ns
Shift clock "L" pulse width	t_{WCKL}		51			ns
Data setup time	t_{DS}		40			ns
Data hold time	t_{DH}		30			ns
Latch pulse "H" pulse width	t_{WLPH}		51			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		51			ns
Latch pulse rise to Shift clock rise time	t_{LS}		51			ns
Latch pulse fall to Shift clock fall time	t_{LH}		51			ns
Enable setup time	t_S		30			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			μs
$\overline{DISPOFF}$ removal time	t_{rem}		100			ns
Input signal rise time	t_r	Note			50	ns
Input signal fall time	t_f				50	ns
Output delay time (1) XCK to EIO_1, EIO_2	t_D	C_L=15 pF			80	ns
Output delay time (2) FR to Y_1-Y_{80}	tpd_1				1.2	μs
Output delay time (3) LP to Y_1-Y_{80}	tpd_2				1.2	μs
Output delay time (4) $\overline{DISPOFF}$ to Y_1-Y_{80}	tpd_3				1.2	μs

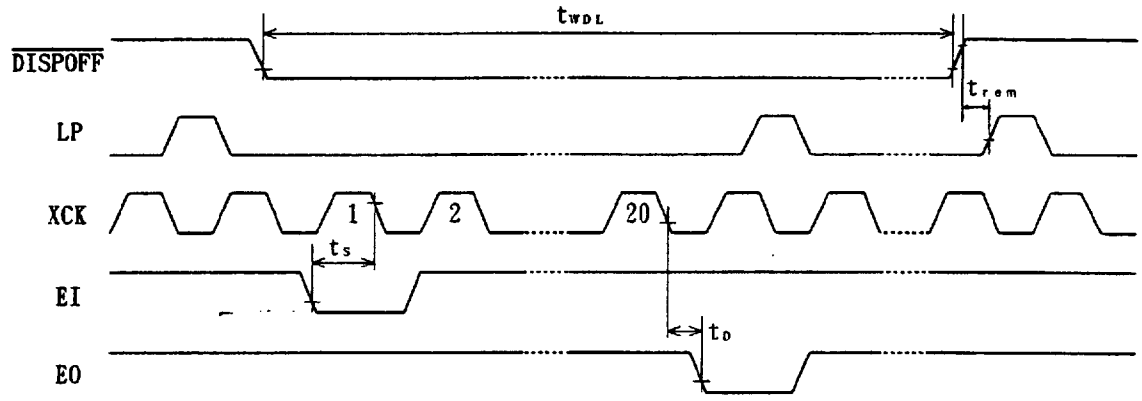
【Note】 (t_{WCK}-t_{WCKH}-t_{WCKL})/2 is maximum in the case of high speed operation.

11-3. Timing Diagrams

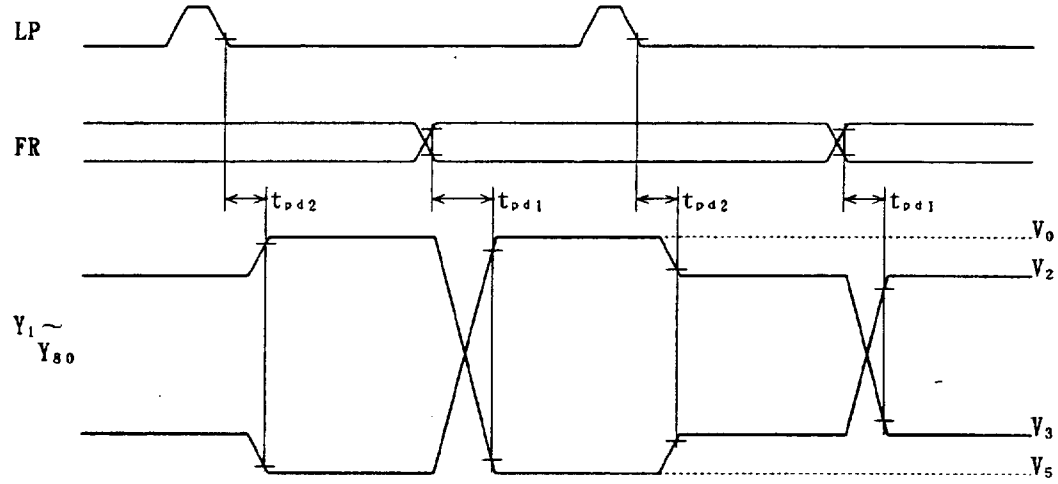
Input Timing Characteristics



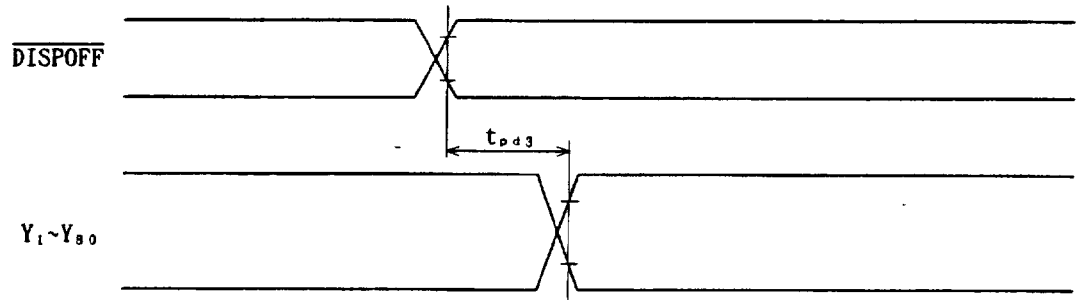
Input/Output Timing Characteristics 1



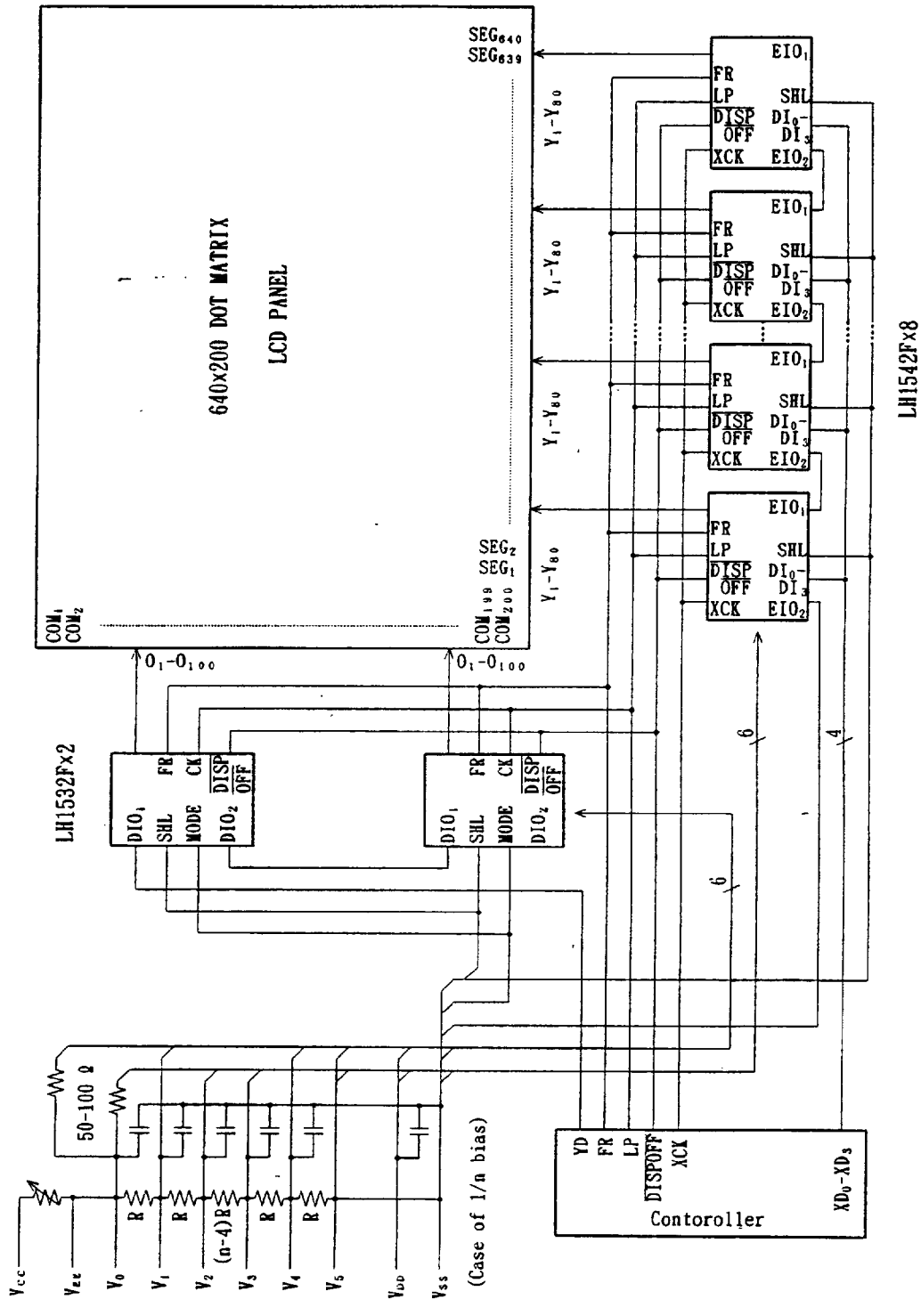
Input/Output Timing Characteristics 2



Input/Output Timing Characteristics 3



12. Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Mim.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V		10		ns

14. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPN2201-00

2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.

   (1) Date code (example) : 4 (a) 37 (b) 0 (c)

   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes the number of times of alteration

3. Packing Specifications

   (1) Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μ mt)	Protects device and prevents ESD (Electro Static Discharge)
Laminated aluminium bag	(520 × 600mm)	Keeping dry.
Adhesive tape paper		Fixing of tape carrier package and sparator.
Carton	Cardboard(420x420x50mm)	Contains a reel.
Label	Paper	Indicates production name, lot.No.. and quantity.
Desiccant	Silica gel	Drying of device

   (2) Packing Form

   a) Tape carrier package(TCP)is wound on a reel with separators 1 and 2 and the ends of them are fixed with adhesive tape.
   b) A label indicating production name. lot no. and quantity is stuck on one side of the reel.
   c) The reel and silica gel is put in a laminated aluminium bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the carton.

* Specification of label

TYPE	
	PRODUCTION NAME LOT NO.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPING DATE

4. Miscellaneous

   (1) The length of the tape carrier is 34 ~ 46 meters maximum per reel, and depends on shipping quantity.

   (2) Before unpacking. prepare a work bench equipped with anti-static devices. Also. the operater shoud ware anti-static wrist bands.

   (3) The device. once unpacked. should be stored in a nitrogen gas, room temperature atomosphere and used within 1 week.

ISSUE DATE	AUG.24.1994	APROVE	CHECK	DESIGN	(NOTE)
ISSUE NUMBER	H6807	A. Suzuki	Y. Honda	T. Kidoguchi	
S/C NUMBER