SHARP

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To :

REFERENCE

# SPECIFICATIONS

Product Type 80 Output LCD Segment Driver built in RAM

Model No. LH1554P

※This tentative specifications contains 41 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: T. Mineyama

T. MINEYAMA
Dept. General Manager

REVIEWED BY: H. Nishioka

PREPARED BY: K. Ohya

ENGINEERING DEPT. 1
LOGIC ENGINEERING CENTER
TENRI INTEGRATED CIRCUITS (IC) GROUP
SHARP CORPORATION

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LH1554P

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Contents

1. Summary

The LH1554P is a dot matrix LC panel system segment driver containing 80 outputs and display RAM.

The driver stores the 8-bit parallel display data from the microcomputer into the internal display RAM and then outputs this RAM data as the LC drive signals.

Since each of the display RAM data bits represents 1 dot on the LC panel, various display patterns data can be easily generated with minimum limits.

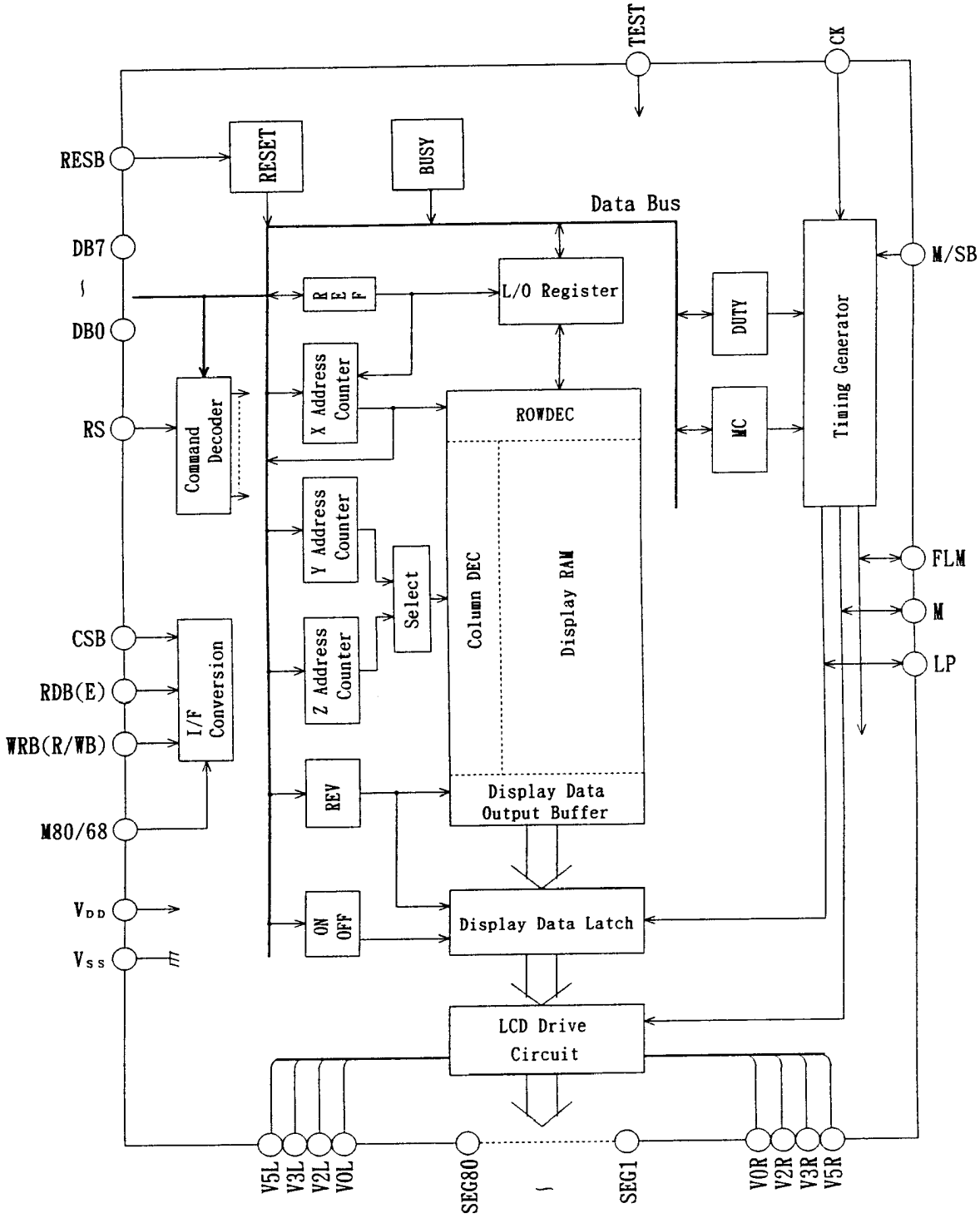
Low power consumption and wide operating voltage enables the chip to be used as interface to LC panel system on battery-powered portable information equipment.

A dot matrix LC display system can be easily configured by using this chip together with the common driver LH1531M (64 output common driver).

2. Features

- Display modes : 2
  Non-inverting mode : RAM data "0" → dot off;RAM data "1" → dot on
  Inverting mode : RAM data "1" → dot off;RAM data "0" → dot on
- Display RAM capacity : 1024 bits(80 x 128)
- Internal display RAM address counter
  Automatic preset of the display start address and automatic address increment
- 8-bit parallel interface for direct connection to the bus of a 8-bit general purpose microcomputer (80 or 68 family)
- Internal LC drive circuits : 80 outputs
- Various command capabilities
  - Display duty ratio settings : selectable 3 types
    1/32, 1/64, 1/128
  - LC AC converting signal frequency settings : selectable 3 types
    Frame frequency, 61 line frequency, 13 line frequency
  - Display start line setting : in unit of line
  - Display on/off control
  - Inverting display/non-inverting display control
  - Display RAM read/write
  - Display RAM address increment control
  - Forward/reverse output control of display drive signal
  - Status read
- Automatic 80-bit display data transfer from display RAM to display data latch
- Power supply
  Logic circuit : 2.5 V to +5.5 V
  LC drive : +10 V to +30 V
- Package : 128PIN QFP
- CMOS silicon gate process(P-silicon substrate)
- Not designed or rated as radiation hardened

3. Block diagram



## 4. Pin description

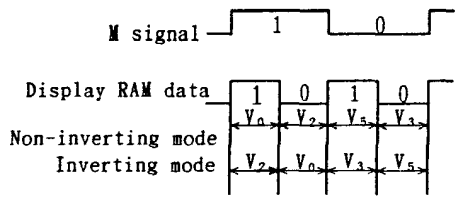
### 4-1. Power supply pins

| Symbol | Pin description |
|---|---|
| $V_{DD}$ | Logic power supply : +2.5 to +5.5 V |
| $V_{SS}$ | GND potential(0 V) |
| $V_{0L}$, $V_{0R}$<br>$V_{2L}$, $V_{2R}$<br>$V_{3L}$, $V_{3R}$<br>$V_{5L}$, $V_{5R}$ | Bias pins of LC drive voltage<br>• Bias voltage pins are usually connected to voltage divider network.<br>• Relationship between voltages should be : $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$<br>• To minimize difference in wave form among LC drive outputs on pins SEG1 through SEG80, connect ViL and ViR(i=0,2,3,5) externally. |

### 4-2. System bus pins

| Symbol | I/O | Pin description |
|---|---|---|
| DB7~DB0 | I/O | 8-bit bidirectional data bus and connects to the data bus of a microcomputer. |
| RS | I | Toggles between command data and display RAM data that will placed on the DB7~DB0.<br>L: display RAM data; H: command data<br>Connects to the address bus of the microcomputer. |
| CSB | I | Active "L" chip select signal. Usually input a decoded address bus signal. |
| RDB<br>(E) | I | • With 80 family microcomputer<br>Connects to $\overline{RD}$ pin of the microcomputer. When "L", this pin is active and the data placed on the LH1554P internal bus are output to the DB7~DB0.<br>• With 68 family microcomputer<br>Connects to E(enable clock input) pin of the microcomputer and active high. |
| WRB<br>(R/WB) | I | • With 80 family microcomputer<br>Connects to $\overline{WR}$ pin of the microcomputer. When "L", this pin is active and the data placed on the DB7~DB0 are read in at "L" to "H" transition.<br>• With 68 family microcomputer<br>Connects to input R/W select signal.<br>H=read; L=write |
| RESB | I | Pulling this pin low starts initializing.<br>The input signal is level_shifted from logic voltage level to LCD drive voltage level inside LCD driver and control LCD drive circuit.<br>When set to Vss level "L" the LCD driver output pins(SEG0~SEG80)are set to level V5.<br>Usually connects to the system reset signal. |
| M80/68 | I | Selects between two microcomputer interface types.<br>L=68 family, H=80 family<br>Usually permanently pulled up or low by external circuit. |

4-3. LCD drive signal

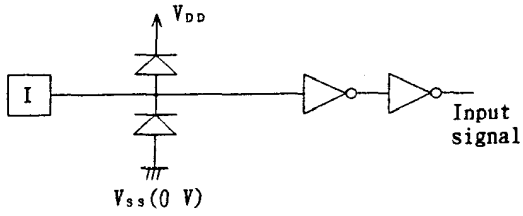
| Symbol | I/O | Pin description |
|---|---|---|
| CK | I | Master clock input which is used to produce the timing clock for internal operation and timing pulse (LP,FLM and M) for LC display. |
| LP | I/O | Display data latch signal which, when goes low, increments the display address counter (Z counter).<br>Also used as the shift clock when connected to CK pin of the common driver LH1531M.<br>Setting of master/slave set pin M/SB<br>M/SB=L(input, slave)<br>M/SB=H(output, master) |
| FLM | I/O | The signal to sync display with common side. High level on this pin sets the display start line address data (content of AZ register) into the address counter(Z counter).<br>Input to the common driver is either on pin DIO1 or DIO2 depending on shift direction.<br>Setting of master/slave set pin M/SB<br>M/SB=L(input, slave)<br>M/SB=H(output, master) |
| M | I/O | AC conversion signal of LC drive output<br>This signal is level_shifted from logic voltage level to LCD drive voltage level inside LCD driver,and control LCD drive circuit.<br>Connects to FR pin of the common driver LH1531M.<br>Setting of master/slave set pin M/SB<br>M/SB=L(input, slave)<br>M/SB=H(output, master) |
| SEG1~ SEG80 | O | Segment drive outputs to LC.<br>Polarity of display RAM data :<br>non-inverting mode : off when "0", on when "1"<br>inverting mode : off when "1", on when "0"<br>One of levels, $V_0$, $V_2$, $V_3$ and $V_5$, is selected according to M signal and display data.<br>  <br><br>※There are two kind of power supply(Logic level voltage,LCD drive voltage)for LCD driver,Please supply regular voltage which assigned by specification for each power pin. |
| M/SB | I | This pin selects between master and slave operation and should be permanently pulled up(H) or pulled down(L).<br>M/SB=L(slave)<br>M/SB=H(master) |

4-4. Remaining pins

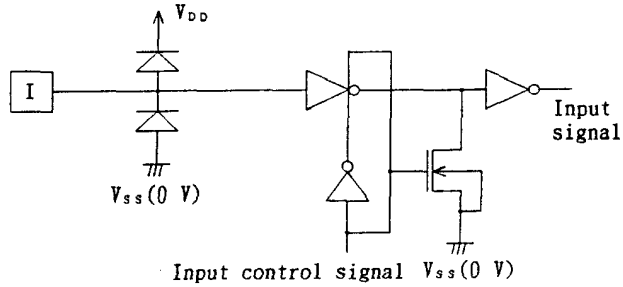
| Symbol | I/O | Pin description |
|---|---|---|
| TEST | I | Testable input pin. Usually should be pulled down(L). |

4-5. Input and output circuit configurations

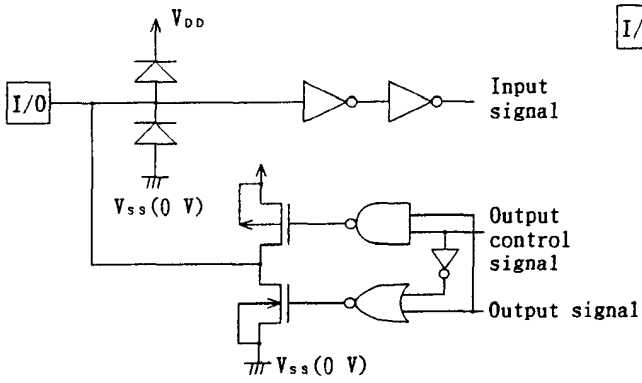
(a-1) Input circuitⅠ
Applicable pins(RS,CSB,RDB, WRB,RESB,M80/68,M/SB,TEST)



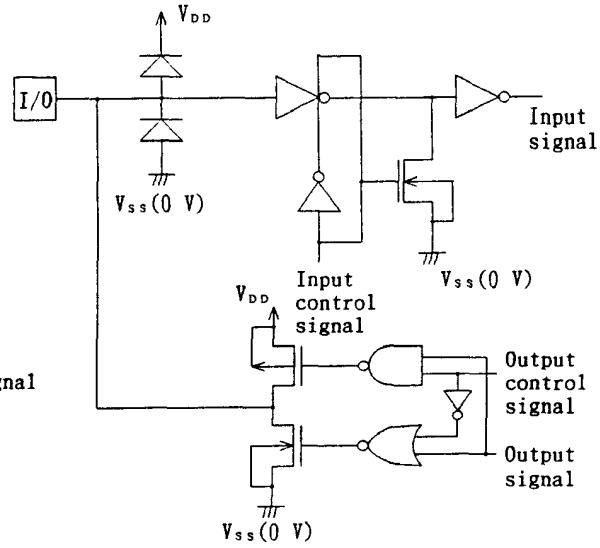

(a-2) Input circuitⅡ
Applicable pin(CK)



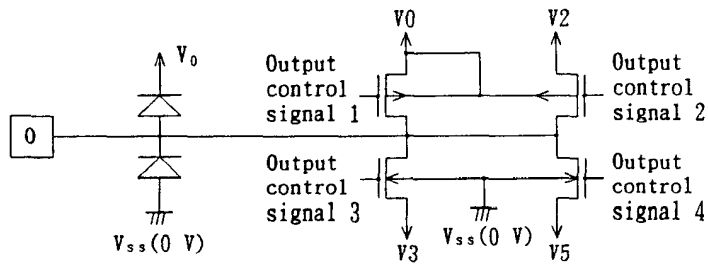

(b-1) Input and output circuitⅠ
Applicable pins(LP,FLM,M)




(b-2) Input and output circuitⅡ
Applicable pins(DB7~DB0)



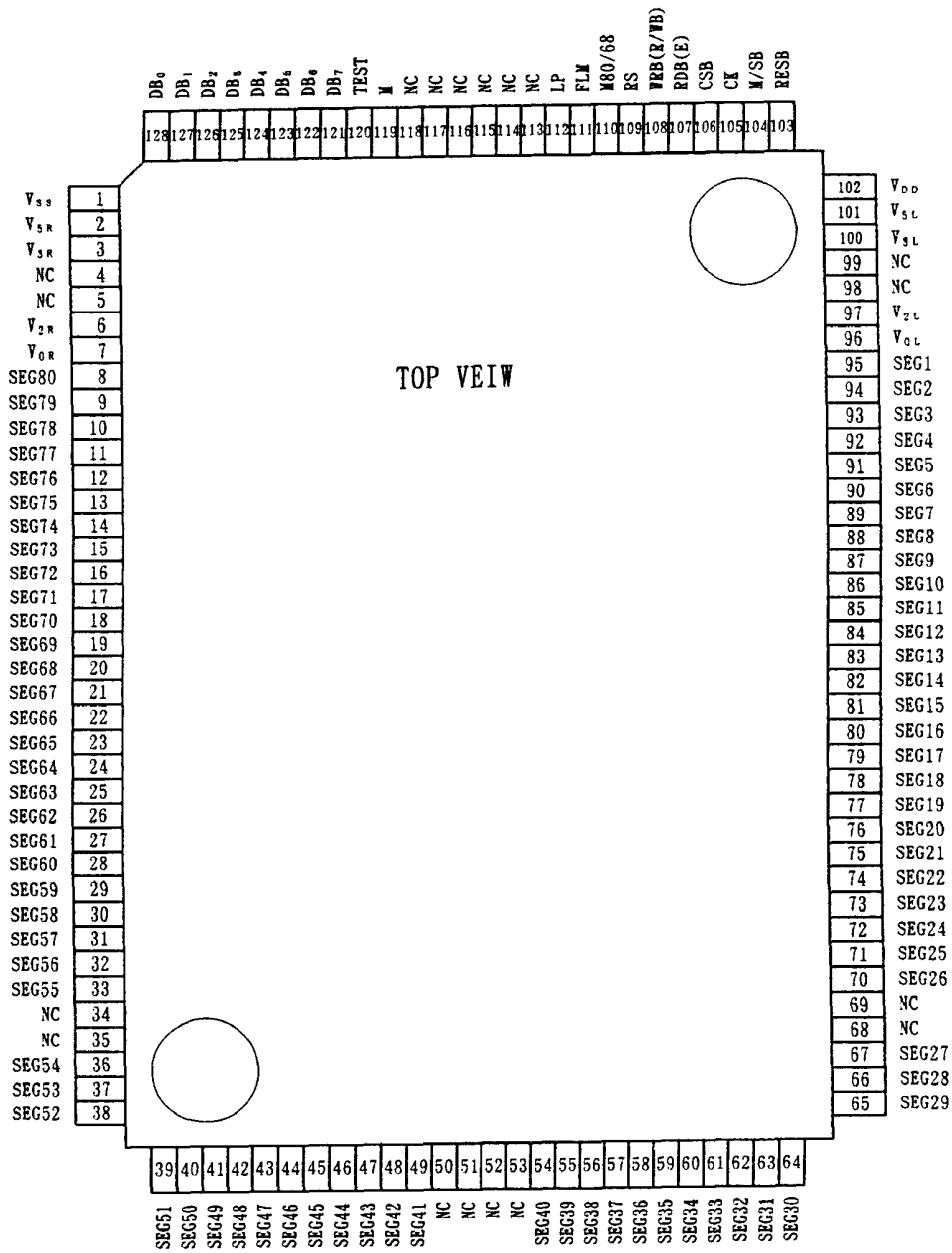

(c) L/C drive output circuit
Applicable pins(SEG1~SEG80)



## 5. Pin

### 5-1. Pin Configuration

LH1554P



5-2 Pin List

| Pin No. | Symbol | I/O | Pin name |
|---|---|---|---|
| 1 | $V_{SS}$ | - | Ground |
| 2, 3 | $V_{5R}$, $V_{3R}$ | - | Power supply for LC drive |
| 4, 5 | NC | - | |
| 6, 7 | $V_{2R}$, $V_{0R}$ | - | Power supply for LC drive |
| 8-33 | SEG55~80 | O | LC drive output |
| 34, 35 | NC | - | |
| 36~49 | SEG41~54 | O | LC drive output |
| 50~53 | NC | - | |
| 54~67 | SEG27~40 | O | LC drive output |
| 68, 69 | NC | - | |
| 70~95 | SEG1~26 | O | LC drive output |
| 96, 97 | $V_{0L}$, $V_{2L}$ | - | Power supply for LC drive |
| 98, 99 | NC | - | |
| 100, 101 | $V_{3L}$, $V_{5L}$ | - | Power supply for LC drive |
| 102 | $V_{DD}$ | - | Power supply for logic system |
| 103 | RESB | I | Reset input |
| 104 | M/SB | I | Master/Slave selection |
| 105 | CK | I | Clock input |
| 106 | CSB | I | Chip select input |
| 107 | RDB(E) | I | 80type:Read signal input, 68type:enable CK input |
| 108 | WRB(R/WB) | I | 80type:Write signal input, 68type:R/W selection |
| 109 | RS | I | Register selection |
| 110 | M80/68 | I | 80type/68type selection |
| 111 | FLM | I/O | First line marker signal input |
| 112 | LP | I/O | Data latch pulse input |
| 113~118 | NC | - | |
| 119 | M | I/O | AC-converting signal input for LC drive wave form |
| 120 | TEST | I | Test mode selection |
| 121~128 | DB7~DB0 | I/O | Data input/output |

## 6. Functional description

### 6-1. Microcomputer interface

#### 6-1-1. Selecting type of interface

The LH1554P's 8 bit data bus can directly connect in parallel, to a general purpose 8 bit microcomputer.
Either 80 or 68 family 8 bit microcomputer interface can be selected by the setting of M80/68 pin.

M80/68=L: 68 family computer interface
M80/68=H: 80 family computer interface

#### 6-1-2. Accessing command register

Data bus I/O pins(DB7(MSB)~DB0(LSB)), chip enable pin CSB, display RAM/register select pin RS, read/write control pin RDB and WRB pin are used when accessing the command register.
If CSB is at high level, the interface is not selected, inhibiting accessing to the command register.
To access the register, be sure to pull CSB low.
Selection between the access to the display RAM data I/O register and access to the command register is through the input to RS.

RS=L: display RAM data I/O register
RS=H: command register

#### 6-1-3. Display RAM data I/O register

The display RAM data I/O register is a combination of input register and output register. The input register temporarily holds the data from the microcomputer, until the data is automatically written into the display RAM.
When writing operating is attempted with RS=L and CSB=L, the data placed on DB7~DB0 is written into the input register on the rising edge of the WRB(with 80 family) or the falling edge of E(68 family).
The output register temporarily holds the data read from the display RAM. The data is then read by the microcomputer.
When reading operating is attempted with RS=L and CSB=L, the data stored in the output register is placed on DB7~DB0 while the RDB=L(80 family) or while the E=H(68 family). Upon completion output register data reading, the register is automatically filled with the data read from the display RAM.
At the same time, the address is also advanced according to the setting in the automatic increment mode.
Because the data in the display RAM is read through the output register, the first reading operation after an address setting cannot reach the display data stored in the display RAM, at the addressed location; the second reading operation will reach that memory location. The first display RAM reading should be designed as a dummy reading. The read timing diagram is shown in Fig.6-1-3.

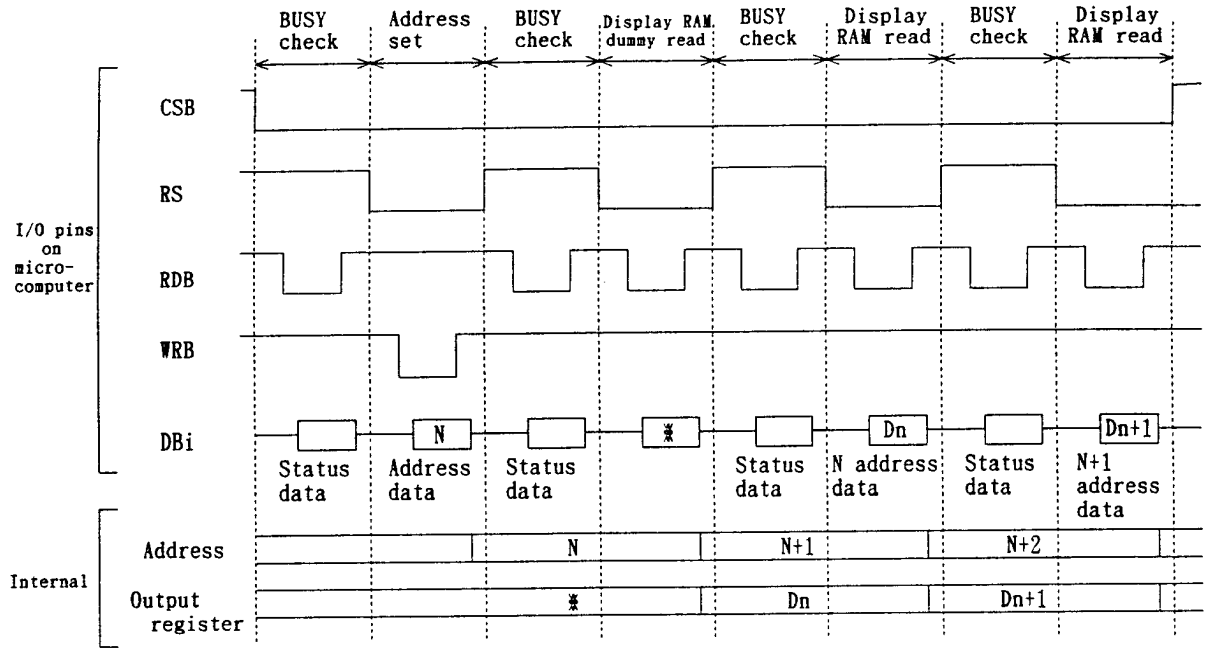



Fig.6-1-3(a) Display RAM and timing diagram

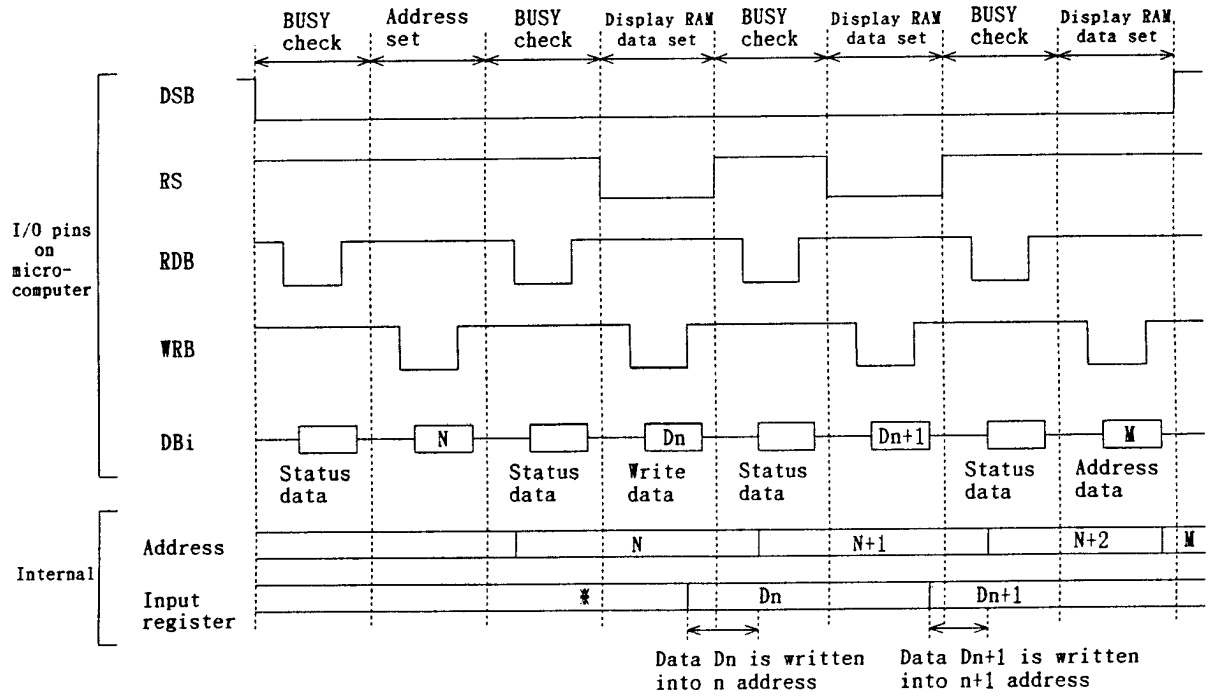



Fig.6-1-3(b) Display RAM write timing diagram

Notes: • BUSY check may be repeated until BUSY=0 is verified.
• The address shown is being incremented.

6-2. BUSY check

The BUSY flag, when at "1" level, shows that current operation is internal and that all commands but the status read are illegal. Any of these command must be issued while BUSY flag is at "0" level. Exception: When SRCH=1, BUSY check is not necessarily before register reading(other than status) or command writing.

6-3. Display RAM

6-3-1. Addressing display RAM

The display RAM contains 80 x 128 bits of memory locations which can be accessed in unit of 8 bits denoted by X and Y addresses from the microcomputer.

Means can be provided to automatically increment the X and Y addresses through the address control register. The addresses are incremented each time the microcomputer reads or writes the display RAM.

Further information is found in command description.

Figure 6-3 shows the display RAM configuration.

A row is selected by the X address and a column by the Y address.

The X addresses of $A_H$~$F_H$ are reserved: do not use these X addresses.

The column address is an 80 bits Z address data read into the display data latch circuit at line frequency on the rising edge of the LP, and then output from the display data latch circuit on the falling edge of the LP. The Z address is the value of the AZ register preset into the Z address counter while the FLM signal output at the frame frequency is at high state. The address is incremented in synchronous with the input LP signal.

The incrementing loop depends on the duty ratio. For further information, see the command description.

The Z address counter operates in synchronous with other LC display related timing signals, and independently of the X and Y address counters.

For the AZ address register, specify the column line of the display RAM to be displayed on the top line.

This is mainly used to change page and screen scrolling.

6-3-2. Display RAM data vs LC display

One bit of display RAM data represents one dot on the LC display.

The status of each dot depends on the non-inverting display/inverting display setting of the REV register.

- With non-inverting display(REV=0): dot is off when RAM data="0"
  dot is on when RAM data="1"
- With inverting display(REV=1): dot is on when RAM data="0"
  dot is off when RAM data="1"

6-3-3. Display output SEG forward/reverse setting

Reversing the display RAM accessing from the microcomputer through the REF register, reverses the output order of the display outputs SEG1~SEG80.

For further information, see the command description.

REF=0, then DB0(LSB)~DB7(MSB)

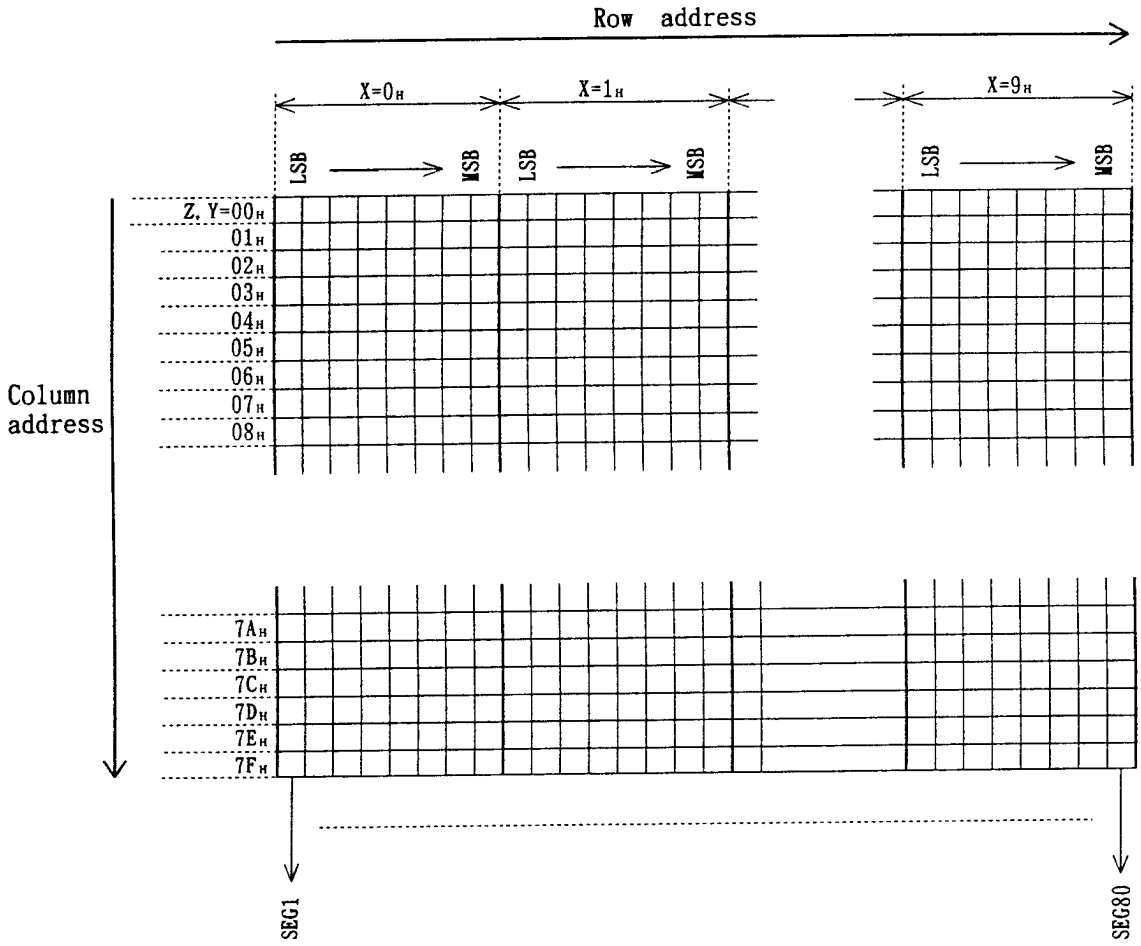



Fig.6-3 Display RAM configuration vs SEG outputs

6-4. Timing generator

The timing generator derives the timing clock for internal operation and the timing pulse(LP,FLM,M) for LC display from the master clock CK. The state of the timing pulse pins and timing generator are shown in Fig.6-4.

| H/SB pin | Mode | LP pin | M pin | FLM pin | State of timing generator |
|---|---|---|---|---|---|
| L | Slave | In | In | In | LP,M,FLM gen. circuits stop |
| H | Master | Out | Out | Out | Operating |

Fig.6-4 State of the timing pulse pins and timing generator

For signals LP, M and FLM, see 4-3 LCD drive circuit signals.

6-5. Initial settings

Placing low level on the RESB pin starts initial.
During initial sequence, RESET flag in the status register is "1", requiring inhibition of operations other than the status register reading.
When changing default settings after the initial, first set the value of the REF register, DUTY register and MC register.

Fig.6-5 Default settings

| Block | | Default setting | |
|---|---|---|---|
| Display RAM | | Unknown | |
| Pins DB0～DB7 | | Input mode | |
| Registers | Y address register | AY6~0=$00_H$ | Column address $00_H$ |
| | X address register | AX3~0=$00_H$ | Row address $0_H$ |
| | Status read selector | SRCH=0 | Status read mode |
| | Z address registers | AZ6~0=$00_H$ | Display starting line: 1st line |
| | X, Y address increment | AIM,AYI,AXI=0 | No increment |
| | M signal period | MC1,0=$0_H$ | Duty ratio x LP(frame period)/2 |
| | Duty ratio | DUTY1,0=$0_H$ | 1/128 |
| | Display control | REF=0,REV=0, ON/OFF=1 | SEG1~SEG80 in normal order, non-inverting, display off |
| | LC output SEG1~SEG80 pins | Output is at $V_5$ level during RESB=L. | |

## 7. Command functions

### 7-1. Commands

| Command | CSB | RS | DB 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Setting by RDB(E),WRB(R/WB) Read mode | Write mode | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display RAM I/O | 0 | 0 | VRAM7~0 (Don't care) | | | | | | | | Read on SRCH=0 | Write on SRCH=0 | DBi ↔ VRAMi read /write(i=0~7) |
| Y address | 0 | 1 | 1 | AY6~0 ($00_H$) | | | | | | | Set SRCH to "1". ↓ Write command code. ↓ Read data code. Return SRCH to "0" | Write on SRCH=0 | Set display RAM column address /read |
| X address | 0 | 1 | 0 | 0 | 0 | 0 | AX3~0 ($0_H$) | | | | | | Set display RAM row address /read |
| Status read select | 0 | 1 | 0 | 0 | 0 | 1 | | | | SRCH(0) | | | Set read register selection. |
| Z address (LSB) | 0 | 1 | 0 | 0 | 1 | 0 | AZ3~0 ($0_H$) | | | | | | Set column address of display RAM to be displayed on top of LCD/read |
| Z address (MSB) | 0 | 1 | 0 | 0 | 1 | 1 | | AZ6~4 ($0_H$) | | | | | |
| X,Y address increment control | 0 | 1 | 0 | 1 | 0 | 0 | | AIM(0) | AYI(0) | AXI(0) | | | Controls increment operation of X and Y address counters. |
| Set M signal period, duty ratio | 0 | 1 | 0 | 1 | 0 | 1 | MC 1,0 ($0_H$) | | DUTY 1,0 ($0_H$) | | • SRCH register cannot be read. | | Set M period /read (3 types) / Set duty ratio /read (3 types) |
| Display control | 0 | 1 | 0 | 1 | 1 | 0 | | REF(0) | REV(0) | ON OFF (1) | | | • ON/OFF: Display on/off<br>• REV: Invert black and white<br>• REF: Set SEG out order(F/R) |
| Read status | 0 | 1 | BUSY | RESET | ON OFF | REV | AX3~0 | | | | Read on SRCH=0 | — | • BUSY: Internal operation state<br>• RESET: Default settings<br>• Other bits: register value |

Note: Figures in parentheses are default settings.

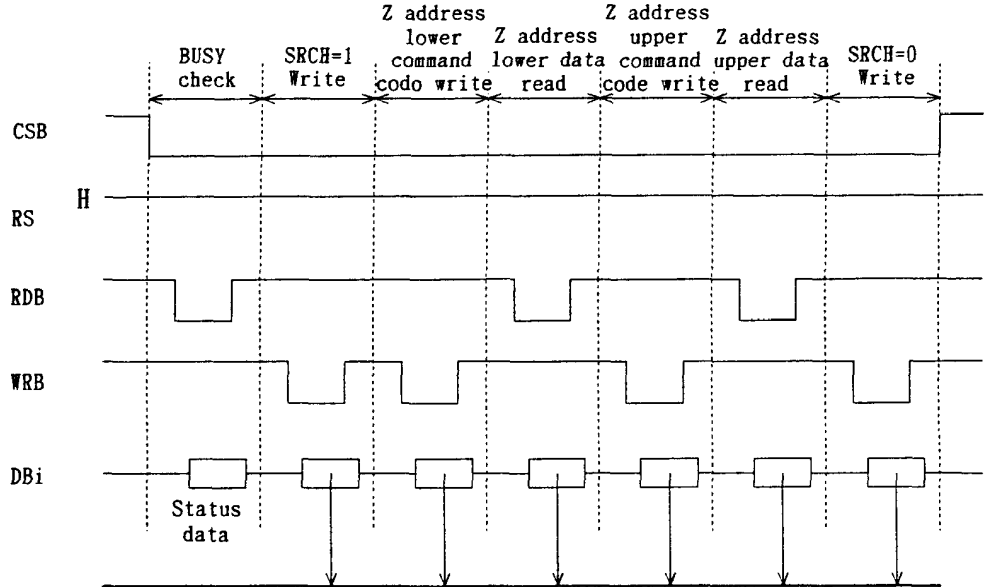
7-2. Functions of command

This section details the commands listed in section 7-1.
Definitions of data code and command code are given below.
for commands to be issued, the chip enable is established(CSB=L).

Example: X address

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | AX3 | AX2 | AX1 | AX0 |
| ← Command code → | | | | | ← Data code → | | | |

Undefined command codes and DB7, DB6, DB5, DB4=(0,1,1,1) are inhibited.
The SRCH controls read operation as follows:
When read operation is performed with SRCH at "0" level, the content of the display RAM output register is placed on the bus when RS=0, or the status data is placed on the bus when RS=1.
To read a register other than display RAM output register and status data register, write "1" to SRCH, write the command code of the command register to be read, and then start read operation. The content of register (data code) is placed on the bus. After reading, reset SRCH to "0".
The data is written into the display RAM input register when SRCH="0" and RS="0". With SRCH="1", BUSY check is not required when writing a command or reading the register.




| | | | | | | |
|---|---|---|---|---|---|---|
| DB7 | 0 | 0 | * | 0 | * | 0 |
| DB6 | 0 | 0 | * | 0 | * | 0 |
| DB5 | 0 | 1 | * | 1 | * | 0 |
| DB4 | 1 | 0 | * | 1 | * | 1 |
| DB3 | $*_F$ | $*_F$ | AZ3 | $*_F$ | * | $*_F$ |
| DB2 | $*_F$ | $*_F$ | AZ2 | $*_F$ | AZ6 | $*_F$ |
| DB1 | $*_F$ | $*_F$ | AZ1 | $*_F$ | AZ5 | $*_F$ |
| DB0 | 1 | $*_F$ | AZ0 | $*_F$ | AZ4 | 0 |

* Don't care

$*_F$ Permanently 1 or 0

Fig.7-2 SRCH settings and command/data read timing

7-3. Command description

In the following tables, symbol *means don't care and $*_F$ means the level is held at "0" or "1".
The SCRH is the register value.

7-3-1. Display RAM input and output

(a) Writing data into display RAM input register

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Display RAM write data | | | | | | | |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

This command places 8 bit data into the display RAM register, the data is then written into the specified X and Y address locations.
See Fig.6-1-3(b).

(b) Reading display RAM output register

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Display RAM write data | | | | | | | |

Initial status(May change ⟶ May change)

| RDB | WRB | CSB |
|---|---|---|
| Read mode | | 0 |

| SRCH |
|---|
| 0 |

This command places content of the display RAM register on the data bus and at the same time, transfers the display RAM data at the specified X and Y address locations to the output register. One dummy read is required after setting X and Y addresses. See Fig.6-1-3(a).

7-3-2. Y address

(a) Setting Y address

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | AY6 | AY5 | AY4 | AY3 | AY2 | AY1 | AY0 |

Initial status(0 ⟶ 0)

| RDB | WRB | DSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

This command sets the column address of the display RAM.
The 7 bit preset value AY6~AY0 is set to the Y address counter whose output specifies the column address.
Increment procedure of the Y address counter is detailed in 7-3-6.(a).
The value of AY6~AY0 is from $00_H$ to $7F_H$.

(b) Reading Y address counter

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | $*_F$ | $*_F$ | $*_F$ | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | AY6 | AY5 | AY4 | AY3 | AY2 | AY1 | AY0 |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH |
|---|
| 1 |
| 1 |

The outputs AY6~AY0 of the Y address counter, instead of Y address set data, are placed on the bus.
The data AY6~AY0 is not equal to that in para.(a)above. If the counter is set to automatically increment the counts, the address to be read also increments.
For command code writing and data code reading procedures, see section 7-2.

7-3-3. X address

(a) X address set

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | AX3 | AX2 | AX1 | AX0 |

Initial status(0 ⟶ 0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

This command sets the Row address of the display RAM.
The 4 bit preset value AX3~AX0 is set to the X address counter whose output denotes the Row address.
The value of AX3~AX0 can be from $0_H$~$9_H$ and $A_H$~$F_H$ cannot be used.
If the SEG output order set register REF is set at "0"(forward), the value AX3~AX0 is set to the X address counter at it is, and the counter operates as the up-counter, incrementing the Row address.
If the REF is set at "1"(reverse), the value $9_H$-$(AX3\sim AX0)_H$ is set to the X address counter which this time operates as down-counter, decrementing the Row address.
For incrementing and decrementing operations, see section 7-3-6(a).

(b) Reading X address counter

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | * | * | * | AX3 | AX2 | AX1 | AX0 |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH | |
|---|---|
| 1 | ← Write |
| 1 | ← Data code read |

Command code

The outputs of the X address counter, instead of the X address set data, are read.
The data AX3~AX0 here is not equal to that in para. (a)above.
If REF is set at "1"(reverse order), the X address counter decrements from the maximum value so that the data is read in the reverse order.
Procedures of command code writing and data code reading are as described in section 7-2.Reading can be through the status reading method which is recommended in terms of software efficiency.

7-3-4. Status read changeover

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | $*_F$ | $*_F$ | $*_F$ | SRCH |

Initial status(0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

SRCH must be set to "1" only when reading the contents of Y address counter, X address counter, Z address counter, X and Y address increment control registers, M signal period setting register, duty ratio setting register and display control register. Reset the SRCH to "0" after reading: hold the SRCH at "0" level when not reading these registers. Also hold SRCH at "0" level when performing writing data into these registers, or reading/writing the display RAM I/O registers, reading status. See section 7-1 Command list. Note that SRCH cannot read.

7-3-5. Z address

(a) Z address set

Z LSB address set

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | AZ3 | AZ2 | AZ1 | AZ0 |

Initial status(0 ⟶ 0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

Z MSB address set

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | $*_F$ | AZ6 | AZ5 | AZ4 |

Initial status(0 ⟶ 0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

Specify the Z address of the display RAM by using AZ6~AZ0 to denote the data to be displayed on the top of the LC screen.
The address AZ6~AZ0 is separated into the MSB command(AZ6~AZ4) and LSB(AZ3~AZ0).
The display can be scrolled up/down by incrementing and decrementing the AZ6~AZ0.
The Z address is incremented by the Z address counter in unit of a line but the unit may vary depending on the settings of duty ratio which is described in the section under the title duty ratio setting register.

(b) Reading Z address counter

Reading LSB of the Z address counter

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | * | * | * | AZ3 | AZ2 | AZ1 | AZ0 |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH | |
|---|---|
| 1 | ← Command code write |
| 1 | ← Data code read |

Reading MSB of the Z address counter

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | * | * | * | * | AZ6 | AZ5 | AZ4 |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH | |
|---|---|
| 1 | ← Command code write |
| 1 | ← Data code read |

Outputs AZ6~AZ0 of the Z address counter are placed on the bus.
These bits are read in unit of lower bits(AZ3~AZ0) and upper bits(AZ6~AZ4).
The Z address counter is read line by line.

7-3-6. XY address increment control

(a) XY address increment control mode set

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | $*_F$ | AIM | AYI | AXI |

Initial status(0 ⟶ 0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

This register directs AIM, AYI and AXI registers whether to increment the X and Y address counters after each read or write of the display RAM I/O registers.
This register allows the microcomputer to access continuous addresses of the display RAM.

The registers AIM, AYI and AXI control the increments of the X and Y address counters as follows:

| AIM | Selection of increment timing | Note |
|---|---|---|
| 0 | Display RAM reading and writing | (1) |
| 1 | Writing into the display RAM(read modify) | (2) |

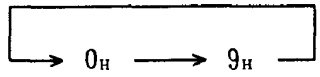
(1) Valid when writing into or reading from continuous address field.
(2) Valid when reading a location of continuous addresses, modifying the data and then writing it back into the location.

| AYI | AXI | Selection of address incrementing | Note |
|---|---|---|---|
| 0 | 0 | No increment | (1) |
| 0 | 1 | X address automatic increment | (2) |
| 1 | 0 | Y address automatic increment | (3) |
| 1 | 1 | X and Y addresses automatic continuous increment | (4) |

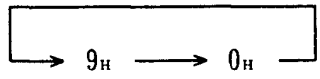
(1) X and Y addresses are not incremented irrespective of AIM setting.
(2) Incremented or decremented according to the AIM setting.

The X address is incremented or decremented in the order shown below, depending on the status of the SEG output forward/reverse setting register REF.

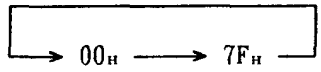
- When REF=0, the address increments from $0_H$ to $9_H$, then back to $0_H$.




- When REF=1, the address decrements from $9_H$ to $0_H$, then back to $9_H$.

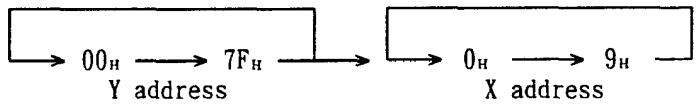



(3) The Y address is incremented for the purpose specified by the setting of AIM.

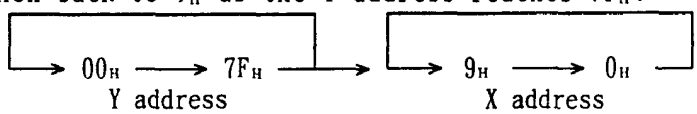



(4) The X address increments or decrements in conjunction with the cycle of the Y address, as illustrated below.

- When REF=0(forward), the X address increments from $0_H$ to $9_H$, then back to $0_H$ as the Y address reaches $7F_H$.




- When REF=1(reverse), the X address decrements from $9_H$ to $0_H$, then back to $9_H$ as the Y address reaches $7F_H$.



7-3-7. M signal period and duty ratio

(a) M Signal period setting, duty ratio setting

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | MC | MC | DUTY | DUTY |
| | | | | | 1 | 0 | 1 | 0 |

Initial status(0 ⟶ 0)

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

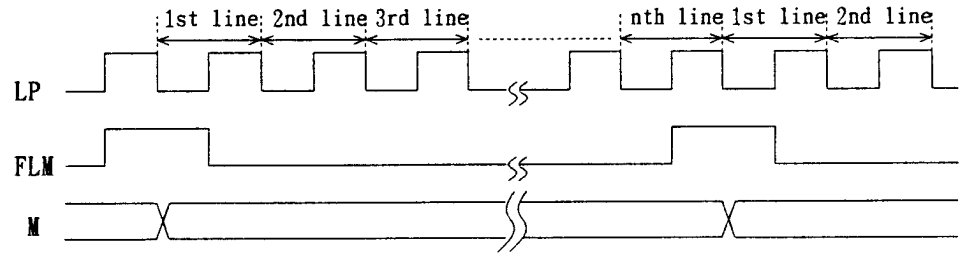
| SRCH |
|---|
| 0 |

The cycle of LC AC conversion signal M is determined by MC1 and MC0. The duty ratio of the signal is 50% and the period of half cycle is as shown in the table below.

Table 7-3-7(a)

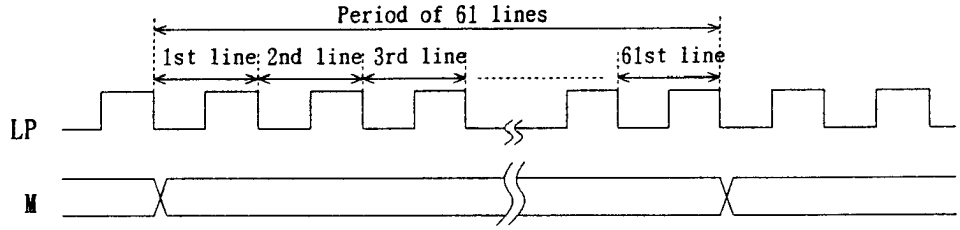
| MC1 | MC0 | Half cycle of LCD AC conversion signal | Timing diagram |
|---|---|---|---|
| 0 | 0 | FLM period(varies with duty ratio) | (1) |
| 0 | 1 | 61x1 Line period | (2) |
| 1 | 0 | 13x1 Line period | (3) |
| 1 | 1 | invalid | – |

〈Timing diagram(1)〉

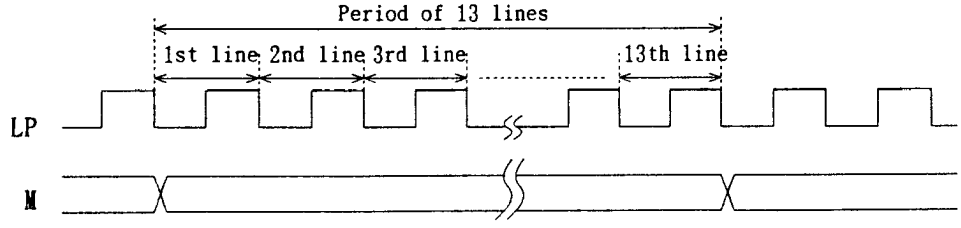



*n=128,64 or 32, depending on duty ratio

〈Timing diagram(2)〉




〈Timing diagram(3)〉

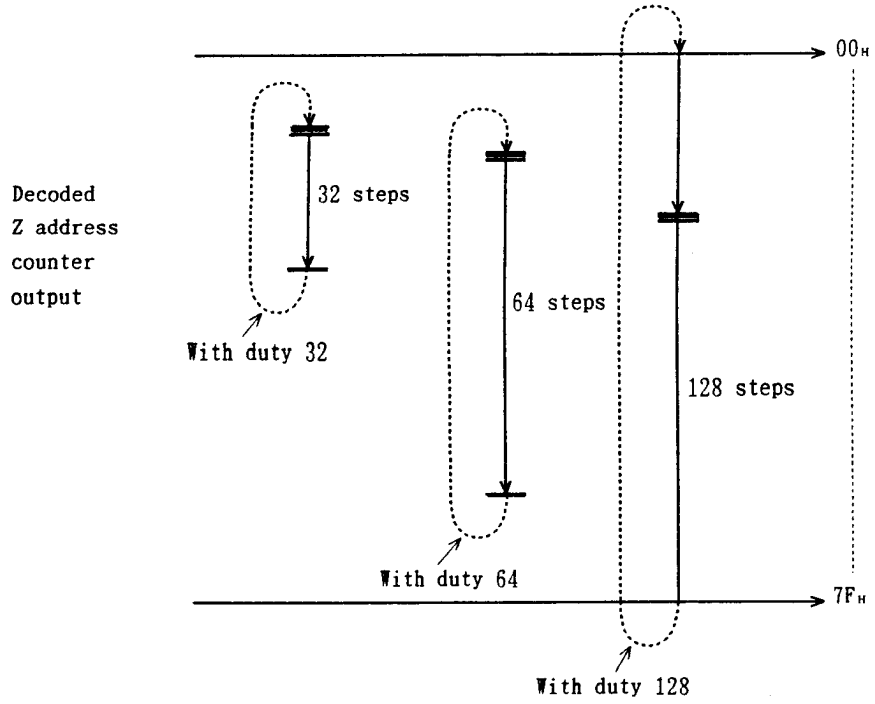


DUTY1 and DUTY0 sets the duty ratio.
The duty ratio determines the FLM period and the steps of the Z address increment.
Table below shows the duty ratio settings.

Table 7-3-7(b)

| DUTY1 | DUTY2 | DUTY ratio | FLM period | Z address count step |
|---|---|---|---|---|
| 0 | 0 | 1/128 | 128x1 line | 128 steps |
| 0 | 1 | 1/64 | 64x1 line | 64 steps |
| 1 | 0 | 1/32 | 32x1 line | 32 steps |
| 1 | 1 | invalid | – | – |

The column address data(AZ6~AZ0) of the display RAM, to be displayed on the top line of the display, is written into the Z address counter when the FLM signal goes high. The Z address counter increments is count on the falling edge of the 1 line period signal LP, up to the steps determined by the duty ratio setting shown in table 7-3-7(b).
This procedure is shown in Fig.7-3-7.




As can be seen from the above figure, all display RAM area can be utilized when duty ratio is 64.
The start point(value of AZ6~AZ0, marked ▬) is in the range $00_H$~$7F_H$.
The Z address counter returns to $00_H$ after $7F_H$.

Fig.7-3-7 Relationship between duty ratio and Z address counter.

(b) Reading M signal period setting and duty ratio setting

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | * | * | * | MC 1 | MC 0 | DUTY 1 | DUTY 0 |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH | |
|---|---|
| 1 | ← Command code write |
| 1 | ← Data code read |

The start point can be monitored by writing the command code and reading data code by following the procedure described in section 7-2.

7-3-8. Controlling display

(a) Display control data bit set

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | $*_F$ | REF | REV | ON/OFF |
| | | | | | | Initial status(0 | 0 | 1) |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |

| SRCH |
|---|
| 0 |

(a-1) Turning on/off the display

On/off data bit turns on/off all display.

| ON/OFF | Display status | Remarks |
|---|---|---|
| 1 | Turns off all display | Contents of the display RAM remain unchanged. The display data latch circuit is controlled according to display status (inverting or non-inverting). |
| 0 | Turns on display | Contents of display RAM are displayed. |

(a-2) Controlling non-inverting/inverting

The display RAM data turns on or off corresponding dots on the display according to the REV data bit setting and display mode (inverting or non-inverting).

| REV | Display status |
|---|---|
| 0 | Non-inverting mode • display RAM data "0"=LCD dots off<br>• display RAM data "1"=LCD dots on |
| 1 | Inverting mode • display RAM data "0"=LCD dots on<br>• display RAM data "1"=LCD dots off |

(a-3) Setting forward/reverse order of SEG1~SEG80 outputs

The REF data bit determines the access direction of X address of the display RAM from the microcomputer, i.e. writing order of the data. See table 7-3-8.

Ability of reversing order of SEG outs and X address relieves the LC panel designers from chip layout limits.

Table 7-3-8 REF setting vs display RAM accessing direction and SEG output order

| REF | Setting by micro-computer | | Display RAM to be written | | SEG outputs | State |
|---|---|---|---|---|---|---|
| | X address set | Data | Row address | Data | | |
| 0 | $N_H$ | DB0(LSB)<br>⋮<br>DB7(MSB) | $N_H$ | LSB<br>⋮<br>MSB | $SEG_{8\times N+1}$<br>⋮<br>$SEG_{8\times N+8}$ | Non-inv. |
| 1 | $N_H$ | DB0(LSB)<br>⋮<br>DB7(MSB) | (*)<br>$9_H-N_H$ | MSB<br>⋮<br>LSB | $SEG8x_{(9H-NH)+8}$<br>⋮<br>$SEG8x_{(9H-NH)+1}$ | Inv. |

* When REF=1, data $9_H$~$N_H$ is read from the X address counter.

(b) Display control data bit read

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | $*_F$ | $*_F$ | $*_F$ | $*_F$ |
| 1 | * | * | * | * | * | R<br>E<br>F | R<br>E<br>V | ON/<br>OFF |

| RDB | WRB | CSB |
|---|---|---|
| Write mode | | 0 |
| Read mode | | 0 |

| SRCH | |
|---|---|
| 1 | ← Command code write |
| 1 | ← Data code read |

* Writing of command code and reading of data code are conducted by following the procedure described in section 7-2.
* Preferably, status read be used to read REV and on/off data bits.

7-3-9. Status read

| RS | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| 1 | BUSY | RESET | ON/<br>OFF | R<br>E<br>V | A<br>X<br>3 | A<br>X<br>2 | A<br>X<br>1 | A<br>X<br>0 |

| RDB | WRB | CSB |
|---|---|---|
| Read mode | | 0 |

| SRCH |
|---|
| 0 |

Note that SRCH must be at "0" during status.
Contents of read data are as shown below.

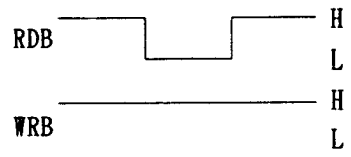
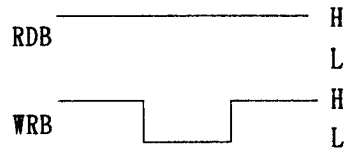
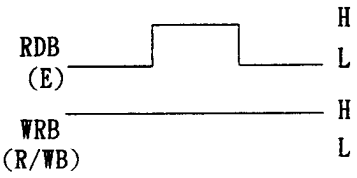
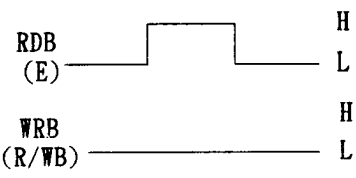
Table 7-3-9

| | | |
|---|---|---|
| BUSY | 0:ready | 1:Internal operation in process |
| RESET | 0:Operating status | 1:Initializing |
| ON/OFF | 0:Display off | 1:Display on |
| REV | 0:Non-inverting display | 1:Inverting display |
| AX3<br>AX2<br>AX1<br>AX0 | Status of X address counter | |

7-3-10. Read mode and write mode

Set the mode as follows according to the type of microcomputer interface.

Table 7-3-10

| | Read mode | Write mode |
|---|---|---|
| 80 family |  |  |
| 68 family |  |  |

8. Precaution

○Precaution when connecting or disconnecting the power

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating.

The detail is as follows.

- When connecting the power supply, connect the LC driver voltage after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC driver voltage.
- We recommend you connecting the serial resistor(50~100 Ω) to the driver voltage $V_{OL(R)}$ of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

9. Absolute maximum ratings

| Parameter | Symbol | Test condition | Pins | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage(1) | $V_{DD}$ | With respect to $V_{SS}$(0 V) Ta=+25 ℃ | $V_{DD}$ | -0.3~+7.0 | V |
| Supply voltage(2) | $V_0$ | | $V_{0L}$,$V_{0R}$ | -0.3~+32.0 | V |
| | $V_2$ | | $V_{2L}$,$V_{0R}$ | -0.3~$V_0$+0.3 | V |
| | $V_3$ | | $V_{3L}$,$V_{3R}$ | -0.3~$V_0$+0.3 | V |
| | $V_5$ | | $V_{5L}$,$V_{5R}$ | -0.3~$V_0$+0.3 | V |
| Input voltage | $V_I$ | | DB7~DB0,RS,CSB RDB,WRB,RESB M80/68,CK,LP,FLM M,M/SB,TEST | -0.3~$V_{DD}$+0.3 | V |
| Storage temperature | Tstg | | | -45~+125 | ℃ |

10. Recommended operating conditions

| Parameter | Symbol | Pin | MIN. | TYP. | MAX. | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | +2.5 | | +5.5 | V | Note1 |
| Recommended operating voltage | $V_0$ | $V_{0L}$,$V_{0R}$ | +10.0 | | +30.0 | V | Note2 |
| Operating temperature | Topr | | -20 | | +85 | ℃ | |

Note1: With respect to $V_{SS}$

Note2: Levels of voltages must be: $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$

11. Electrical characteristics

11-1 DC characteristics

Unless otherwise noted: $V_{SS}=V_5=0$ V, $V_{DD}=+2.5$~$+5.5$ V, $V_0=+30.0$ V, Ta=-20~+85 ℃

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Input high voltage(1) | $V_{IH1}$ | | | 0.8$V_{DD}$ | | $V_{DD}$ | V | (1) |
| Input low voltage (1) | $V_{IL1}$ | | | 0 | | 0.2$V_{DD}$ | V | (1) |
| Input high voltage(2) | $V_{IH2}$ | | | 0.8$V_{DD}$ | | $V_{DD}$ | V | (2) |
| Input low voltage (2) | $V_{IL2}$ | | | 0 | | 0.2$V_{DD}$ | V | (2) |
| Output high voltage(1) | $V_{OH1}$ | $I_{OH}$=-0.4 mA | | $V_{DD}$-0.4 | | | V | (3) |
| Output low voltage (1) | $V_{OL1}$ | $I_{OL}$= 0.4 mA | | | | 0.4 | V | (3) |
| Output high voltage(2) | $V_{OH2}$ | $I_{OH}$=-0.4 mA | | $V_{DD}$-0.4 | | | V | (4) |
| Output low voltage (2) | $V_{OL2}$ | $I_{OL}$= 0.4 mA | | | | 0.4 | V | (4) |
| Input leakage current | $I_{LI}$ | $V_I=V_{SS}$~$V_{DD}$ | | -10.0 | | 10.0 | μA | (5) |
| Output leakage current | $I_{LO}$ | $V_I=V_{SS}$~$V_{DD}$ | | -10.0 | | 10.0 | μA | (6) |
| LC driver output on resistance | $R_{ON}$ | \|ΔVon\| =0.5 V | $V_O$=30 V | | 0.7 | 1.0 | kΩ | (7) |
| | | | $V_O$=20 V | | 1.0 | 1.5 | | |
| Stand-by current | $I_{STB}$ | CK=0 V CSB=$V_{DD}$(1) | $V_{DD}$=3 V | | | 5.0 | μA | (8) |
| | | | $V_{DD}$=5 V | | | 10.0 | | |
| Consumed current(1) | $I_{DDM1}$ | Master mode (2) | $V_{DD}$=3 V | | | 50 | μA | (9) |
| | | | $V_{DD}$=5 V | | | 150 | | |
| Consumed current(2) | $I_{DDM2}$ | Master mode (3) | $V_{DD}$=3 V | | | 800 | μA | |
| | | | $V_{DD}$=5 V | | | 2500 | | |
| Consumed current(3) | $I_{DDS1}$ | Slave mode (4) | $V_{DD}$=3 V | | | 30 | μA | |
| | | | $V_{DD}$=5 V | | | 100 | | |
| Consumed current(4) | $I_{DDS2}$ | Slave mode (5) | $V_{DD}$=3 V | | | 800 | μA | (9) |
| | | | $V_{DD}$=5 V | | | 2500 | | |

| Parameter | Symbol | Test conditions | | MIN. | TYP. | MAX. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Consumed current(5) | $I_{OM2}$ | Master mode (6) | $V_{DD}$=3 V | | | 50 | μA | (10) |
| | | | $V_{DD}$=5 V | | | 50 | | |

Note: Forward current direction is defined as one from outside into LSI.

*Applicable pins*

(1) RESB,M80/68,M/SB,FLM,M,LP,CK
(2) DB7～DB0,RS,CSB,RDB(E),WRB(R/WB)
(3) LP,FLM,M
(4) DB7～DB0
(5) RESB,M80/68,M/SB,FLM,M,LP,CK,RS,CSB,RDB(E),WRB(R/WB)
(6) When DB7~DB0 in high impedance state
(7) SEG1~SEG80
(8) $V_{SS}$
(9) $V_{DD}$
(10) $V_{OL}$,$V_{OR}$

Conditions

(1) Standby current
Current to $V_{DD}$ pin in master mode, with no CK input, no chip select (CSB=$V_{DD}$)

(2) Consumed current(1)
Current to $V_{DD}$ pin in master mode, with CK input(1 MHz at $V_{DD}$=5.0 V, 500 kHz at $V_{DD}$=3.0 V, 50 % duty), no chip select(CSB=$V_{DD}$), During access ,no load

(3) Consumed current(2)
Current to $V_{DD}$ pin in master mode, with CK input(1 MHz at $V_{DD}$=5.0 V , 500 kHz at $V_{DD}$=3.0 V , 50% duty), writing alternating data(reverse/non-reverse) into the display RAM at 1 μs(at $V_{DD}$=5.0 V) or 2 μs(at $V_{DD}$=3.0 V) cycle time
During access ,no load.

(4) Consumed current(3)
Current to $V_{DD}$ pin in slave mode, with no chip select(CSB=$V_{DD}$) and under the following conditions:

| $V_{DD}$=5.0 V | $V_{DD}$=3.0 V |
|---|---|
| • CK input(1 MHz,50 % duty) | • CK input(500 kHz,50 % duty) |
| • LP input(7.8 kHz,50 % duty) | • LP input(3.9 kHz,50 % duty) |
| • FLM input(61 Hz) | • FLM input(30.5 Hz) |
| • M input(30.5 Hz) | • M input(15.25 Hz) |

During access (Input timing as specified in AC characteristics) ,no load.

(5) Consumed current(4)
Current to $V_{DD}$ pin in slave mode, when writing alternating data (reverse/non-reverse) into the display RAM at 1 μs (at $V_{DD}$=5.0 V) or 2 μs (at $V_{DD}$=3.0 V) cycle time under the following conditions:

| $V_{DD}$=5.0 V | $V_{DD}$=3.0 V |
|---|---|
| • CK input(1 MHz,50 % duty) | • CK input(500 kHz,50 % duty) |
| • LP input(7.8 kHz,50 % duty) | • LP input(3.9 kHz,50 % duty) |
| • FLM input(61 Hz) | • FLM input(30.5 Hz) |
| • M input(30.5 Hz) | • M input(15.25 Hz) |

During access (Input timing as specified in AC characteristics), no load.

(6) Consumed current(5)
Current at $V_{OR}$,$V_{OL}$ in under conditions(3)
During access ,no load.

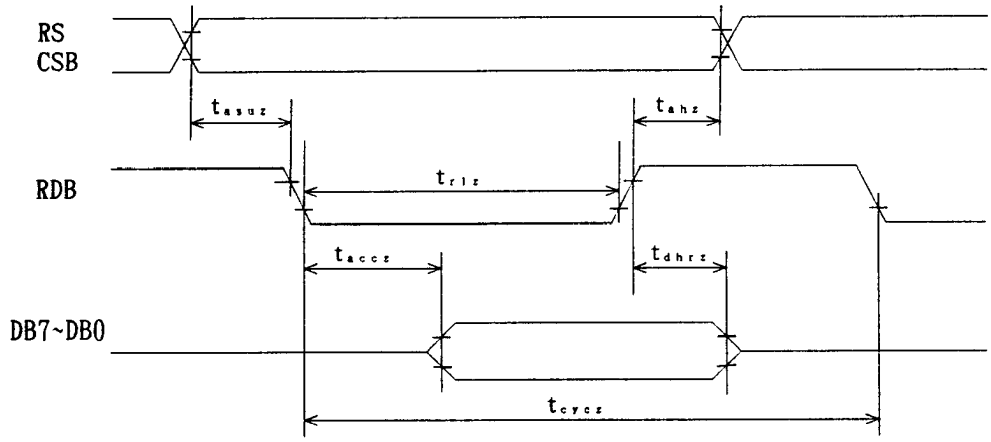
11-2. AC characteristics

11-2-1. System bus read/write timing(80 family) (Output Load 70 pF)

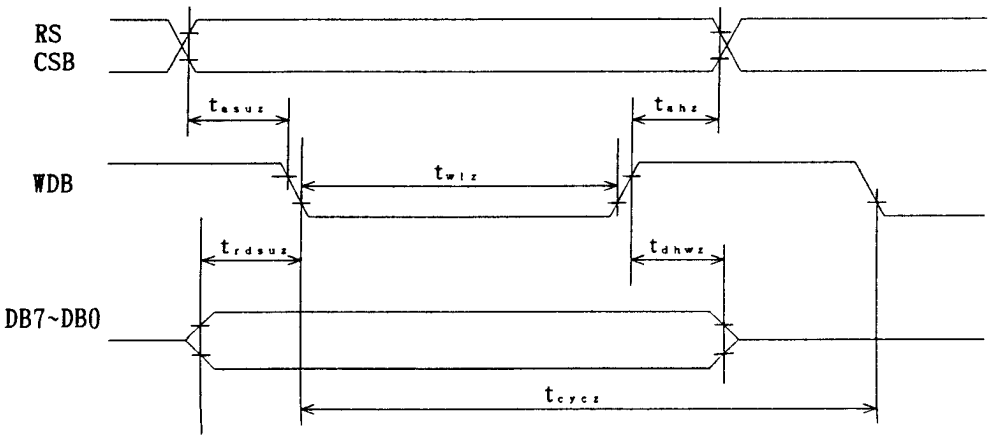
$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

| Parameter | Symbol | $V_{DD}$=2.5~4.5 V | | $V_{DD}$=4.5~5.5 V | | Unit | Pin |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| Address hold time | $t_{ahz}$ | 40 | | 20 | | ns | RS |
| Address set-up time | $t_{asuz}$ | 300 | | 150 | | ns | CSB |
| System cycle time | $t_{cycz}$ | 1300 | | 1000 | | ns | WRB |
| Read/write pulse width | $t_{rlz}$, $t_{wlz}$ | 700 | | 350 | | ns | RDB |
| Data set-up time | $t_{rdsuz}$ | -30 | | -15 | | ns | DB0 |
| Write data hold time | $t_{dhwz}$ | 40 | | 20 | | ns | ∫ |
| Read data access time | $t_{accz}$ | | 700 | | 350 | ns | |
| Read data hold time | $t_{dhrz}$ | 20 | | 10 | | ns | DB7 |
| Input signal rising falling time | $t_r$, $t_f$ | | 30 | | 15 | ns | All pins |

〈Read cycle〉




〈Write cycle〉

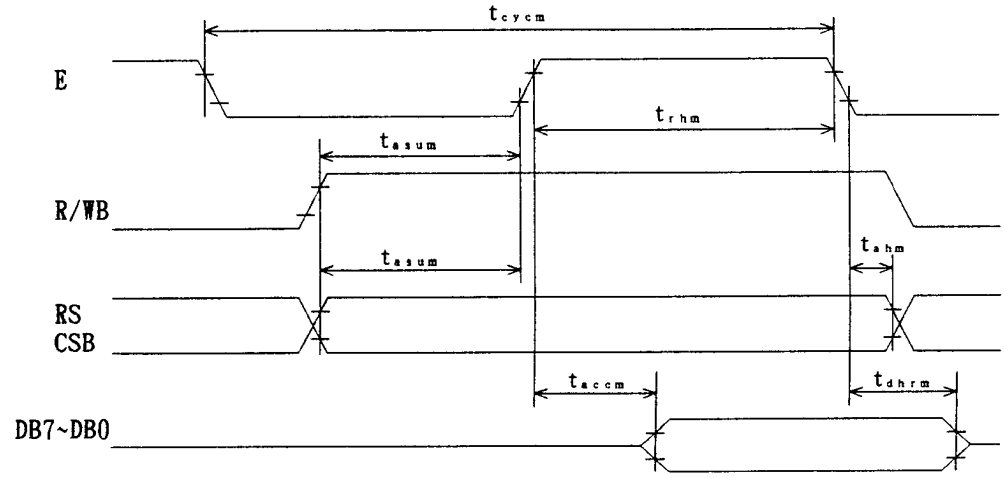


11-2-2. System bus read/write timing(68 family) (Output Load 70 pF)

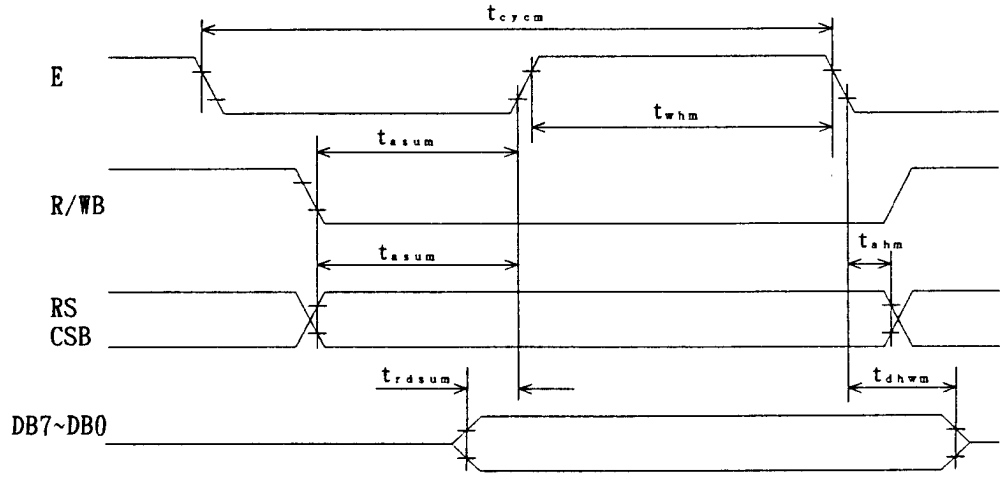
$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

| Parameter | | Symbol | $V_{DD}$=2.5~4.5 V MIN. | MAX. | $V_{DD}$=4.5~5.5 V MIN. | MAX. | Unit | Pin |
|---|---|---|---|---|---|---|---|---|
| System cycle time | | $t_{cycm}$ | 1300 | | 1000 | | ns | E |
| Address set-up time | | $t_{asum}$ | 300 | | 150 | | ns | RS,CSB |
| Address hold time | | $t_{ahm}$ | 40 | | 20 | | ns | R/WB |
| Data set-up time | | $t_{rdsum}$ | -30 | | -15 | | ns | DB0 |
| Write data hold time | | $t_{dhwm}$ | 40 | | 20 | | ns | ⟆ |
| Read data access time | | $t_{accm}$ | | 700 | | 350 | ns | |
| Read data hold time | | $t_{dhrm}$ | 20 | | 10 | | ns | DB7 |
| Enable pulse width | Read pulse | $t_{rhm}$ | 700 | | 350 | | ns | E |
| | Write pulse | $t_{whm}$ | 700 | | 350 | | ns | |
| Input signal rising,falling time | | $t_r$, $t_f$ | | 30 | | 15 | ns | All pins |

〈Read cycle〉



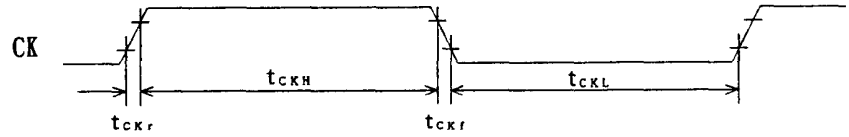

〈Write cycle〉



11-2-3. Master clock input timing

$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

| Parameter | Symbol | $V_{DD}$=2.5~4.5 V | | $V_{DD}$=4.5~5.5 V | | Unit | Pin |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| CK low level width | $t_{CKL}$ | 300 | | 200 | | ns | CK |
| CK high level width | $t_{CKH}$ | 300 | | 200 | | ns | |
| CK rising and falling time | $t_{ckr}$, $t_{ckf}$ | | 40 | | 20 | ns | |

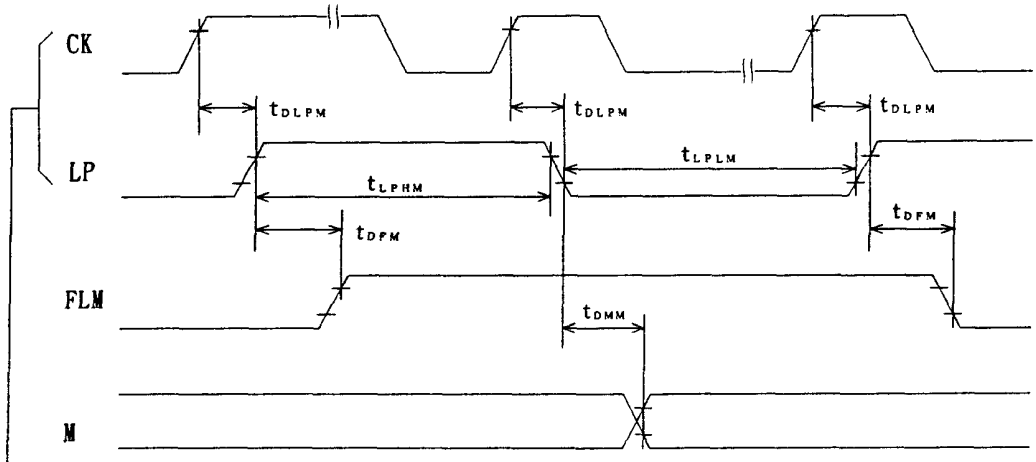



11-2-4. Display control timing

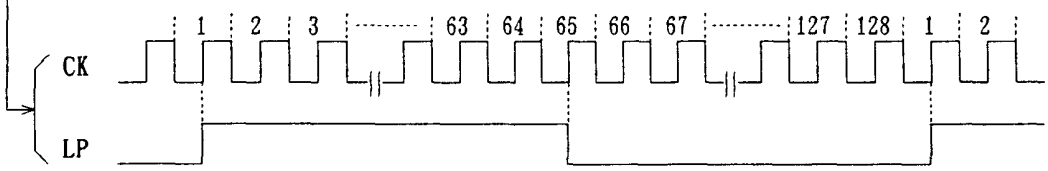
(a) Output timing in master mode (Output Load 70 pF)

$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

| Parameter | Symbol | $V_{DD}$=2.5~4.5 V | | $V_{DD}$=4.5~5.5 V | | Unit | Pin |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| CK fall to LP delay time | $t_{DLPM}$ | 10 | 1000 | 10 | 500 | ns | LP |
| LP low level width | $t_{LPLM}$ | 38.4 | | 25.6 | | μs | |
| LP high level width | $t_{LPHM}$ | 38.4 | | 25.6 | | μs | |
| LP rise to FLM delay time | $t_{DFM}$ | 10 | 1000 | 10 | 500 | ns | FLM |
| LP rise to M delay time | $t_{DMM}$ | 10 | 1000 | 10 | 500 | ns | M |



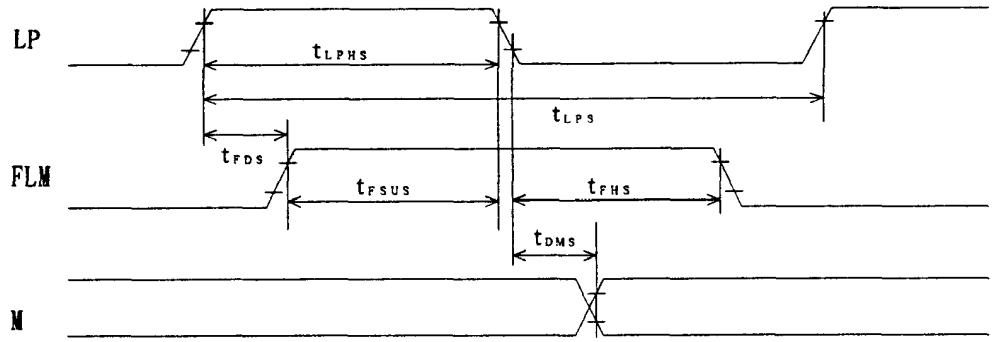

〈Timing of CK and LP in the master mode are as shown below〉



(a) Input timing in the slave mode

$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

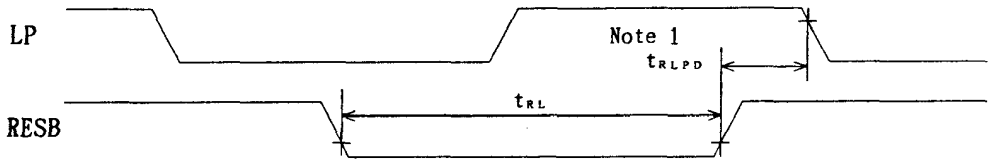
| Parameter | Symbol | $V_{DD}=2.5$~4.5 V | | $V_{DD}=4.5$~5.5 V | | Unit | Pin |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| LP period | $t_{LPS}$ | 76.8 | | 51.2 | | µs | LP |
| LP high level width | $t_{LPHS}$ | 38.4 | | 25.6 | | µs | |
| FLM set-up time | $t_{FSUS}$ | 30 | | 20 | | µs | FLM |
| FLM hold time | $t_{FHS}$ | 30 | | 20 | | µs | |
| LP rise to FLM delay time | $t_{FDS}$ | 100 | | 100 | | ns | |




11-2-5. Reset input timing

$V_{SS}=V_5=0$ V, $V_0=10$ V~30 V, Ta=-20 ℃~+85 ℃

| Parameter | Symbol | $V_{DD}=2.5$~4.5 V | | $V_{DD}=4.5$~5.5 V | | Unit | Pin |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| RESB level pulse width | $t_{RL}$ | 1.2 | | 1.2 | | µs | RESB |
| RESB off time(Note 1) | $t_{RLPD}$ | 100 | | 100 | | ns | |




Note 1: When the same reset signal is applied to both RESB pin of the LH1554P and $\overline{\text{DISPOFF}}$ pin of the common driver LH1531M.
If a separate signal is applied to $\overline{\text{DISPOFF}}$ pin of the LH1531M or if the pin is pulled up to high level, this requirement is not applied.

12. LC driver output timing
Display timing in the non-inverting mode

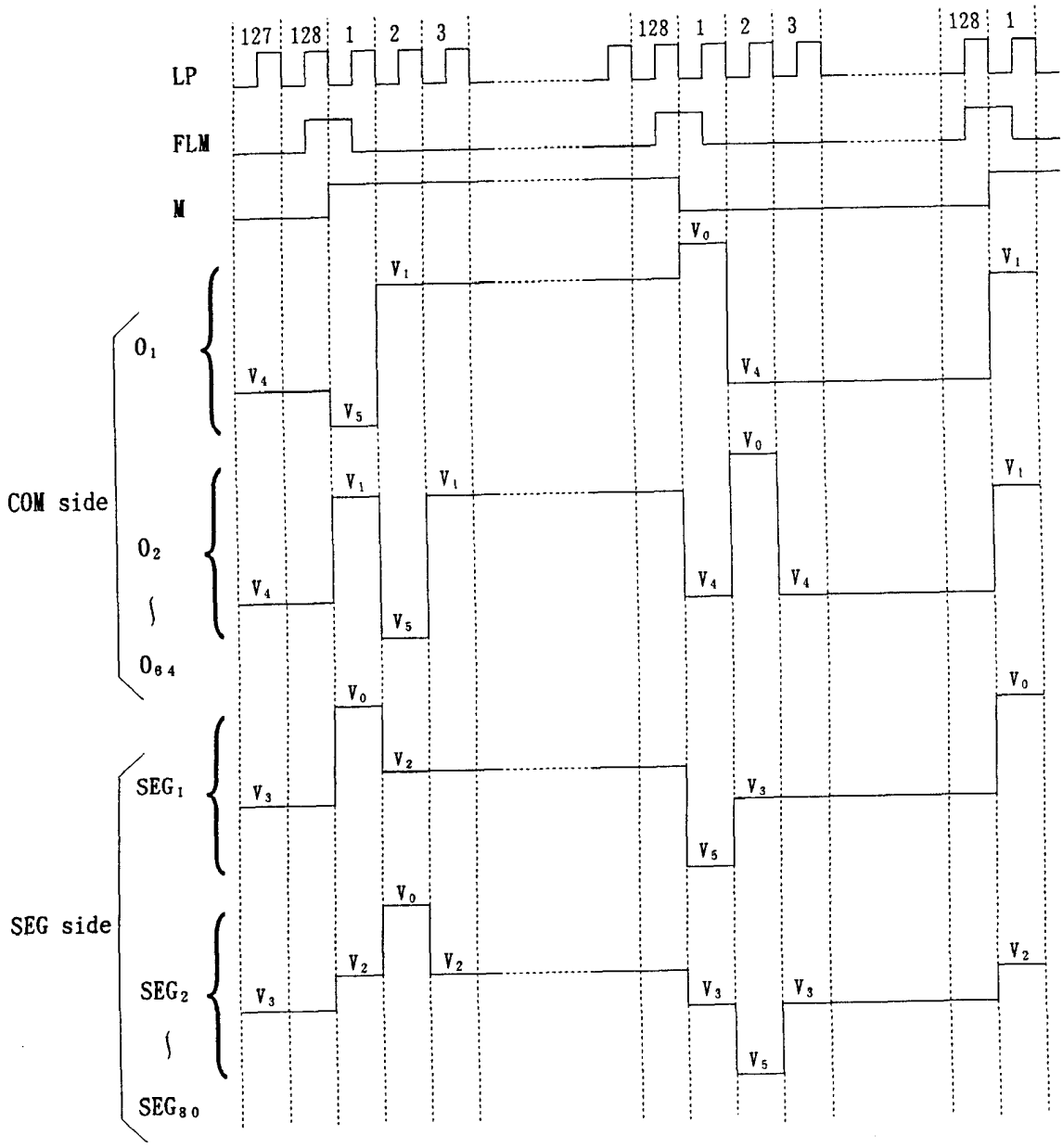
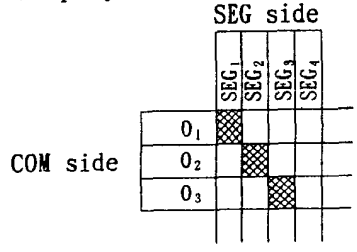


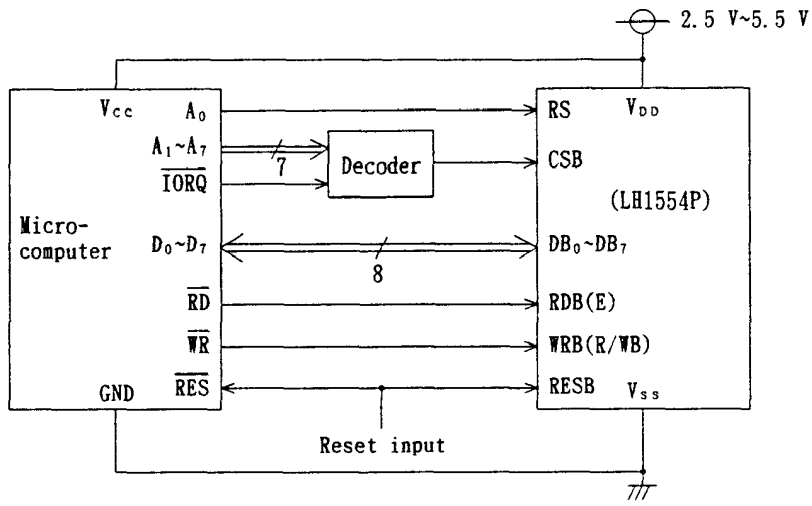

Fig.11. Example of display wave form



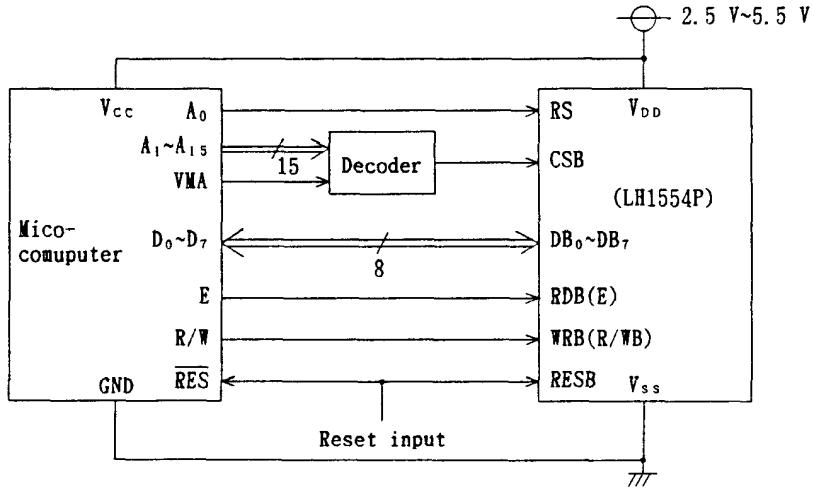
13. Typical applications(reference only)

13-1. Connection to microcomputer

(a) 80 family microcomputer



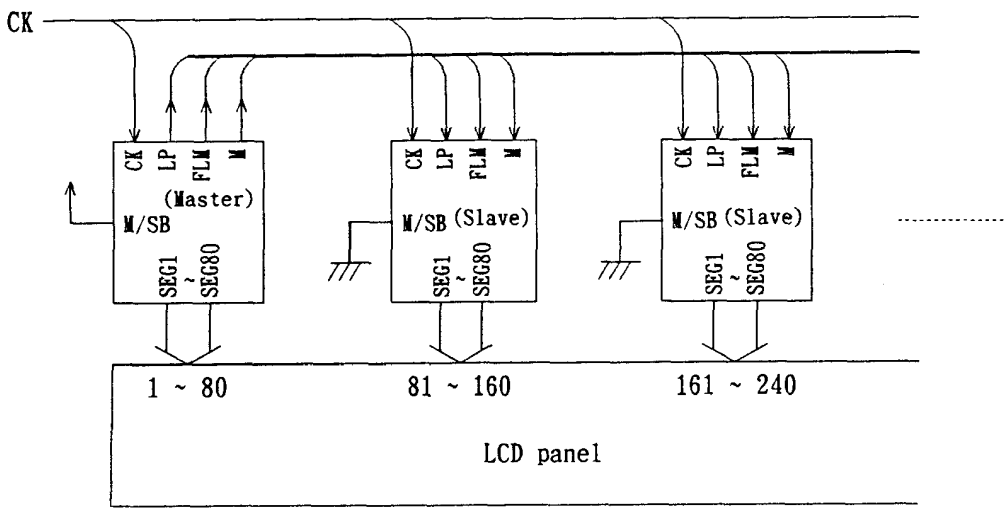

(b) 68 family microcomputer



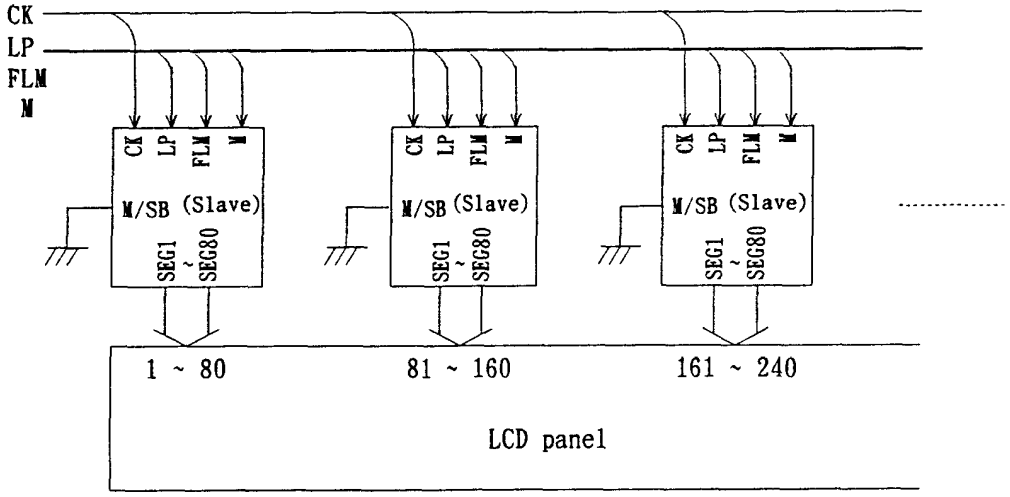

When connecting the microcomputer to two or more LH1554P's, adjust the decoding conditions of the address signal to be applied to each CSB pin.

13-2. Connection of display signals when two or more LH1554P's are used

(a) Master→slave→slave→ ·····

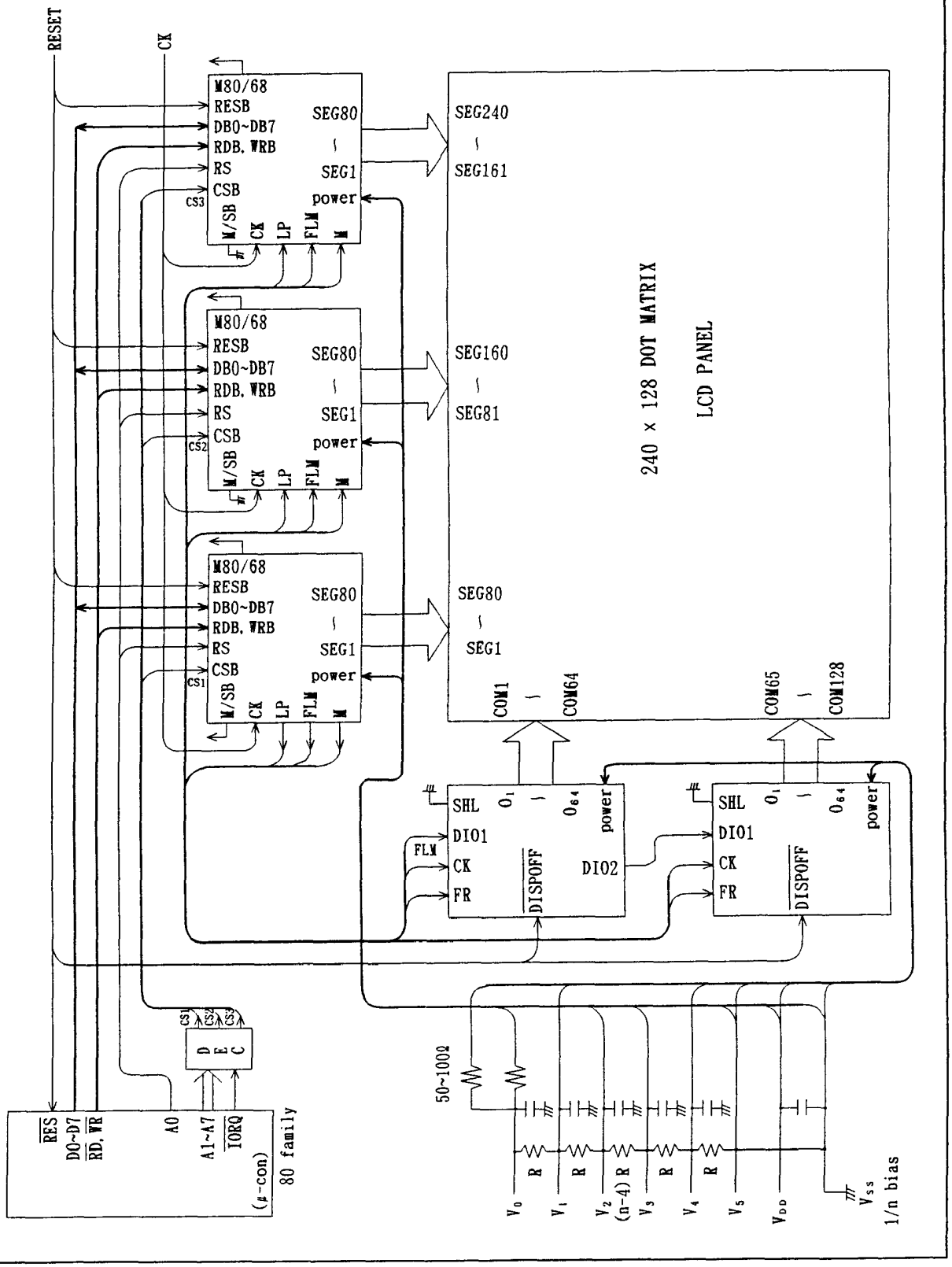



(b) Slave→slave→slave→ ·····



13-3. Typical system configuration(segment side: LH1554P; common side: LH1531M)

* With this application, REF register= "0"



## 14 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA1143

2. Markings

2－1. Marking contents

(1) Product name : LH1554P

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××

- YY → Denotes the production year. (Lower two digits of the year.)
- WW → Denotes the production week. (01, 02, 03, ・・・・・52, 53)
- ××× → Denotes the production ref.code (1~3)

Indicates the product was manufactured in the WWth week of 19YY.

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA1143

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

| Material Name | Material Specificaiton | Purpose |
|---|---|---|
| Tray | Conductive plastic (50devices/tray) | Fixing of device |
| Upper cover tray | Conductive plastic (1tray/case) | Fixing of device |
| Laminated aluminum bag | Aluminum polyethylene (1bag/case) | Drying of device |
| Desiccant | Silica gel | Drying of device |
| P P band | Polypropylene (3pcs/case) | Fixing of tray |
| Inner case | Card board (500devices/case) | Packaging of device |
| Label | Paper | Indicates part number, quantity and date of manufacture |
| Outer case | Card board | Outer packing of tray |

(Devices shall be placed into a tray in the same direction.)

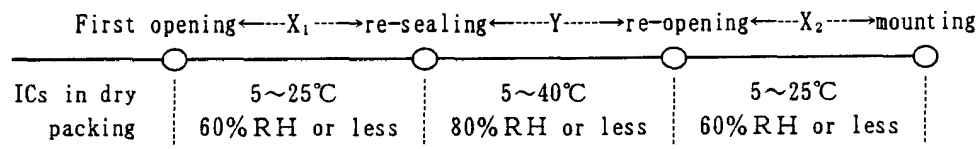
3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).




$X_1 + X_2$ : within 4 days
Y : within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃.
Heat resistance tray is used for shipping tray.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

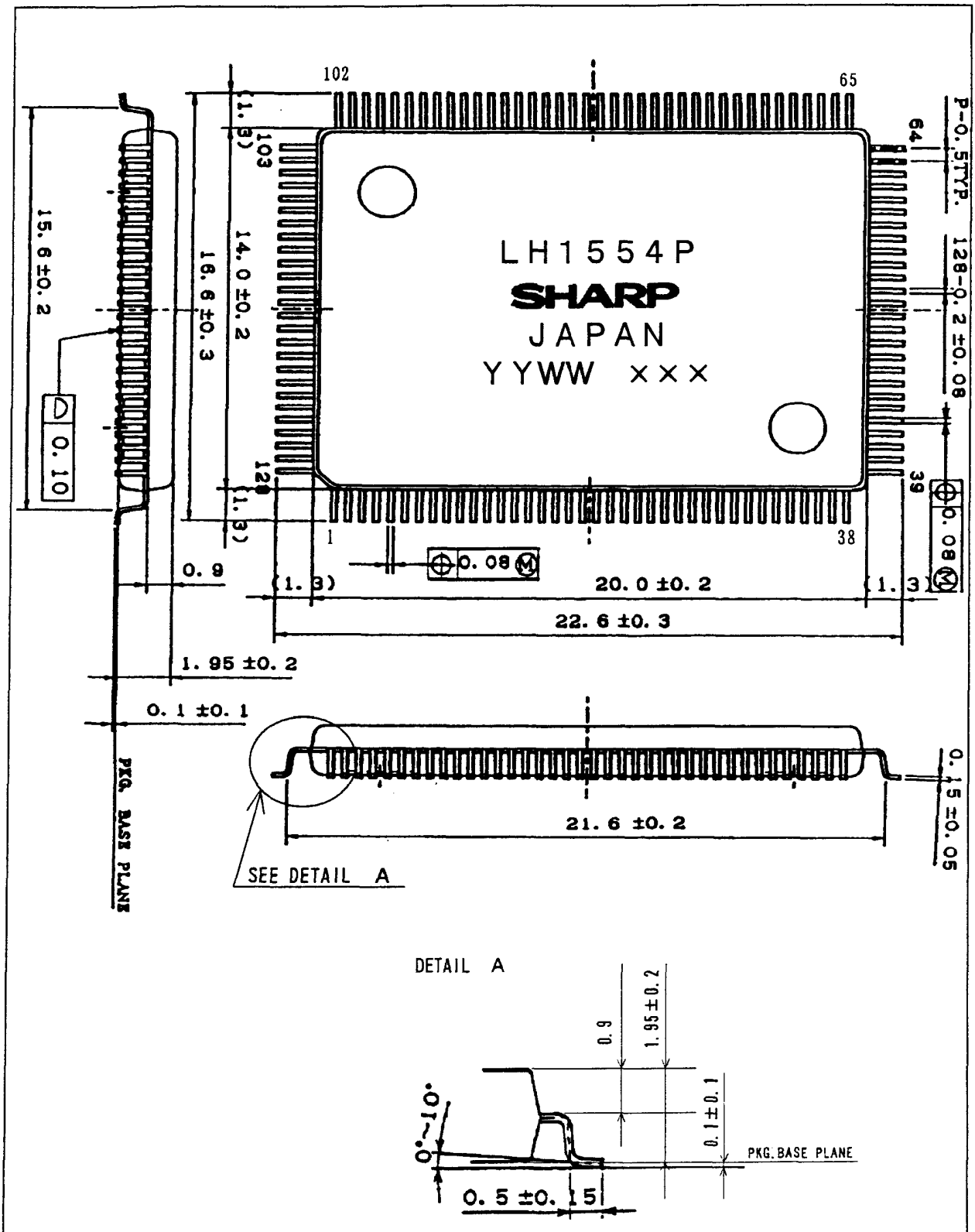
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

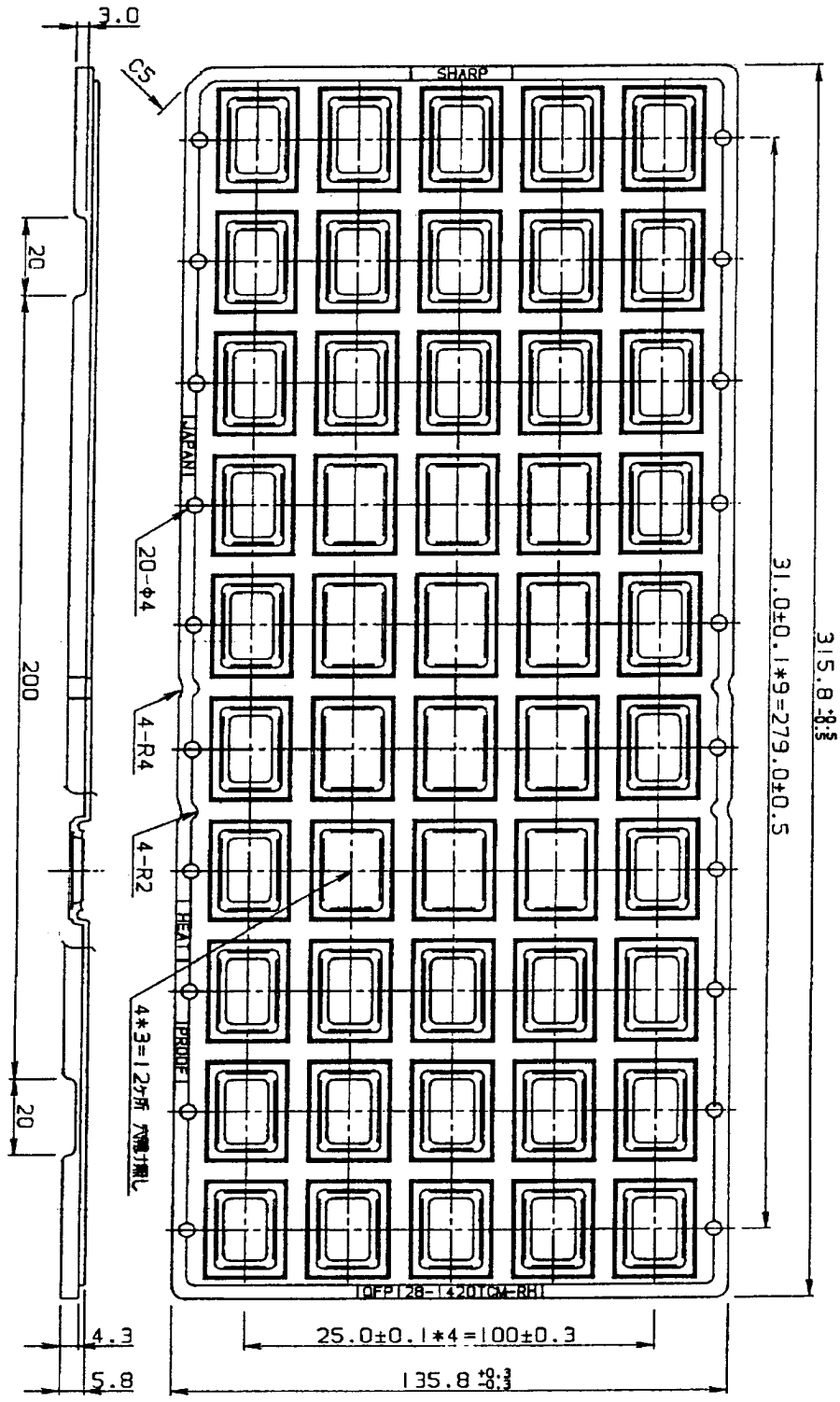
| Mounting Method | Temperature and Duration | Measurement Point |
|---|---|---|
| Reflow soldering (air) | Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second | IC surface |
| Vapor phase solderring | 215℃ or less, duration less than 40 seconds above 200℃ | Steam |
| Manual soldering (soldering iron) | 260℃ or less, duration less than 10 seconds | IC outer lead surface |

5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃




| | | | | |
|---|---|---|---|---|
| 名称 NAME | QFP128-P-1420 | リード仕上 LEAD FINISH | TIN-LEAD PLATING | 備考 NOTE プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin. |
| DRAWING NO. | AA1143 | 単位 UNIT | mm | |




| 名称 NAME | QFP128−1420TCM−RH | 備考 NOTE |
|---|---|---|
| DRAWING NO. | CV763 | 単位 UNIT mm |