PCI-WD

PCI Multi-function
Watchdog and System Monitor Card

User Manual

PCI-WD

User Manual

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Introduction

The PCI-WD is a PCI-compatible half-card which provides system monitoring of system power supplies, fan operation, system temperature and Processor activity and generates alarm functions in the event of a system malfunction.

The heart of the system monitoring is performed by the National Semiconductor LM78 IC. This highly integrated devices performs the supply, fan and temperature monitoring circuits as well interrupt generation.

Four PCI power rails (+3.3V, +5V, +12V and -12V) can be monitored for over and under voltage excursions. In the event of the rails drifting out specification the system is notified.

Three fan speed counter circuits provide a warning to the system that fans are operating out of specification. This function requires the use of Tacho pulse fans which provide output pulses the frequency of which is proportional to the fan speed. If the fan speed drops below predefined limits, the system is notified.

A programmable watchdog timer facilitates monitoring of application software execution. This is achieved by the use of a timer which notifies the system on the event of a time out. The user application must refresh this timer before the count has expired indicating successful code execution. The timer is software selectable between 1 and 255 seconds.

The PCI-WD has an onboard temperature monitor to notify the system that temperature within the PC enclosure has risen past a prescribed level.
External events can be monitored through an isolated digital input. The input voltage levels can range from -50V to + 50V with an input current level of 1mA. In the event of a state of change on this input the system is notified.

In response to any of the above monitoring circuits detecting an error or change in condition, the system can generate a number of responses including activating a relay, activating an on board audible alarm, illuminating an LED or resetting the system. Each of the above responses can be enabled and disabled under software control.

All Input / Output lines are available on a 15 Way rugged screw terminal connector.
One PCI interrupt line may be selectively driven by a number of interrupt sources on the board, the interrupting source being readily identified by the board.
The PCI-WD is intended to be installed with the minimum of user interaction. The board is configured by the system BIOS and by the application drivers and no on-board links are required to select functionality.

About the Manual

This manual is organised into four chapters. Each chapter covers a different aspect of using the PCI-WD. In order to get the best results from the product, the user is urged to read all chapters, paying particular note to Chapter 1 which deals with the initial installation of the card.

Chapter 1 Explains how to install the card in your computer.

Chapter 2 Details the connections to and from the card.

Chapter 3 Gives details of the card's address mapping and internal register details allowing the user to write custom software to control the card.

Chapter 4 Presents the card's technical specification. Use this section to determine the card's suitability for a particular application

This manual describes the complete hardware functionality of the PCI-WD board. All the functions described may not necessarily be supported by the current release of the Windows NT driver and DLL set.

CHAPTER 1

INSTALLING THE PCI-WD

The card is installed by removing the cover of the host computer and inserting the card into a free PCI slot. The rear panel of the card should then be secured to the rear panel of the host computer with the screw supplied with the computer.

When the computer is switched on, the BIOS will detect the presence of the card and will allocate it with a set of base addresses and an interrupt. These parameters may then be used by the application software to access the card. If the card is to be directly accessed by a user's DOS application, it will be necessary for the application to determine where the BIOS has located the card.

To this end a software function has been provided. Refer to the "Readme.txt" file on the supplied disk for details.

CHAPTER 2

CONNECTION DETAILS

External Connector P1

The following table refers to the 15 way two-part screw terminal connector (P1) at the rear of the card.

PIN	USAGE
1	Relay Normally closed contact
2	Relay Common contact
3	Relay Normally open contact
4	Opto input (+ve)
5	Opto input (-ve)
6	Vcc (fused at 1A)
7	IIC interface (not yet implemented)
8	IIC interface (not yet implemented)
9	IIC interface (not yet implemented)
10	Digital Ground
11	External +ve voltage monitor 1 (not yet implemented)
12	External +ve voltage monitor 2 (not yet implemented)
13	External -ve voltage monitor 1 (not yet implemented)
14	External open collector output
15	Analogue ground (gnd reference for external voltage monitor inputs)

Fan Connections (P3, P5 & P6)

The fan monitoring circuits connect to the fans by standard 0.1” pitch latched two way Molex connectors. Pin 1 of the connectors must be connected to the open collector output of the fan and pin 2 referenced to the fan ground connection which also be the system 0 volt connection. The polarity of these connections is identified on the PCI-WD PCB silk-screen.

Reset Output Connection (P7)

This output is used to force a system reset in the same manor as the PC front panel reset switch. The connector (P7) should be wired in parallel across the front panel reset switch and/or the motherboard reset pin header. The connector is a standard 0.1 pitch latched 2 way Molex connector. The polarity of this connector is identified on the PCI-WD PCB silk-screen.

Suitable Interface Signal Types

Digital Input

The opto isolated digital input has two connections across which a voltage applied. This voltage may be between -50 volts and +50 volts. Any voltage between -50 volts and +2.4 volts will be interpreted as a logic zero, and any voltage between +4.4 volts and +50 volts will be interpreted as logic 1. The current on this input signal is a constant 1mA, when the input voltage conforms to the logic 1 requirements, and 5uA (max) for a logic 0.

A fused (1 amp) +5 volt supply and ground reference signal is available on the screw terminal connector to allow this input to be configured in voltage free switching input installations. When configured in this way there is no electrical isolation between the input circuit and the host PC.

Fan Pulse Inputs

The use of the fan pulse counters requires the use of special fans who provide an open collector tacho output. The connections to the board are made via three two way Molex connectors P3, P5 and P6. The first and second fan counter circuits are programmable to cover a range of speeds from 1100 to 8800rpm. The third fan input is fixed at 4400 rpm.

External Supply Monitor Inputs

The External supply inputs are not currently supported and should therefore remain unconnected.

Digital Output

The digital output is a non-isolated open collector output capable of sinking 500mA. The maximum switching voltage is +50V. When an inductive load is being driven by this output, it is essential that a reverse biased diode is connected across the load to catch the back EMFs generated when the output is de-energised and the load current falls to zero.

Relay Output

The relay output contacts provide voltage free signalling to indicate a change in system status. The relay contacts can be configured for Normally Open, Normally Closed or Changeover operation. The contacts are rated at 1 Amp 24 Volt dc and 0.5 Amp 125 Volt ac. Care should be exercised with any voltage in excess of 50 Volts

Reset Output

The reset connector (P7) requires the user to wire a parallel connection from the PCI-WD card (P7) to the reset header of the PC motherboard and the reset switch. This cabling arrangement allows the PC reset switch to be used independently of the PCI-WD reset function.

CHAPTER 3

PROGRAMMING DETAILS

This chapter provides details of the cards internal registers.

Address Map

The address map for the PCI-WD occupies a 12-byte block of addresses.

All the following addresses are relative to the addresses contained in PCI Base Address Registers 2, (BAR2) as indicated. The BAR2 is located at address offset 18h in the PCI configuration space:-

ADDRESS (hex)	FUNCTION	ACCESS WIDTH	READ/ WRITE
Base2 + 5	LM78 Internal Address Register	byte	W
Base2 + 6	LM78 Internal Data Register	byte	R/W
Base2 + 8	Watchdog Timer Count Load Register	byte	W
Base2 + 8	Watchdog Timer Reset port	byte	R
Base2 + 9	PCI-WD IRQ and WD timer Enable/Disable Register	byte	W
Base2 + 9	PCI-WD Status Register	byte	R
Base2 + a	PCI WD Output Mask Register	byte	W
Base2 + b	PCI-WD Output Control Register	byte	W

In order to access the internal registers of the LM78, the user must first write the address of the register to port Base2 + 5h. The data is then written to or read from port Base2 + 6h. A full description of the LM78 registers is given in the appendices.

The Base2 + 8+ registers have the following bit assignments.

Base2 + 8 : The value written to this register determines the watchdog time-out period in multiples of 2 sec. Valid entries are 1 to 127(2 to 254 seconds). When this address is read, a refresh of the watchdog timer is generated. The value read from this address is extraneous.

Base2 + 9 : Writing to this register enables the watchdog timers and the various interrupt sources. Reading this register returns the enable register status and the board IRQ status. The bit assignments are tabulated below:

Interrupt Enable/ Status Register (Base 2 +9 $_h$) Write		
Bit no.	**Function**	
b7	Not used	
b6	Not used	
b5	Not used	
b4	Not used	
b3	Watchdog Timer Interrupt enable	1 = Enable, 0 = Disable
b2	LM78 Interrupt enable	1 = Enable, 0 = Disable
b1	External input interrupt enable	1 = Enable, 0 = Disable
b0	Watchdog Timer enable	1 = Enable, 0 = Disable

Interrupt Enable Register (Base 2 + 9 $_h$) Read		
Bit no.	**Function**	
b7	Watchdog timer IRQ status	1 = triggered
b6	LM78 IRQ status	1 = triggered
b5	External input IRQ status	1 = triggered
b4	External opto input value	1: ip =>4.4V, 0: ip<2.4V
b3	Watchdog Timer Interrupt enable status	
b2	LM78 Interrupt enable status	
b1	External input interrupt enable status	
b0	Watchdog Timer enable status	

Base2 + A : This register allows the PCI-WD to provide a number of different output actions in response to a fault condition. These outputs are; a system reset, a relay contact change over, a buzzer sounding, an LED illuminating and an open collector transistor output being driven. By setting the appropriate bits of this register any combination of the above outputs can be activated on the occurrence of a fault condition. This register is write only.

Output Response Register (Base 2 + A $_h$) Write		
Bit no.	**Function**	
b7	Not used	
b6	Not used	
b5	Not used	
b4	Activate open collector	1 = Enable, 0 = Disable
b3	Illuminate LED	1 = Enable, 0 = Disable
b2	Alarm Buzzer	1 = Enable, 0 = Disable
b1	Relay change over	1 = Enable, 0 = Disable
b0	System reset	1 = Enable, 0 = Disable

Base2 + B : This register permits direct access to the output functions of the PCI-WD card. It may be used instead of or in conjunction with the Output Response Register. With this register the relay, LED, reset, buzzer etc, functions can be accessed directly through an IO write. This register is write only.

Output Response Register (Base 2 + B $_h$) Write		
Bit no.	**Function**	
b7	Not used	
b6	Not used	
b5	Not used	
b4	Activate open collector	1 = Enable, 0 = Disable
b3	Illuminate LED	1 = Enable, 0 = Disable
b2	Alarm Buzzer	1 = Enable, 0 = Disable
b1	Relay change over	1 = Enable, 0 = Disable
b0	System reset	1 = Enable, 0 = Disable

Supply Monitors

The supply monitor circuits can be programmed to detect over and undervoltage on the supply rails. One negative and three positive rails are monitored as standard. The LM78 supports an 8 bit ADC with a resolution of 16mV over an input range of 0 - 4.08 volts. For this reason the +5 Volt and the ±12 Volt supplies are attenuated. Consequently the LSB weighting for each supply will differ depending on the attenuation. The following table list each of the supply attenuation factors and the corresponding LSB value.

Supply Voltage	Voltage to ADC input	LSB Weighting
+3.3 Volts	3.3 Volts	16mV/bit
5 Volts	2.98 Volts	26.8mV/bit
+12 Volts	3.00 Volts	64mV/bit
-12 Volts	3.00 Volts	64mV/bit

The converted results can be read from the corresponding Value RAM locations within the LM78. Any rail suffering an out of limit excursion can be read through Interrupt status registers 1 and 2. The under and over voltage limits can be programmed into the corresponding Value RAM locations.

Fan Monitors

The fan monitor circuits can be enabled and disabled under software control to accommodate a variety of system configurations using the LM78 address registers 45h & 46h. Each fan monitor has software selectable count limits which can be accessed through Value RAM locations 3Bh & 3Ch & 3Dh. In addition fan monitors 1 and 2 can be configured for different nominal fan speeds of 8800, 4400, 2200 and 1100 rpm through LM78 register address 47h. Fan monitor 3 is fixed for a nominal speed of 4400 rpm.

Temperature Monitor

The PCI-WD provides on board temperature monitoring to indicate when an excessive temperature rise has occurred. The temperature data is represented by an 8-bit, two’s complement word with an LSB of 1°C The upper temperature limit and the temperature hysteresis can be programmed by the user through the LM78 Value RAM locations 39h & 3Ah.

Watchdog Timer

The watchdog timer comprises of an 8-bit load counter with a time base of 2 Hz giving a watchdog refresh period of 1 to 255 seconds. The watchdog refresh period is set through register Base2 + 8h. The watchdog timer can be enabled/ disabled through bit 0 of register Base2 + 9h.

Isolated External Input

The status of the external input can be read directly from port Base2 + 9 bit 4. In addition a change of state on this input can generate a interrupt to the system. This interrupt operation can enabled/disabled through port Base2+ 9 bit 1.

Interrupt Selection

A total of 10 sources of interrupt are available from the supply, fans, temperature, external input and watchdog timer monitors. These interrupts are divided between the LM78 functions (power fan and temperature monitors) and the non LM78 functions (watchdog timer and External input).

The LM78 can generate interrupts on the occurrence of an out of limit condition on one of more of the enabled LM78 monitor circuits. The LM78 produces a single interrupt signal which is in turn combined on board with the non-LM78 monitor circuits to produce a single interrupt signal for the PCI-WD. The interrupt status registers are located at LM78 register addresses 41h and 42H. A full description of these registers and their bit assignments can be found in the appendices.

The non-LM78 function interrupts are accessed at Base2 + 9. The bit assignments for these interrupts can be found in the previous section. Given the combined gating of the various interrupt sources, the source of the interrupt must first be determined by reading the Interrupt status register at address Base3 + 1h. This determines if the interrupt was generated by the LM78, the watchdog timer or the external input. If it was the LM78 its Interrupt registers must then be read. Having serviced an interrupt, the source should be cleared by momentarily clearing the relevant bit in the interrupt enable register (Base 2 + 9).

The use of interrupts is not essential but greatly enhances the functionality of the card. When the card is configured to run without interrupts i.e. in polled mode, the polling interval between successive polls must be greater than 1.5 seconds to ensure a complete system monitor scan and update of the data ram area of the LM78.

CHAPTER 4

TECHNICAL SPECIFICATIONS

Supply Monitors

Resolution:	8 bit Delta Sigma ADC
Accuracy	±1% / volts
LSB Weighting:	
3.3 Volt rail	16mV/ bit
5 Volt rail	26.8mV/bit
±12 Volt rail	64mV/bit

Relay Output

Contact rating:	1A 24V DC, 120V 0.5A AC (non inductive)
Maximum current:	2A
Maximum Switched Voltage:	125 Volts
Maximum Switched Power:	24W/ 60VA
Minimum contact load:	1mA, 1Volt

Digital Input

Maximum Input Voltage:	±50 Volts DC or AC peak
Input Current:	1mA ± 200µA for Vth< Vin< 50V DC +5µA (max) for -50V DC < Vin < Vth

Open Collector Output:

Maximum Drive Current:	500mA (Logic Low) Vout = 0.4 Volts (non inductive)
Maximum off state voltage	50 Volts DC
Maximum output Dissipation	750mW

Fan inputs:

Maximum Input voltage:	+5Volt from totem pole source +12Volt open collector source
Fan 1 & 2 nominal input:	Divisor = 1, count =153, RPM = 8800 Divisor = 2, count =153, RPM = 4400 Divisor = 3, count =153, RPM = 2200 Divisor = 4, count =153 RPM = 1100
Fan 3 nominal input:	Count = 153, RPM = 4400

Temperature Monitor

Range:	-10°C < Ta< +100°C
Accuracy:	±3°C
Resolution:	1°C

Interrupts

Interrupt Sources:	Register selectable to 12 sources, +3.3V, +5V, +12V, -12V, 3 fan circuits temperature monitor, external input and watchdog timer
Levels Supported:	One PCI INTn# interrupt
Address Overhead:	12 I/O addresses in 2 PCI address spaces

Power

Board Power Requirement:	+5 Volts, 1.8 W maximum +3.3Volts @ 1mA max +12 Volts @ 1mA max -12 Volts @ 1mA max

Physical

Signal Connections:	1 x 15 way two-part screw terminal connector
Dimensions:	124 (L) x 99 (H) board only 140 (L) x XX (H) x 22(W) including bracket

Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in our standard industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements of EN55022:1995 for a Class A product subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for an industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to boards. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple “pig-tail”. Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

- Cables which connect externally to boards at TTL levels should not exceed two metres in length.

Failure to observe these recommendations may invalidate the EMC compliance.

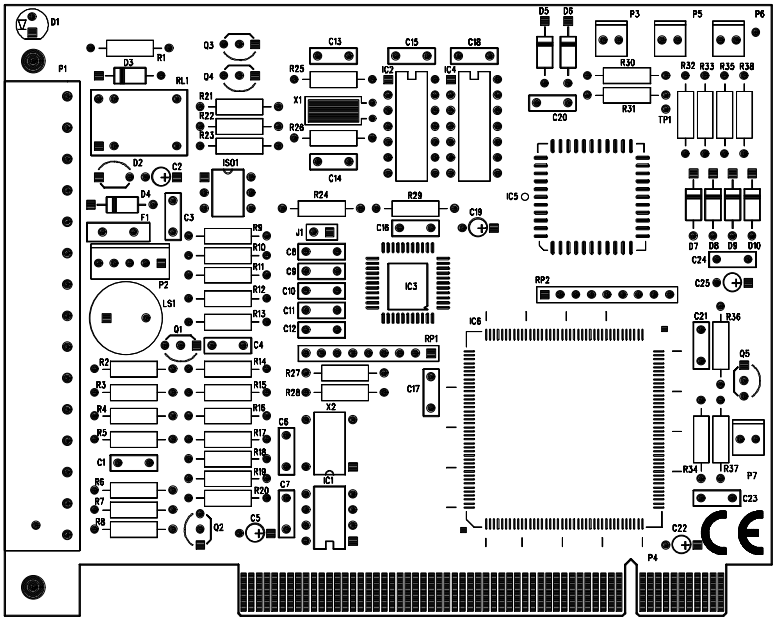
> Warning
> This is a Class A product. In a domestic environment this product may cause radio-interference in which case the user may be required to take adequate measures.

EMC Specification

A suitably compliant industrial PC fitted with this card meets the following specification:

Emissions	EN 55022:1995		
	Radiated	Class A	
	Conducted	Class A & B	
Immunity	EN 50082-2:1995 incorporating:		
	Electrostatic Discharge		EN 61000-4-2
	Radio Frequency Susceptibility		ENV50140
			ENV50204
	Fast Burst Transients		EN 61000-4-4

PCB LAYOUT DIAGRAM



LM78 REGISTERS AND RAM

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Address Register (Base2 + 5h)

Bit	Name	Read/ Write	Description
6-0	Address Pointer	Read/Write	Address RAM and Register
7	Busy	Read Only	1 = busy on bus transaction

Address Pointer Index

Register & RAM	Location (Hex)	power on value
Configuration Register	40h	08h
IRQ# status Register 1	41h	00h
IRQ# status Register 2	42h	00h
IRQ# Mask Register 1	45h	00h
IRQ# Mask Register 2	46h	40h
VID/Fan divisor	47h	5Fh
Chip Reset/ID register	49h	40h
Value RAM	20-3Fh	
Value RAM	60 7Fh	

Data Register (Base2 +6h)

Bit	Name	Read/Write	Description
7-0	Data	Read/Write	Data read/ written to RAM

Configuration Register -LM78 address 40h

Bit	Name	Read/Write	Description
0	Start	Read/Write	1= monitor, 0= standby
1	Not Used	Read/Write	
2	NMI/IRQ# enable	Read/Write	1= enable NMI/IRQ# output
3	INT_Clear	Read/Write	1= disable SMI/NMI outputs
4	Not Used	Read/Write	
5	NMI/IRQ# Select	Read/Write	1 selects NMI, 0 selects IRQ#
6	Not Used	Read/Write	
7	INITIALIZATION	Read/Write	1 = restore power on defaults

Interrupt Status Register1 -LM78 address 41h

Bit	Name	Read /Write	Description
0	+3V3 monitor	Read	1=high or limit has been exceeded
1	+5V monitor	Read	1=high or limit has been exceeded
2	+12V monitor	Read	1=high or limit has been exceeded
3	Not Used	Read	
4	Temperature	Read	1=high or limit has been exceeded
5	Not Used	Read	
6	Fan 1	Read	1=fan count limit has been exceeded
7	Fan 2	Read	1=fan count limit has been exceeded

Interrupt Status Register2 -LM78 address 42h

Bit	Name	Read /Write	Description
0	+Spare2 monitor	Read	Not Used
1	-12V monitor	Read	1=high or limit has been exceeded
2	-Spare 1 monitor	Read	Not Used
3	Fan 3	Read	1 = fan count limit has been exceeded
4	Chassis Intrusion	Read	Not Used
5	FIFO over flow	Read	Not Used
6	SMI_IN#	Read	Not Used
7	Reserved	Read	Not Used

IRQ# Mask Register1 -LM78 address 45h

Bit	Name	Read /Write	Description
0	+3V3 monitor	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
1	+5V monitor	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
2	+12V monitor	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
3	Not Used	Read /Write	
4	Temperature	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
5	Not Used	Read /Write	
6	Fan 1	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
7	Fan 2	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt

IRQ# Mask Register2 -LM78 address 46h

Bit	Name	Read /Write	Description
0	Not Used	Read /Write	
1	-12V monitor	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
2	Not Used	Read /Write	
3	Fan 3	Read /Write	1=disable corresponding interrupt status bit for IRQ# interrupt
4	Not Used	Read /Write	
5	Not Used	Read /Write	
6	Not Used	Read /Write	
7	Reserved	Read /Write	

Fan Divisor Register -LM78 address 47h

Bit	Name	Read /Write	Description
3-0	Not Used	Read	
5-4	Fan 1 RPM Control	Read /write	Fan 1 Speed Control <5:4> = 00 - divide by 1 <5:4> = 01 - divide by 2 <5:4> = 10 - divide by 4 <5:4> = 11 - divide by 8
6-7	Fan 2 RPM Control	Read /Write	Fan 2 Speed Control <7:6> = 00 - divide by 1 <7:6> = 01 - divide by 2 <7:6> = 10 - divide by 4 <7:6> = 11 - divide by 8

Chip Reset/ ID Register -LM78 address 49h

Bit	Name	Read /Write	Description
4-0	Reserved	Read	
5	Chip Reset	Read /Write	1= reset all register to default state
6	Device ID	Read	1 =LM78J, 0 = old part
7	Reserved	Read	

Value RAM

Address	Address with Auto increment	Description
20h	60h	+3.3V reading
21h	61h	+5V reading
22h	62h	+12V reading
23h	63h	Not Used
24h	64h	Not Used
25h	65h	-12V reading
26h	66h	Not Used
27h	67h	Temperature reading
28h	68h	Fan1 reading
29h	69h	Fan2 reading
2Ah	6Ah	Fan 3 reading
2Bh	6Bh	+3.3V high limit
2Ch	6Ch	+3.3V low limit
2Dh	6Dh	+5V high limit
2Eh	6Eh	+5V low limit
2Fh	6Fh	+12V high limit
30h	70h	+12V low limit
31h	71h	Not Used
32h	72h	Not Used
33h	73h	Not Used
34h	74h	Not Used

Address	Address with Auto increment	Description
35h	75h	-12V High limit
36h	76h	-12V low limit
37h	77h	Not Used
38h	78h	Not Used
39h	79h	Over temperature limit (high)
3Ah	7Ah	Temperature Hysteresis Limit (low)
3Bh	7Bh	Fan1 count limit
3Ch	7Ch	Fan2 count limit
3Dh	7Dh	Fan3 count limit
3E-3Fh	7E-7Fh	Reserved