# mosaic
semiconductor, inc.

Description

The PUMA 2F4001 is a 4Mbit CMOS 5.0V only FLASH memory in a 66 pin ceramic PGA package, which is configerable as 8, 16, 32 bit wide output using Chip Select 1-4. Access times of 150ns, 170ns and 200ns are available. The device utilises Sector Erase / Program architecture (128 bytes / sector) with Sector program times of 10ms. Data Polling / Toggle bit indication of end of write. The device incorporates Hardware and Software Data protection which disables any program / erase operations. The package includes on-board decoupling capacitors and is suitable for thermal ladder operations.

4,194,304 bit CMOS FLASH Memory Module

Features

- Fast Access Time of 150/170/200ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Operating Power 380/693/1320 mW (max.) Low power standby 6.6 mW (max.)
- JEDEC 66 pin PGA
- Hardware and Software Data Protection
- Page Write (128 Bytes) in 10ms typ.
- Data retention time of 10 years
- Can be screened in accordance with MIL-STD-883.

Block Diagram
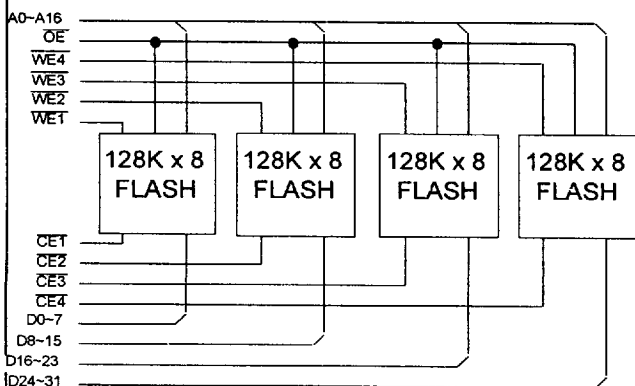
Pin Definition
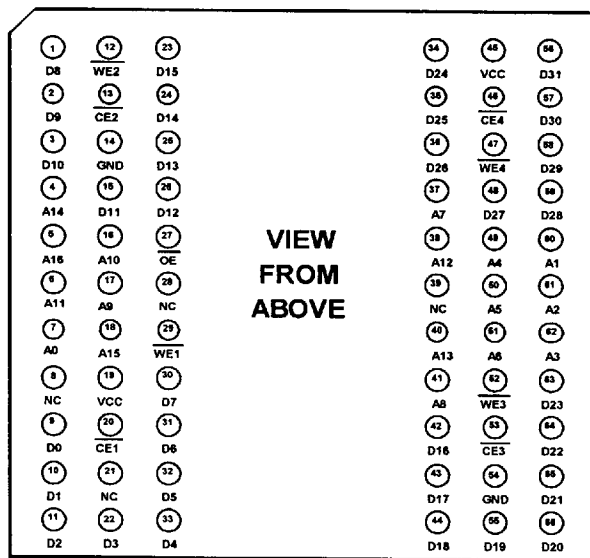
Pin Functions

A0-A16	Address Inputs	D0-D31	Data Input/Output
CS1-4	Chip Selects	WE1-4	Write Enable
OE	Output Enable	NC	No Connect
V$_{cc}$	Power (+5V)	GND	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings [1]

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.5 to +7.0	V
Output voltages with respect to GND	V_{OUT}	-0.5 to +7.0	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	typ	max	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	-	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (**I** Suffix)
	T_{AM}	-55	-	125	°C (**M, MB** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		Symbol	Test Condition	min	max	Unit
Input Leakage Current		I_{LI1}	V_{IN} = GND to V_{CC}	-	10	µA
Output Leakage Current	32 bit	I_{LO}	V_{IN} = GND to V_{CC}, $\overline{CS}^{(1)}$=V_{IH}	-	40	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}^{(1)}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, I_{OUT}=0mA, f=5MHz[2]	-	240	mA
	16 bit	I_{CC16}	As above	-	126	mA
	8 bit	I_{CC8}	As above	-	69	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}^{(1)}$=V_{IH}, $I_{I/O}$=0mA, Other Inputs = V_{IH}	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}^{(1)}$=V_{CC}-0.3V, $I_{I/O}$=0mA, Other Inputs = V_{CC}	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL}=2.1mA.	-	0.4	V
Output High Voltage		V_{OH}	I_{OH}=-400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1-4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		Symbol	Test Condition	typ	max	Unit
Input Capacitance $\overline{CS1}$~4, $\overline{WE}$1~4		C_{IN1}	V_{IN}=0V	-	16	pF
	Other Inputs	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance		C_{OUT}	V_{OUT}=0V	-	22	pF

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Operating Modes

The table below shows the logic inputs required to control the operating modes of each device on the PUMA 2F4001.

MODE	CS	OE	WE	Outputs
Read	0	0	1	Data Out
Write (1)	0	1	0	Data In
Standby	1	X	X	High Z
Write Inhibit	X	X	1	
Write Inhibit	X	0	X	
Output Disable	X	1	X	High Z

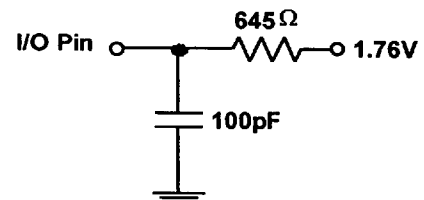$1 = V_{IH}$ $0 = V_{IL}$ X = Don't care

Note : (1) Refer to AC Programming Waveforms

AC Test Conditions   Output Test Load

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{cc}=5V±10%

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AC OPERATING CONDITIONS

Read Cycle

Parameter	Symnbol	-15 min	-15 max	-17 min	-17 max	-20 min	-20 max	Unit	Notes
Read Cycle Time	t_{RC}	150	-	170	-	200	-	ns	
Address Access Time	t_{AA}	-	150	-	170	-	200	ns	
Chip Select Access Time	t_{CS}	-	150	-	170	-	200	ns	
Output Enable Access Time	t_{OE}	0	70	0	80	0	80	ns	
Chip Enable to Output Enable Float	t_{DF}	0	40	0	50	0	50	ns	
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns	

Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	90	-	-	ns
Writ Pulse Width High	t_{WPH}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Byte Cycle Load Time	t_{BLC}	-	-	150	μs

Data Polling

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	10	-	-	ns
Output Enable Hold Time	t_{OEH}	10	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Toggle Bit

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	t_{DH}	10	-	-	ns
Output Enable Hold Time	t_{OEH}	10	-	-	ns
Output Enable High Pulse	t_{OEHP}	150	-	-	ns
Write Recovery Time	t_{WR}	0	-	-	ns

Read Cycle Timing Waveform
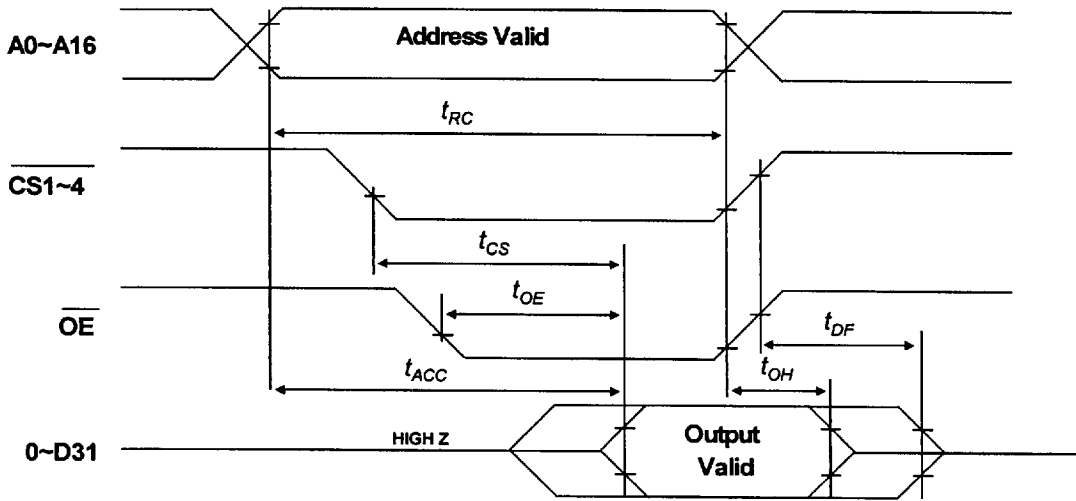
AC Byte Write Waveform - $\overline{WE}$ Controlled

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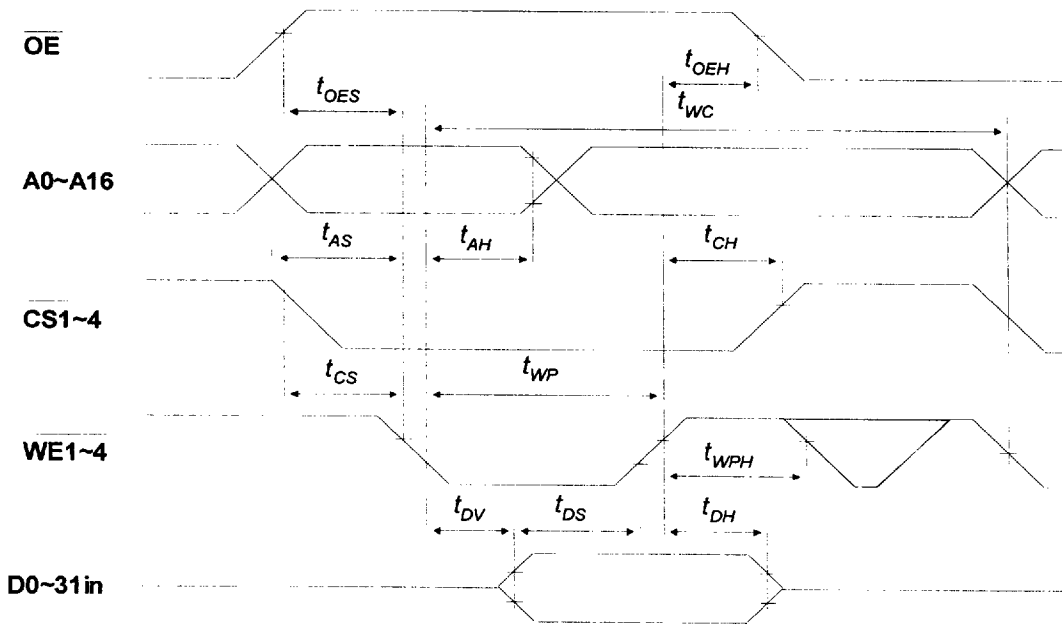
AC Byte Write Waveform - $\overline{CS}$ Controlled
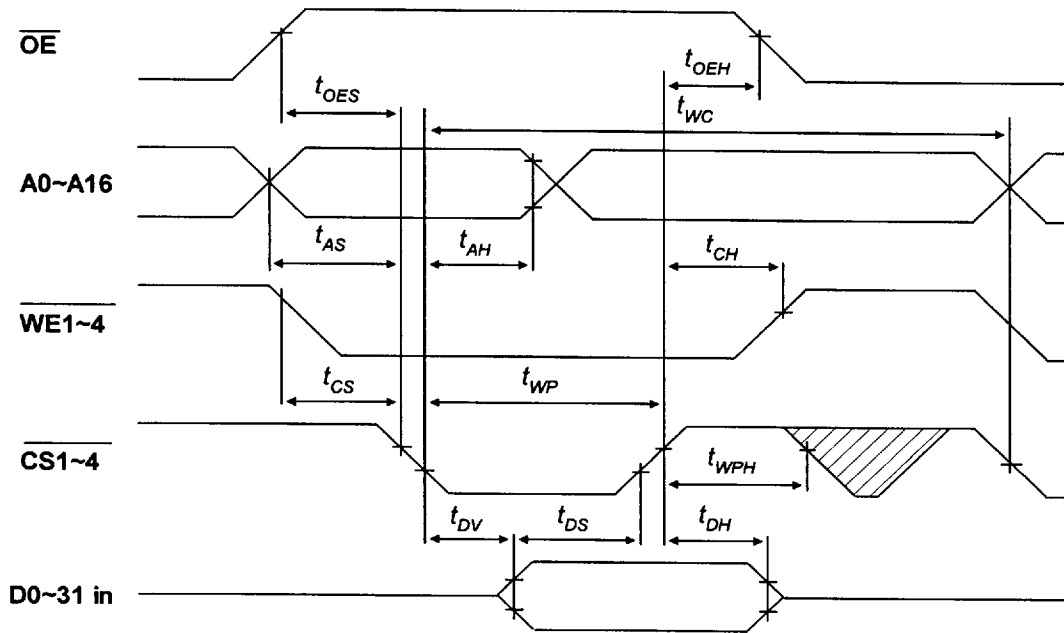
Page Mode Write Waveform

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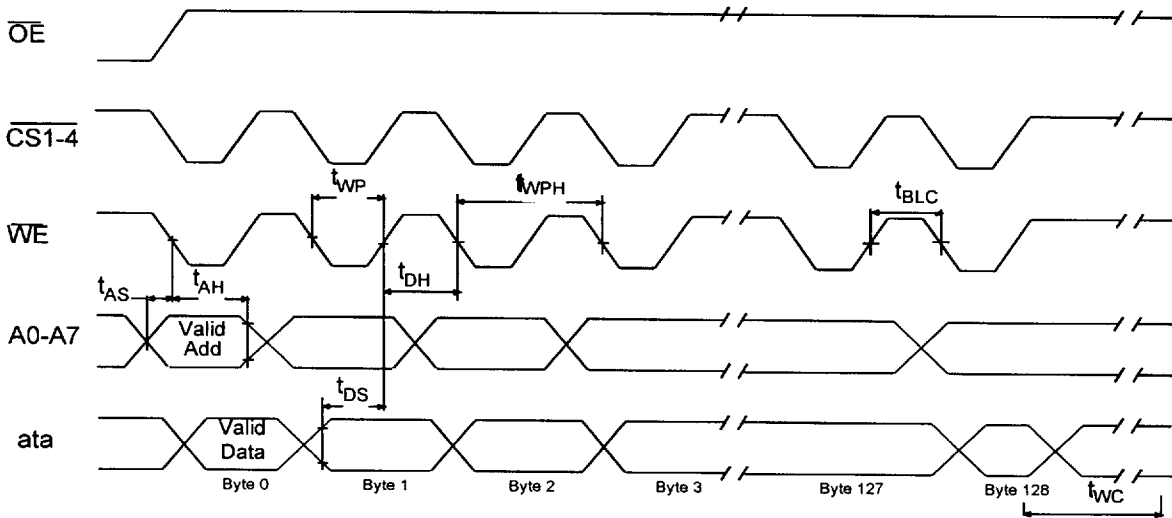
DATA Polling Waveform
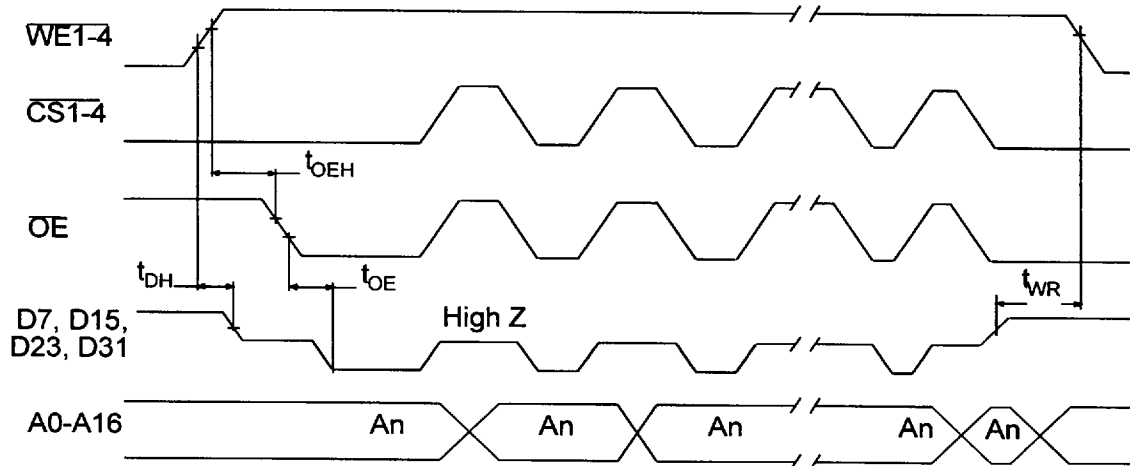
Toggle Bit Waveform
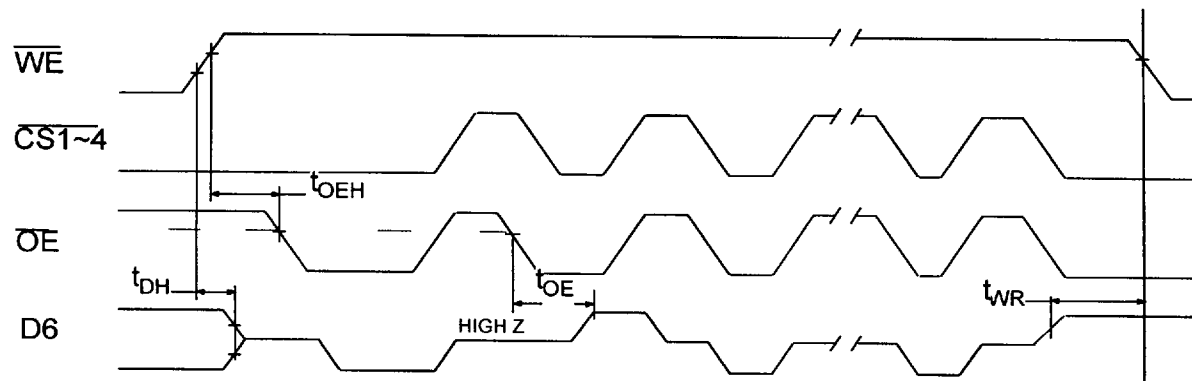
(1) Toggling either OE or CE or both OE and CE will operate toggle bit.
(2) Beginning and adding state of D7, D15, D23, D31 may vary.
(3) Any address location may be used but the address should not vary.

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Software Protected Write Waveform
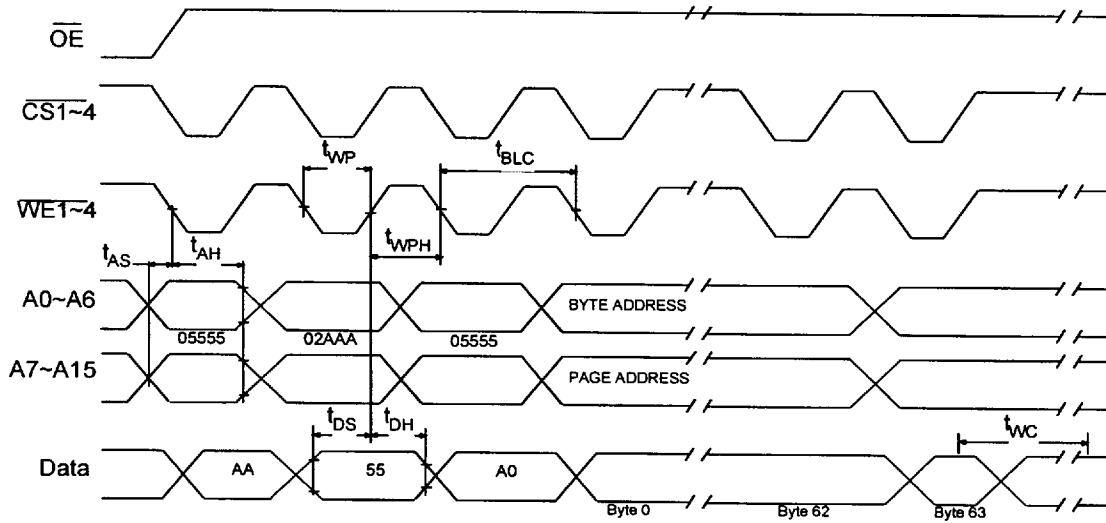
Note: (1)   A7 through A16 must specify the page address during each high to low transition of Write Enable (or Chip select).

(2)   Output Enable must be high only when Write Enable and Chip Select are both low.

(3)   All bytes that are not loaded within the sector being programmed will be erased to FF

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Device Operation

Read

The PUMA 2F4001 read operations are initiated when Write Enable is high and both Output Enable and Chip Select are LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture elimanates bus connection in a system environment. The data bus will be in a high impendence state when either Output Enable or Chip Select is HIGH.

Write

The device is reprogrammed on a sector basis. Byte loads are used to enter the 128 bytes of a sector to be programmed or the software codes for data protection. A byte load is performed by applying a low pulse on the WE or CE input with CE or WE low (respectively) and OE high. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE.

If a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. Once the bytes of a sector are loaded into the device, they are simulateously programmed during the internal programming period. After the first byte has been loaded into the device, successive bytes are loaded in the same manner.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling on D7. Once the end of a program cycle has been detected, a new access for a read or program can begin.

Each new byte to be programmed must have its high to low transition on $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) within 150 µs of the high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the sector address. The sector address must be valid during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$). A0 to A6 specify the byte address within the sector. The bytes may be loaded in any order; sequential loading is not required.

DATA Polling

In order to detect the end of a write cycle, two methods are provided. During a write operation (Byte or Page) an attempt to read the last byte written will result in the compliment of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the write cycle is completed, true data appears on the outputs and the next write cycle nay begin. Using this method of indicating the end of a write can effectively reduce the total write time by 50%.

TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 (D14, D22 or D30, depending on the device selected). toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read as normal, allowing the next write cycle to be performed. This can eliminate the software housekeeping chore and saving and fetching the last address and data written in order to implement DATA polling. This can be especially helpful in an array composed of multiple PUMA 2F4001 modules that are frequently updated.

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Hardware Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

- If $V_{cc} < 3.8V$, Write is inhibited.
- $\overline{OE}$ low, $\overline{CS}$ or $\overline{WE}$ high inhibits inadvertant Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.
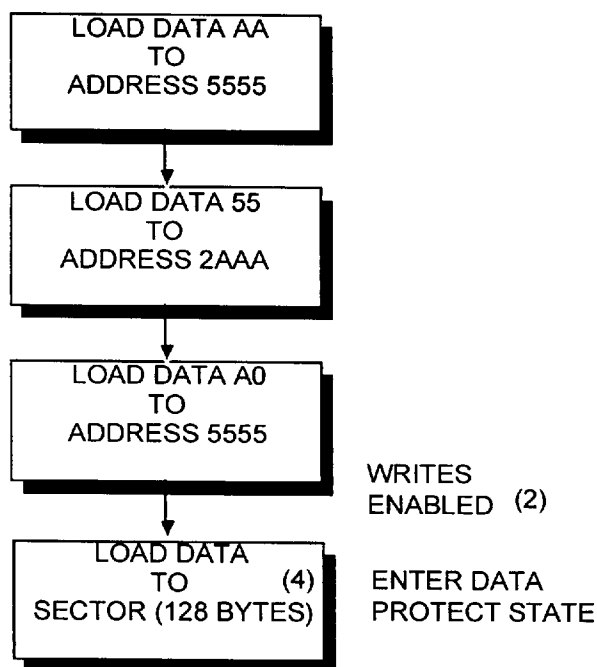- Pulses are less than 15ns on $\overline{WE}$ do not initiate a Write Cycle.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is

Software Data Protection

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected sate. After the Software data protection is enabled the same three program commands must begin each program cycle inorder for the programs to occur. Once set the Software data protection feature remains active unless the dissable command is issued.

Software Data Protection Algorithm (1)

Regardless of wheather the device has been protected or not, once the software data protected aglorithm is used and the data is written, the PUMA 2F4001 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the PUMA 2F4001 will be write protected during power-down and any subsequent power-up.

```
┌─────────────────────┐
│   LOAD DATA AA      │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA 55      │
│        TO           │
│   ADDRESS 2AAA      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA A0      │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘        WRITES
          │                    ENABLED (2)
          ▼
┌─────────────────────┐
│   LOAD DATA         │
│        TO      (4)  │        ENTER DATA
│  SECTOR (128 BYTES) │        PROTECT STATE
└─────────────────────┘
```

Notes:
(1) Data Format I/O7-I/O0 (Hex);
   Once initiated, this sequence of write operations should not be interrupted.
(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.
(3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.
(4) 128 bytes of data must be loaded.

Mosaic Semiconductor, Inc., 7420 Carroll Rd. Suite 300, San Diego, CA 92121   Tel: 619.271.4565 Fax: 619.271.6058

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Software Data Protect Disable Algorithm

In the event the user wants to deactivate the software data protection feature for treprogramming ithe following six step algorithm will reset the internal protection circuit. After t_{wc}, the PUMA 2F4001 will be in standard operating mode.

```
┌─────────────────────┐
│   LOAD DATA AA      │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA 55      │
│        TO           │
│   ADDRESS 2AAA      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA 80      │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA AA      │
│        TO           │
│   ADDRESS 5555      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA 55      │
│        TO           │
│   ADDRESS 2AAA      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐                 EXIT DATA
│   LOAD DATA 20      │                 PROTECT
│        TO           │                 STATE  (3)
│   ADDRESS 5555      │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│   LOAD DATA XX      │
│        TO           │
│   ANY ADDRESS (4)   │
└─────────────────────┘
          │
          ▼
┌─────────────────────┐
│  LOAD LAST BYTE     │
│        TO           │
│   LAST ADDRESS      │
└─────────────────────┘
```

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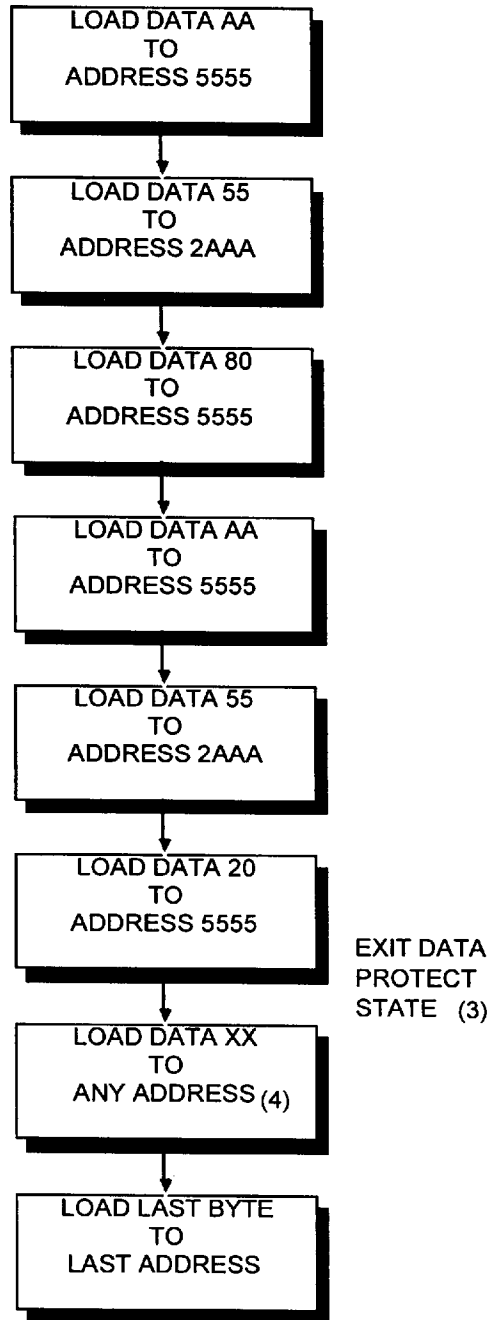
Chip Erase Algorithm

The Puma 2F4001 offers a chip erase function in which the entire device can be erased in 20 ms by a six byte algorithm. Once this code has been entered, the device will set each byte to a high state, (FFh) erasing any stored data. The device will also internally time this operation so that no external clocks are needed.

```
┌──────────────────────┐
│    LOAD DATA AA      │
│         TO          │
│   ADDRESS 5555      │
└──────────────────────┘
          │
          ▼
┌──────────────────────┐
│    LOAD DATA 55      │
│         TO          │
│   ADDRESS 2AAA      │
└──────────────────────┘
          │
          ▼
┌──────────────────────┐
│    LOAD DATA 80      │
│         TO          │
│   ADDRESS 5555      │
└──────────────────────┘
          │
          ▼
┌──────────────────────┐
│    LOAD DATA AA      │
│         TO          │
│   ADDRESS 5555      │
└──────────────────────┘
          │
          ▼
┌──────────────────────┐
│    LOAD DATA 55      │
│         TO          │
│   ADDRESS 2AAA      │
└──────────────────────┘
          │
          ▼
┌──────────────────────┐
│    LOAD DATA 10      │
│         TO          │
│   ADDRESS 5555      │
└──────────────────────┘
```

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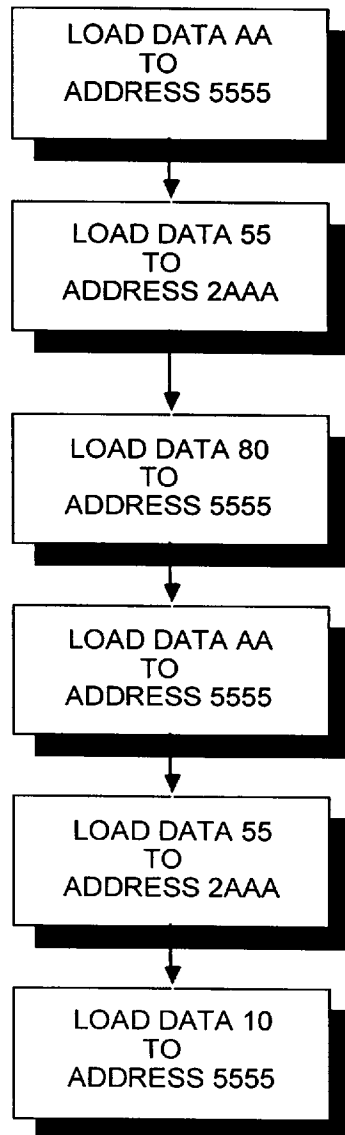
Package Details (Dimensions in mm (inches))

27.58 (1.086) square
27.08 (1.066) square

LEAD FINISH IS 300 µINCH MINIMUM
SOLDER OVER 50 TO 350 µINCH NICKEL

8.13 (0.320) max

1.52 (0.060)
1.02 (0.040)

4.83 (0.190)
4.32 (0.170)

0.53 (0.021)
0.38 (0.015)

1.27 (0.050)

1.27 (0.050)
1.66 (0.026)

2.54 (0.010)

15.24 (0.60) typ

3.81 (0.150) ref

2.54 (0.010)

10.67 (0.420)
10.16 (0.400)
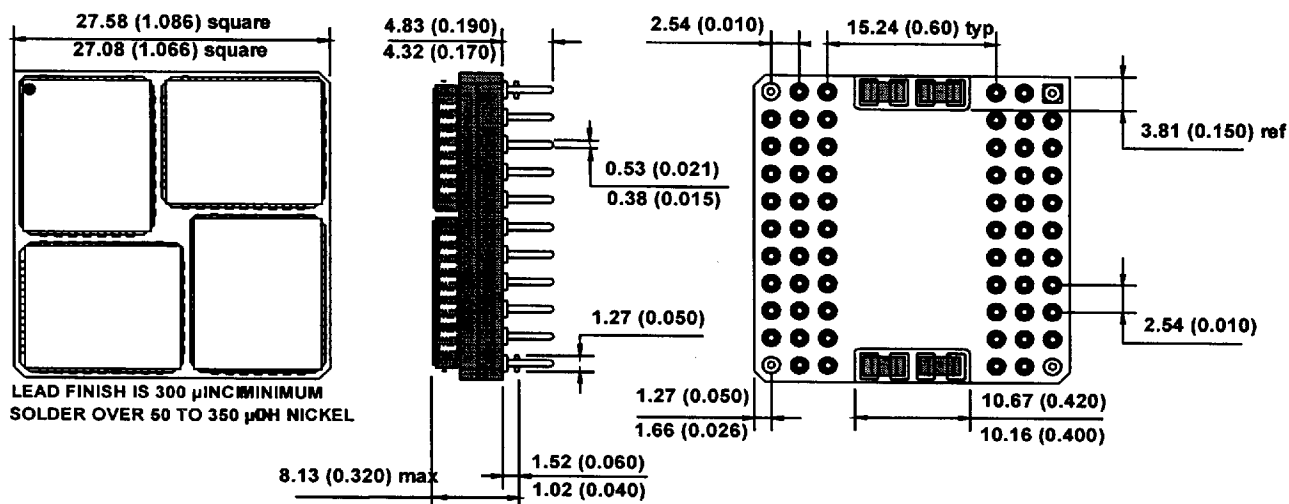
Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with Mil-883 method 5004.

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable Device Specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C, 160 hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	5%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

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Ordering Information

PUMA 2 F 4001 MB -15

Speed
- 15 = 150 ns
- 17 = 170 ns
- 20 = 200 ns

Temp. range/screening
- Blank = Commercial Temperature
- I = Industrial Temperature
- M = Military Temperature
- MB = Screened in accordance with MIL·STD·883

Organisation
- 4001 = 128K x 32, user configurable as 256K x 16 and 512K x 8

Memory Type
- F = FLASH

Package
- PUMA 2 = 66 pin Ceramic PGA

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