

# DATA SHEET

## **74HC4052; 74HCT4052**

**Dual 4-channel analog multiplexer,  
demultiplexer**

Product specification  
Supersedes data of 2003 May 16

2004 Nov 11

## Dual 4-channel analog multiplexer, demultiplexer

## 74HC4052; 74HCT4052

### FEATURES

- Wide analog input voltage range from  $-5\text{ V}$  to  $+5\text{ V}$
- Low ON-resistance:
  - $80\ \Omega$  (typical) at  $V_{CC} - V_{EE} = 4.5\text{ V}$
  - $70\ \Omega$  (typical) at  $V_{CC} - V_{EE} = 6.0\text{ V}$
  - $60\ \Omega$  (typical) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation: to enable  $5\text{ V}$  logic to communicate with  $\pm 5\text{ V}$  analog signals
- Typical “break before make” built in
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds  $2000\text{ V}$
  - MM EIA/JESD22-A115-A exceeds  $200\text{ V}$ .
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

### APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating.

### DESCRIPTION

The 74HC4052 and 74HCT4052 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4052B. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4052 and 74HCT4052 are dual 4-channel analog multiplexers or demultiplexers with common select logic. Each multiplexer has four independent inputs/outputs (pins nY0 to nY3) and a common input/output (pin nZ). The common channel select logics include two digital select inputs (pins S0 and S1) and an active LOW enable input (pin  $\bar{E}$ ). When pin  $\bar{E} = \text{LOW}$ , one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin  $\bar{E} = \text{HIGH}$ , all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs (pins S0, S1, and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are  $2.0\text{ V}$  to  $10.0\text{ V}$  for 74HC4052 and  $4.5\text{ V}$  to  $5.5\text{ V}$  for 74HCT4052. The analog inputs/outputs (pins nY0 to nY3 and nZ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed  $10.0\text{ V}$ .

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

### FUNCTION TABLE

INPUT <sup>(1)</sup>			CHANNEL BETWEEN
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

### Note

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care.

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## QUICK REFERENCE DATA

 $V_{EE} = GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f = 6\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC4052	74HCT4052	
$t_{PZH}/t_{PZL}$	turn-on time $\bar{E}$ or Sn to $V_{OS}$	$C_L = 15\text{ pF}$ ; $R_L = 1\text{ k}\Omega$ ; $V_{CC} = 5\text{ V}$	28	18	ns
$t_{PHZ}/t_{PLZ}$	turn-off time $\bar{E}$ or Sn to $V_{OS}$	$C_L = 15\text{ pF}$ ; $R_L = 1\text{ k}\Omega$ ; $V_{CC} = 5\text{ V}$	21	13	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	57	57	pF
$C_S$	maximum switch capacitance	independent (Y)	5	5	pF
		common (Z)	12	12	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o] \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$C_S$  = maximum switch capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = number of inputs switching;

$\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$  = sum of the outputs.

2. For 74HC4052 the condition is  $V_I = GND$  to  $V_{CC}$

For 74HCT4052 the condition is  $V_I = GND$  to  $V_{CC} - 1.5\text{ V}$ .

## ORDERING INFORMATION

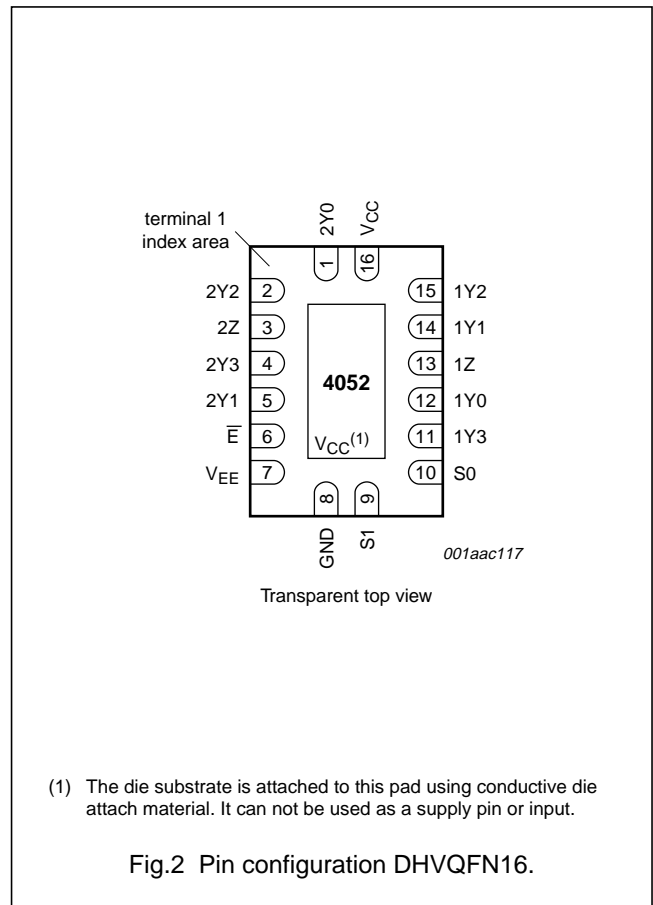
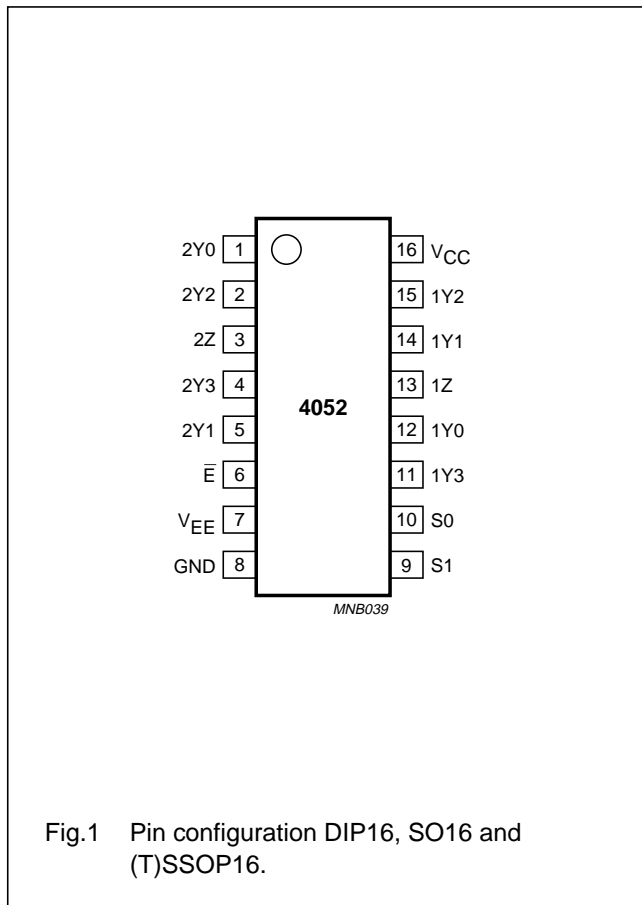
TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC4052D	-40 °C to +125 °C	16	SO16	plastic	SOT109-3
74HCT4052D	-40 °C to +125 °C	16	SO16	plastic	SOT109-3
74HC4052DB	-40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74HCT4052DB	-40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74HC4052N	-40 °C to +125 °C	16	DIP16	plastic	SOT38-9
74HCT4052N	-40 °C to +125 °C	16	DIP16	plastic	SOT38-9
74HC4052PW	-40 °C to +125 °C	16	TSSOP16	plastic	SOT403-1
74HC4052BQ	-40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1
74HCT4052BQ	-40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1

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## PINNING

PIN	SYMBOL	DESCRIPTION
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V <sub>EE</sub>	negative supply voltage
8	GND	ground (0 V)
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V <sub>CC</sub>	positive supply voltage



# Dual 4-channel analog multiplexer, demultiplexer

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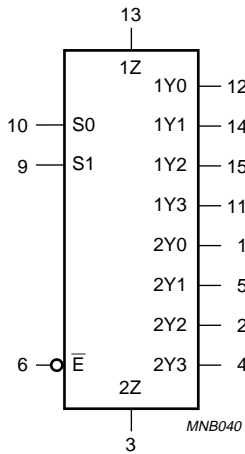


Fig.3 Logic symbol.

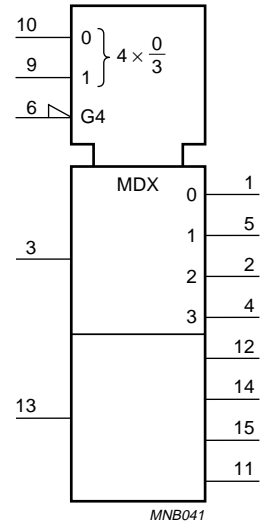


Fig.4 IEC logic symbol.

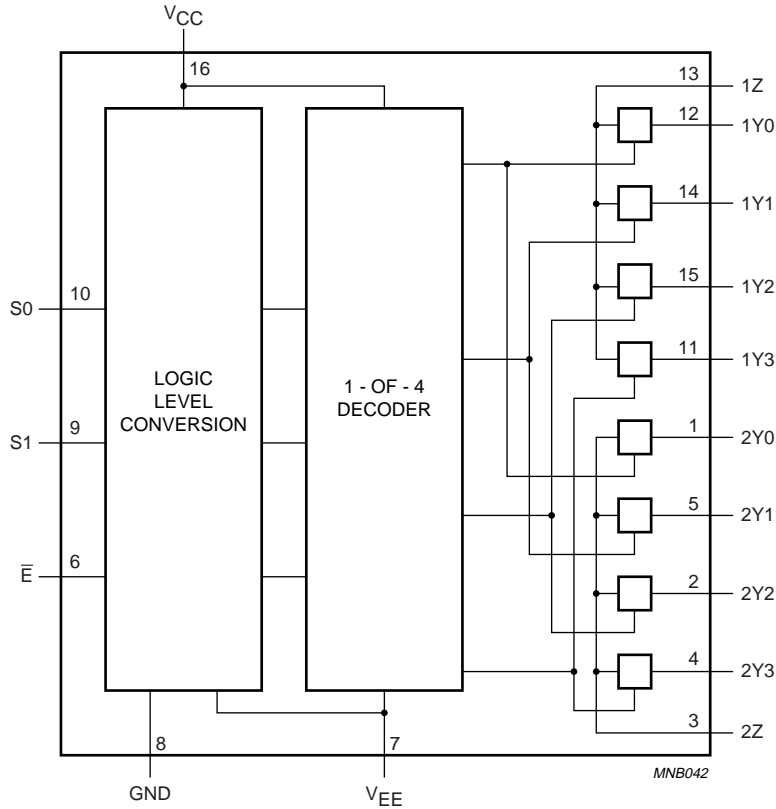


Fig.5 Functional diagram.

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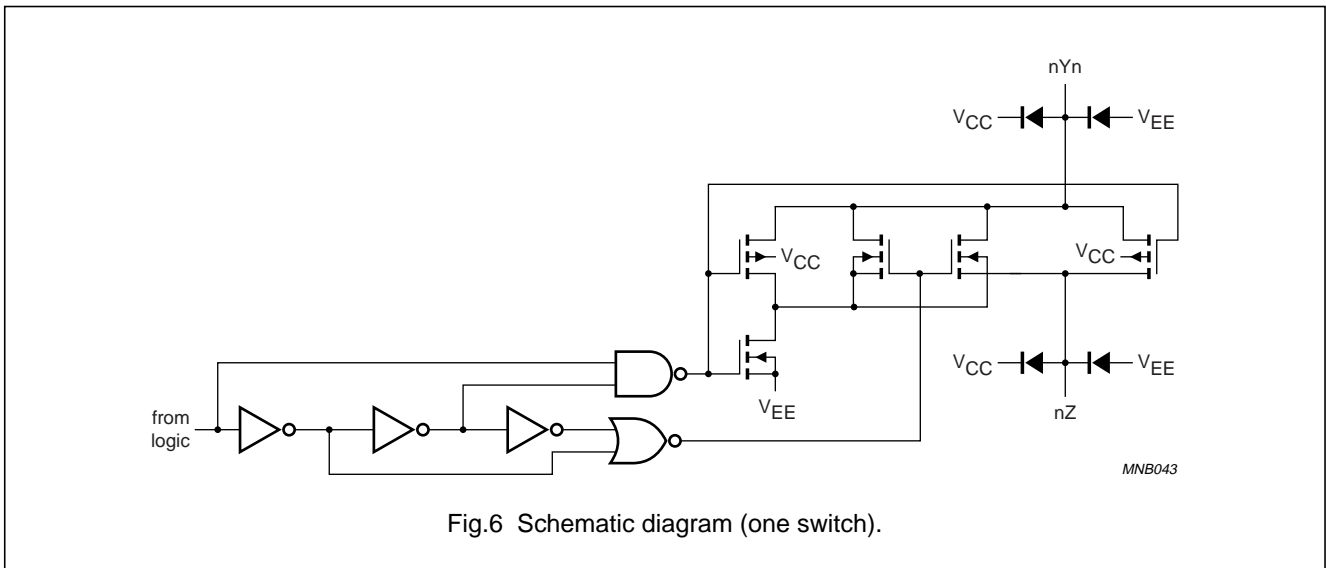


Fig.6 Schematic diagram (one switch).

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to  $V_{EE} = GND$  (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+11.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SK}$	switch diode current	$V_S < -0.5\text{ V}$ or $V_S > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_S$	switch current	$-0.5\text{ V} < V_S < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{EE}$	$V_{EE}$ current		-	$\pm 20$	mA
$I_{CC}; I_{GND}$	$V_{CC}$ or GND current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ ; note	-	500	mW
$P_S$	power dissipation per switch		-	100	mW

**Notes**

- To avoid drawing  $V_{CC}$  current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no  $V_{CC}$  current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed  $V_{CC}$  or  $V_{EE}$ .
- For DIP16 packages: above 70 °C derate linearly with 12 mW/K.  
 For SO16 packages: above 70 °C derate linearly with 8 mW/K.  
 For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC4052			74HCT4052			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V <sub>CC</sub>	supply voltage	see Figs 7 and 8							
		V <sub>CC</sub> – GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V <sub>CC</sub> – V <sub>EE</sub>	2.0	5.0	10.0	2.0	5.0	10.0	V
V <sub>I</sub>	input voltage		GND	–	V <sub>CC</sub>	GND	–	V <sub>CC</sub>	V
V <sub>S</sub>	switch voltage		V <sub>EE</sub>	–	V <sub>CC</sub>	V <sub>EE</sub>	–	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	–	+125	–40	–	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 2.0 V	–	6.0	1000	–	6.0	500	ns
		V <sub>CC</sub> = 4.5 V	–	6.0	500	–	6.0	500	ns
		V <sub>CC</sub> = 6.0 V	–	6.0	400	–	6.0	500	ns
		V <sub>CC</sub> = 10.0 V	–	6.0	250	–	6.0	500	ns

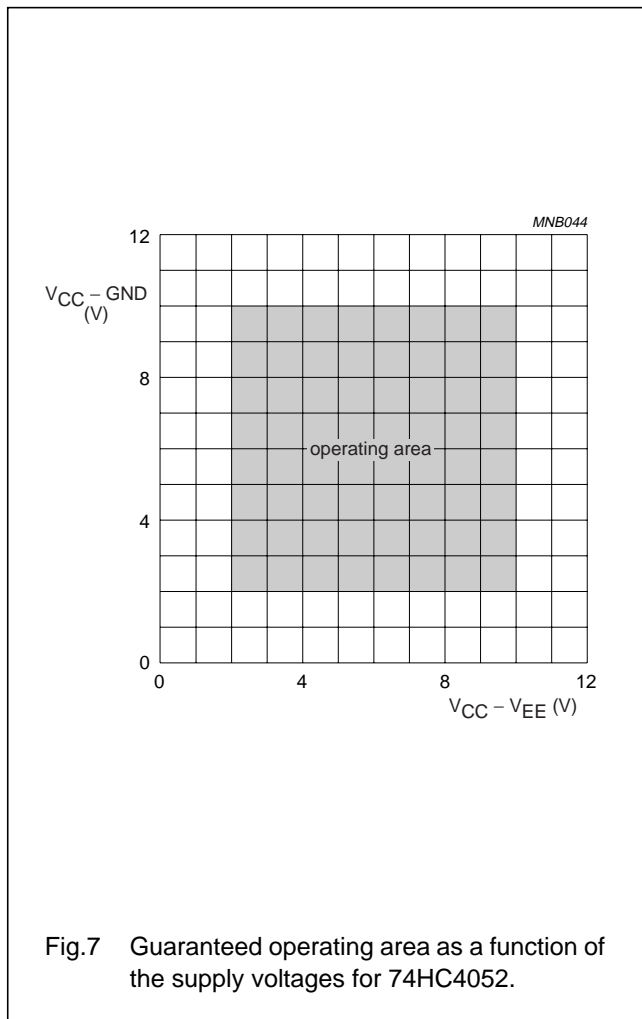


Fig.7 Guaranteed operating area as a function of the supply voltages for 74HC4052.

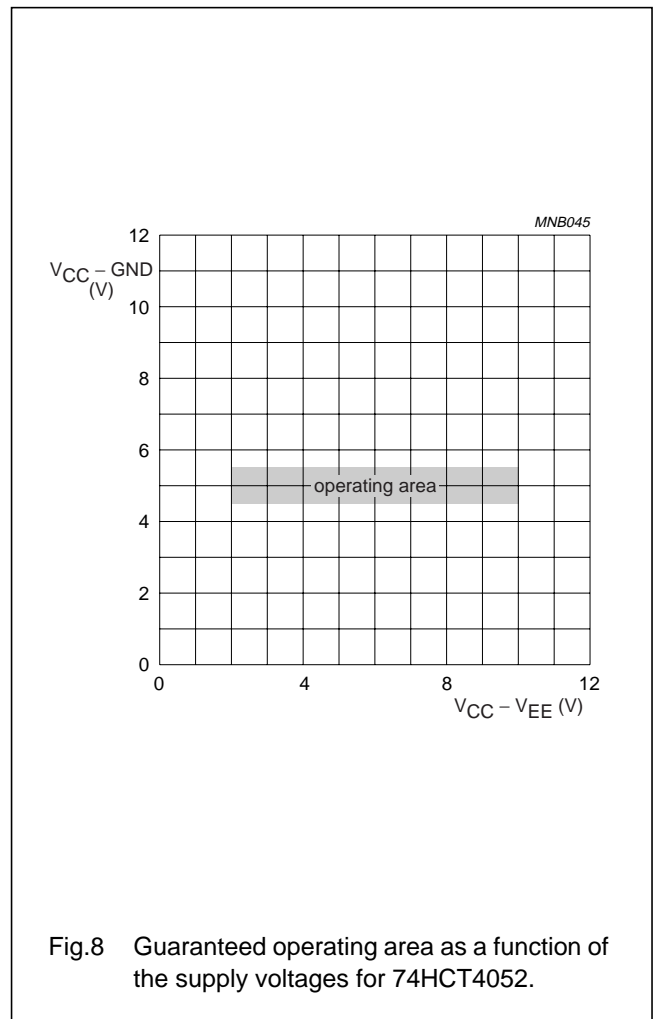


Fig.8 Guaranteed operating area as a function of the supply voltages for 74HCT4052.

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## DC CHARACTERISTICS

## Family 74HC4052

$V_{is}$  is the input voltage at pins nYn or nZ, whichever is assigned as an input;  $V_{os}$  is the output voltage at pins nZ or nYn, whichever is assigned as an output; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{CC}$ (V)	$V_{EE}$ (V)				
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ ; note 1								
$V_{IH}$	HIGH-level input voltage		2.0	–	1.5	1.2	–	V
			4.5	–	3.15	2.4	–	V
			6.0	–	4.2	3.2	–	V
			9.0	–	6.3	4.7	–	V
$V_{IL}$	LOW-level input voltage		2.0	–	–	0.8	0.5	V
			4.5	–	–	2.1	1.35	V
			6.0	–	–	2.8	1.8	V
			9.0	–	–	4.3	2.7	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND	6.0	0	–	–	$\pm 1.0$	$\mu\text{A}$
			10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ M_S  = V_{CC} - V_{EE}$ ; see Fig.9 per channel all channels	10.0	0	–	–	$\pm 1.0$	$\mu\text{A}$
			10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ M_S  = V_{CC} - V_{EE}$ ; see Fig.10	10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $V_{EE}$	6.0	0	–	–	80.0	$\mu\text{A}$
			10.0	0	–	–	160.0	$\mu\text{A}$



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SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)	V <sub>EE</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>								
V <sub>IH</sub>	HIGH-level input voltage		2.0	–	1.5	–	–	V
			4.5	–	3.15	–	–	V
			6.0	–	4.2	–	–	V
			9.0	–	6.3	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	–	0.5	V
			4.5	–	–	–	1.35	V
			6.0	–	–	–	1.8	V
			9.0	–	–	–	2.7	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	0	–	–	±1.0	μA
			10.0	0	–	–	±2.0	μA
I <sub>S(OFF)</sub>	analog switch OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  M <sub>S</sub>   = V <sub>CC</sub> – V <sub>EE</sub> ; see Fig.9 per channel all channels	10.0	0	–	–	±1.0	μA
			10.0	0	–	–	±2.0	μA
I <sub>S(ON)</sub>	analog switch ON-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  M <sub>S</sub>   = V <sub>CC</sub> – V <sub>EE</sub> ; see Fig.10	10.0	0	–	–	±2.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub>	6.0	0	–	–	160	μA
			10.0	0	–	–	320.0	μA

**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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## Family 74HCT4052

$V_{is}$  is the input voltage at pins nYn or nZ, whichever is assigned as an input;  $V_{os}$  is the output voltage at pins nZ or nYn, whichever is assigned as an output; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{CC}$ (V)	$V_{EE}$ (V)				
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}</math>; note 1</b>								
$V_{IH}$	HIGH-level input voltage		4.5 to 5.5	–	2.0	1.6	–	V
$V_{IL}$	LOW-level input voltage		4.5 to 5.5	–	–	1.2	0.8	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND	5.5	0	–	–	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - V_{EE}$ ; see Fig.9 per channel	10.0	0	–	–	$\pm 1.0$	$\mu\text{A}$
			10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - V_{EE}$ ; see Fig.10	10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $V_{EE}$	5.5	0	–	–	80.0	$\mu\text{A}$
			5.0	–5.0	–	–	160.0	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current per input	$V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND	4.5 to 5.5	0	–	45	202.5	$\mu\text{A}$
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}</math></b>								
$V_{IH}$	HIGH-level input voltage		4.5 to 5.5	–	2.0	–	–	V
$V_{IL}$	LOW-level input voltage		4.5 to 5.5	–	–	–	0.8	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND	5.5	0	–	–	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	analog switch OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - V_{EE}$ ; see Fig.9 per channel	10.0	0	–	–	$\pm 1.0$	$\mu\text{A}$
			10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{S(ON)}$	analog switch ON-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - V_{EE}$ ; see Fig.10	10.0	0	–	–	$\pm 2.0$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or $V_{CC}$ ; $V_{os} = V_{CC}$ or $V_{EE}$	5.5	0	–	–	160.0	$\mu\text{A}$
			5.0	–5.0	–	–	320.0	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current per input	$V_I = V_{CC} - 2.1\text{ V}$ ; other inputs at $V_{CC}$ or GND	4.5 to 5.5	0	–	–	220.5	$\mu\text{A}$

## Note

1. All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

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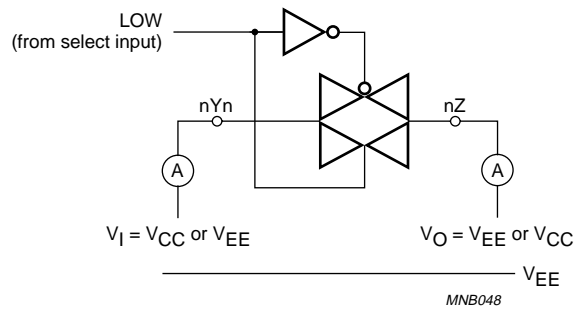


Fig.9 Test circuit for measuring OFF-state current.

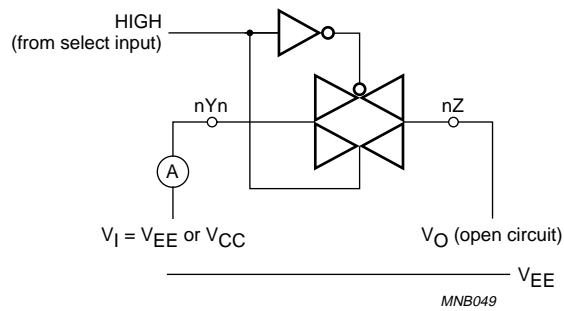


Fig.10 Test circuit for measuring ON-state current.

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**Resistance  $R_{ON}$  for 74HC4052 and 74HCT4052** $V_{IS}$  is the input voltage at pins nYn or nZ, whichever is assigned as an input; see notes 1 and 2; see Fig.11.

SYMBOL	PARAMETER	TEST CONDITIONS				MIN.	TYP.	MAX.	UNIT	
		OTHER	$V_{CC}$ (V)	$V_{EE}$ (V)	$I_S$ ( $\mu$ A)					
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C}</math> to <math>+85\text{ }^{\circ}\text{C}</math>; note 3</b>										
$R_{ON(peak)}$	ON-resistance (peak)	$V_{IS} = V_{CC}$ to $V_{EE}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	–	–	$\Omega$	
			4.5	0	1000	–	100	225	$\Omega$	
			6.0	0	1000	–	90	200	$\Omega$	
			4.5	–4.5	1000	–	70	165	$\Omega$	
$R_{ON(rail)}$	ON-resistance (rail)	$V_{IS} = V_{EE}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	150	–	$\Omega$	
			4.5	0	1000	–	80	175	$\Omega$	
			6.0	0	1000	–	70	150	$\Omega$	
			4.5	–4.5	1000	–	60	130	$\Omega$	
			$V_{IS} = V_{CC}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	150	–	$\Omega$
				4.5	0	1000	–	90	200	$\Omega$
				6.0	0	1000	–	80	175	$\Omega$
				4.5	–4.5	1000	–	65	150	$\Omega$
$\Delta R_{ON}$	maximum ON-resistance difference between any two channels	$V_{IS} = V_{CC}$ to $V_{EE}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	–	–	–	–	$\Omega$	
			4.5	0	–	–	9	–	$\Omega$	
			6.0	0	–	–	8	–	$\Omega$	
			4.5	–4.5	–	–	6	–	$\Omega$	
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C}</math> to <math>+125\text{ }^{\circ}\text{C}</math></b>										
$R_{ON(peak)}$	ON-resistance (peak)	$V_{IS} = V_{CC}$ to $V_{EE}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	–	–	$\Omega$	
			4.5	0	1000	–	–	270	$\Omega$	
			6.0	0	1000	–	–	240	$\Omega$	
			4.5	–4.5	1000	–	–	195	$\Omega$	
$R_{ON(rail)}$	ON-resistance (rail)	$V_{IS} = V_{EE}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	–	–	$\Omega$	
			4.5	0	1000	–	–	210	$\Omega$	
			6.0	0	1000	–	–	180	$\Omega$	
			4.5	–4.5	1000	–	–	160	$\Omega$	
			$V_{IS} = V_{CC}$ ; $V_I = V_{IH}$ or $V_{IL}$	2.0	0	100	–	–	–	$\Omega$
				4.5	0	1000	–	–	240	$\Omega$
				6.0	0	1000	–	–	210	$\Omega$
				4.5	–4.5	1000	–	–	180	$\Omega$

**Notes**

- For 74HC4052:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V; for 74HCT4052:  $V_{CC} - GND = 4.5$  and  $5.5$  V,  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V.
- When supply voltages ( $V_{CC} - V_{EE}$ ) near 2.0 V the analog switch ON-resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.
- All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

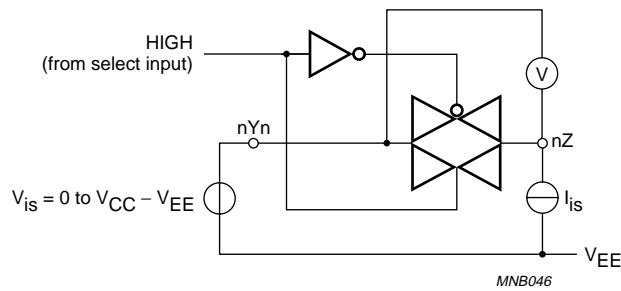
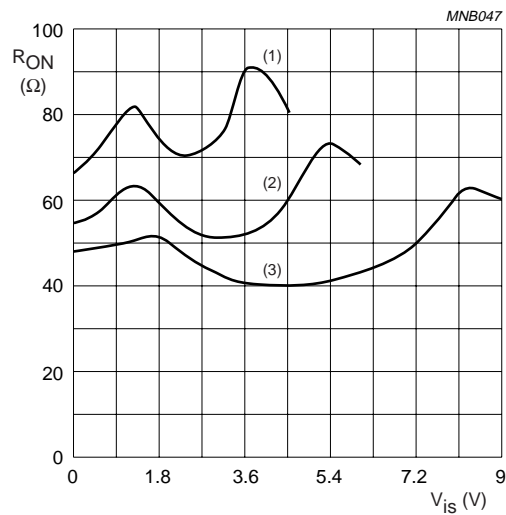


Fig.11 Test circuit for measuring  $R_{ON}$ .



$V_{is} = 0$  V to  $V_{CC} - V_{EE}$   
 (1)  $V_{CC} = 4.5$  V  
 (2)  $V_{CC} = 6$  V  
 (3)  $V_{CC} = 9$  V

Fig.12 Typical  $R_{ON}$  as a function of input voltage  $V_{is}$ .

Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

## AC CHARACTERISTICS

## Type 74HC4052

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{CC}$ (V)	$V_{EE}$ (V)				
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C; note 1</b>								
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$	$R_L = \infty$ ; see Fig.19	2.0	0	–	14	75	ns
			4.5	0	–	5	15	ns
			6.0	0	–	4	13	ns
			4.5	–4.5	–	4	10	ns
$t_{PZH}/t_{PZL}$	turn-on time $\bar{E}$ , Sn to $V_{os}$	$R_L = \infty$ ; see Figs 20, 22 and 21	2.0	0	–	105	405	ns
			4.5	0	–	38	81	ns
			6.0	0	–	30	69	ns
			4.5	–4.5	–	26	58	ns
$t_{PHZ}/t_{PLZ}$	turn-off time $\bar{E}$ , Sn to $V_{os}$	$R_L = 1$ k $\Omega$ ; see Figs 20, 22 and 21	2.0	0	–	74	315	ns
			4.5	0	–	27	63	ns
			6.0	0	–	22	54	ns
			4.5	–4.5	–	22	48	ns
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>								
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$	$R_L = \infty$ ; see Fig.19	2.0	0	–	–	90	ns
			4.5	0	–	–	18	ns
			6.0	0	–	–	15	ns
			4.5	–4.5	–	–	12	ns
$t_{PZH}/t_{PZL}$	turn-on time $\bar{E}$ , Sn to $V_{os}$	$R_L = \infty$ ; see Figs 20, 22 and 21	2.0	0	–	–	490	ns
			4.5	0	–	–	98	ns
			6.0	0	–	–	83	ns
			4.5	–4.5	–	–	69	ns
$t_{PHZ}/t_{PLZ}$	turn-off time $\bar{E}$ , Sn to $V_{os}$	$R_L = 1$ k $\Omega$ ; see Figs 20, 22 and 21	2.0	0	–	–	375	ns
			4.5	0	–	–	75	ns
			6.0	0	–	–	64	ns
			4.5	–4.5	–	–	57	ns

## Note

1. All typical values are measured at  $T_{amb} = 25$  °C.

Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

**Type 74HCT4052**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)	V <sub>EE</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>								
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>	R <sub>L</sub> = ∞; see Fig.19	4.5	0	–	5	15	ns
			4.5	–4.5	–	4	10	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	turn-on time $\bar{E}$ , Sn to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	41	88	ns
			4.5	–4.5	–	28	60	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	turn-off time $\bar{E}$ , Sn to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	26	63	ns
			4.5	–4.5	–	21	48	ns
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>								
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>	R <sub>L</sub> = ∞; see Fig.19	4.5	0	–	–	18	ns
			4.5	–4.5	–	–	12	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	turn-on time $\bar{E}$ , Sn to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	–	105	ns
			4.5	–4.5	–	–	72	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	turn-off time $\bar{E}$ , Sn to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; see Figs 20, 22 and 21	4.5	0	–	–	75	ns
			4.5	–4.5	–	–	57	ns

**Note**1. All typical values are measured at T<sub>amb</sub> = 25 °C.

# Dual 4-channel analog multiplexer, demultiplexer

## 74HC4052; 74HCT4052

### Type 74HC4052 and 74HCT4052

Recommended conditions and typical values; GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ .  $V_{is}$  is the input voltage at pins nYn or nZ, whichever is assigned as an input.  $V_{os}$  is the output voltage at pins nYn or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS				TYP.	UNIT
		OTHER	$V_{is(p-p)}$ (V)	$V_{CC}$ (V)	$V_{EE}$ (V)		
$d_{sin}$	sine-wave distortion	f = 1 kHz; $R_L = 10\text{ k}\Omega$ ; see Fig.13	4.0	2.25	-2.25	0.04	%
			8.0	4.5	-4.5	0.02	%
		f = 10 kHz; $R_L = 10\text{ k}\Omega$ ; see Fig.13	4.0	2.25	-2.25	0.12	%
			8.0	4.5	-4.5	0.06	%
$\alpha_{OFF(feedthr)}$	switch OFF signal feed-through	$R_L = 600\text{ }\Omega$ ; f = 1 MHz; see Figs 14 and 15	note 1	2.25	-2.25	-50	dB
				4.5	-4.5	-50	dB
$\alpha_{ct(s)}$	crosstalk between two switches/multiplexers	$R_L = 600\text{ }\Omega$ ; f = 1 MHz; see Fig.16	note 1	2.25	-2.25	-60	dB
				4.5	-4.5	-60	dB
$V_{ct(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	$R_L = 600\text{ }\Omega$ ; f = 1 MHz; $\bar{E}$ or Sn, square-wave between $V_{CC}$ and GND, $t_r = t_f = 6\text{ ns}$ ; see Fig.17	-	4.5	0	110	mV
				4.5	-4.5	220	mV
$f_{max}$	minimum frequency response (-3dB)	$R_L = 50\text{ }\Omega$ ; see Figs 13 and 18	note 2	2.25	-2.25	170	MHz
				4.5	-4.5	180	MHz
$C_S$	maximum switch capacitance	independent (Y)	-	-	-	5	pF
		common (Z)	-	-	-	12	pF

### Notes

1. Adjust input voltage  $V_{is}$  to 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).
2. Adjust input voltage  $V_{is}$  to 0 dBm level at  $V_{os}$  for 1 MHz (0 dBm = 1 mW into 50  $\Omega$ ).

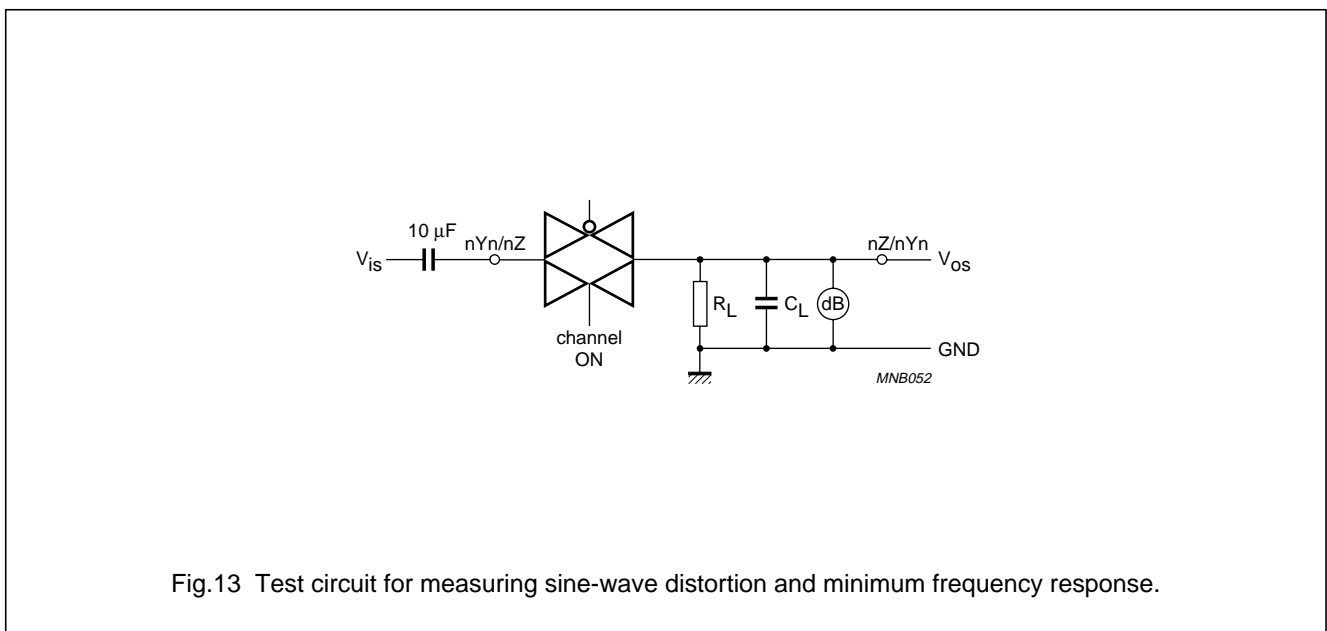


Fig.13 Test circuit for measuring sine-wave distortion and minimum frequency response.



Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

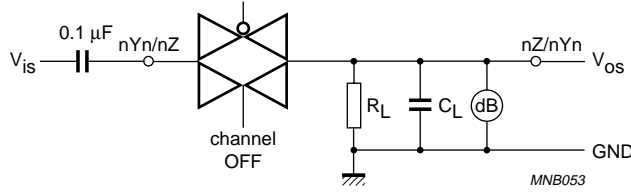
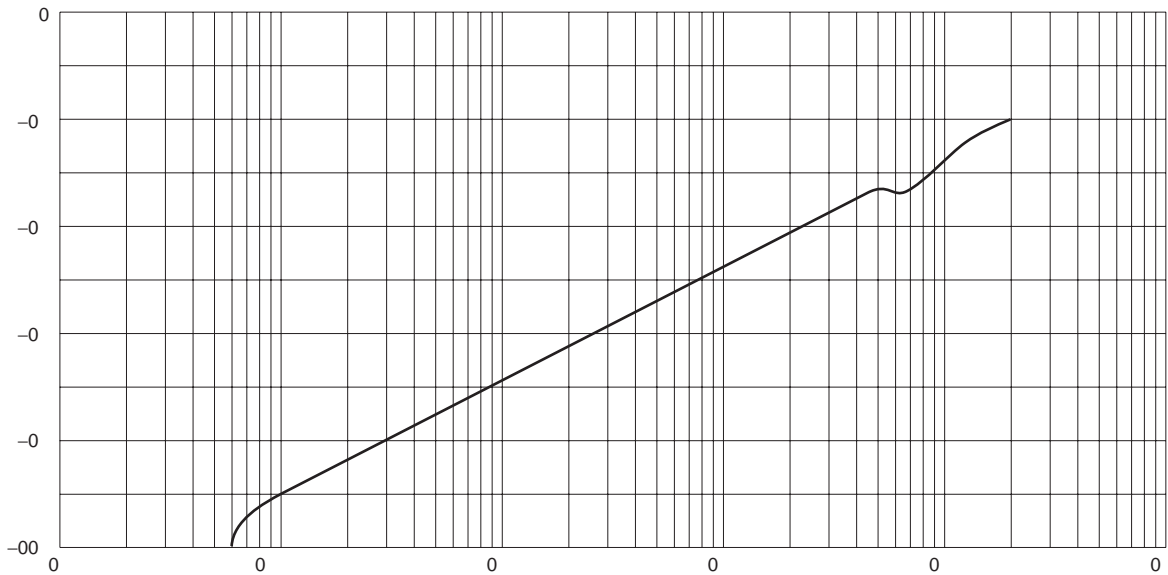
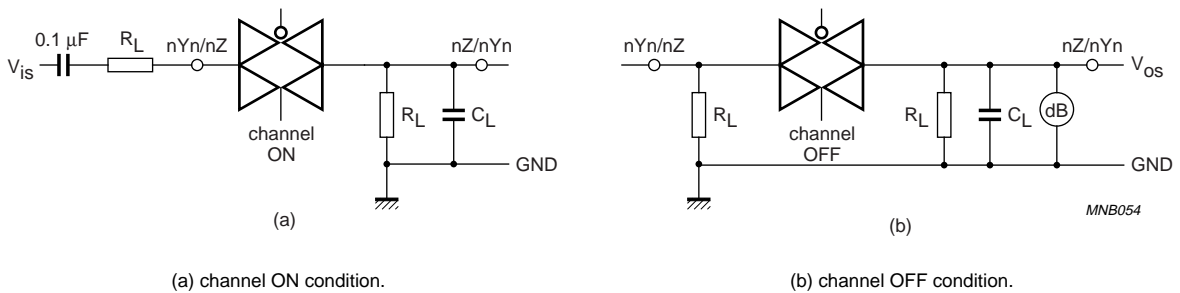


Fig.14 Test circuit for measuring switch OFF signal feed-through.



Test conditions:  $V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -4.5\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

Fig.15 Typical switch OFF signal feed-through as a function of frequency.



(a) channel ON condition.

(b) channel OFF condition.

Fig.16 Test circuits for measuring crosstalk between any two switches/multiplexers.

Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

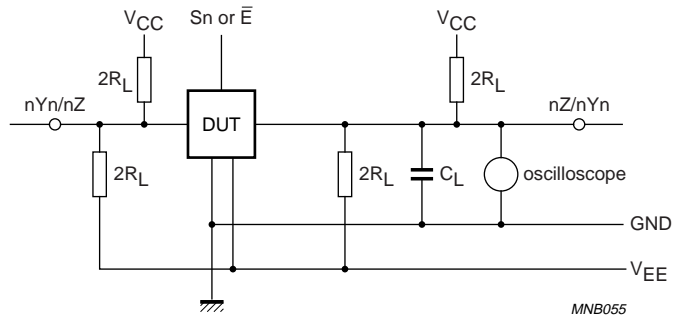
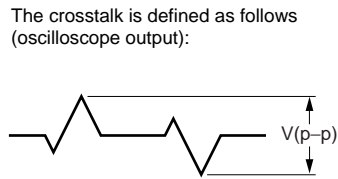
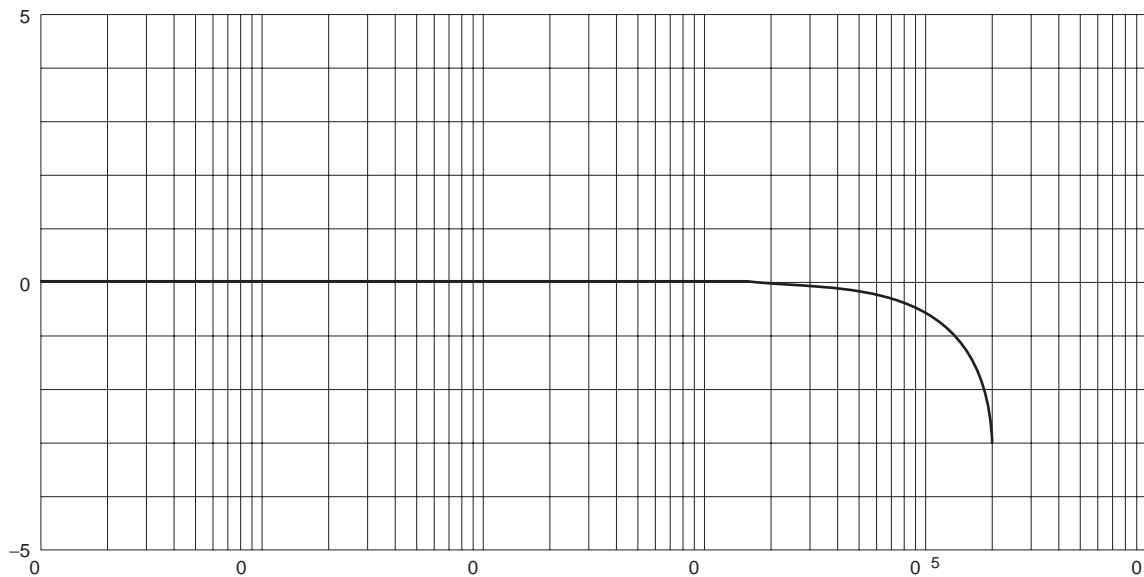


Fig.17 Test circuit for measuring crosstalk between control and any switch.



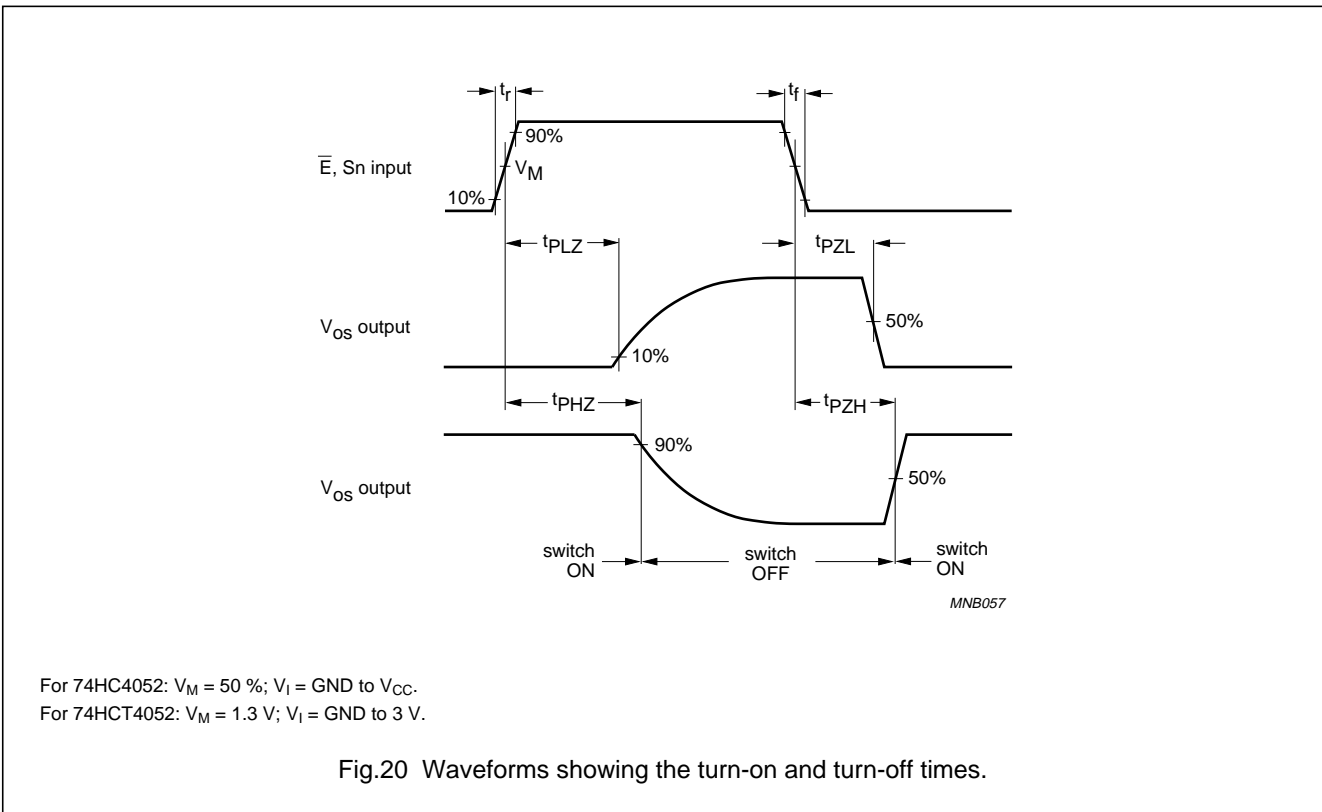
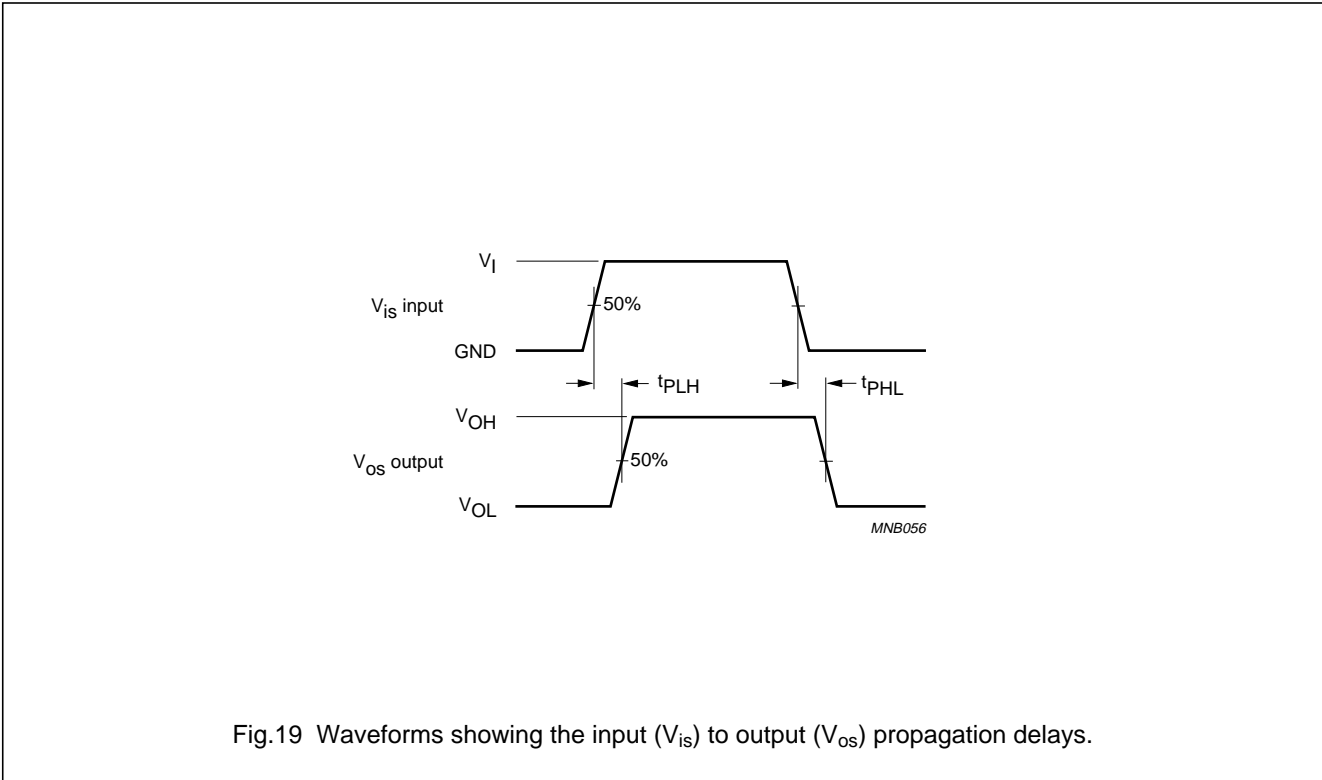
Test conditions:  $V_{CC} = 4.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $V_{EE} = -4.5\text{ V}$ ;  $R_L = 50\ \Omega$ ;  $R_{source} = 1\text{ k}\Omega$ .

Fig.18 Typical frequency response.

Dual 4-channel analog multiplexer, demultiplexer

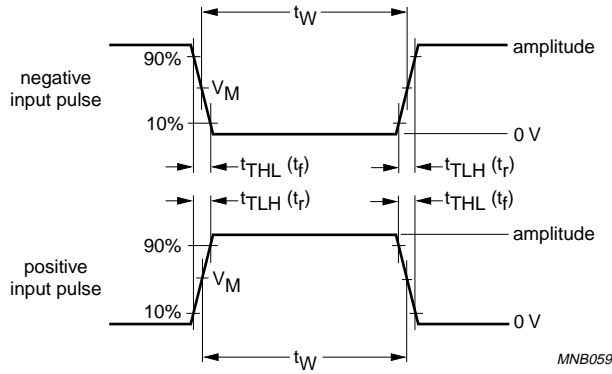
74HC4052; 74HCT4052

AC WAVEFORMS



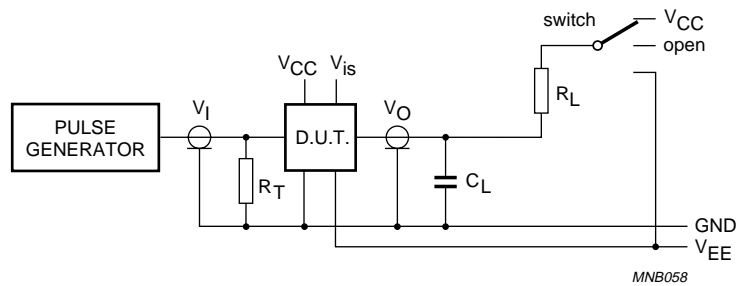
Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052



FAMILY	AMPLITUDE	$V_M$	$t_r$ and $t_f$	
			$f_{max}$ ; PULSE WIDTH	OTHER
74HC4052	$V_{CC}$	50 %	< 2 ns	6 ns
74HCT4052	3.0 V	1.3 V	< 2 ns	6 ns

Fig.21 Input pulse definitions.



TEST	SWITCH	$V_{is}$
$t_{PZH}$	$V_{EE}$	$V_{CC}$
$t_{PZL}$	$V_{CC}$	$V_{EE}$
$t_{PHZ}$	$V_{EE}$	$V_{CC}$
$t_{PLZ}$	$V_{CC}$	$V_{EE}$
other	open	pulse

Definitions for test circuit:

$R_L$  = load resistance

$C_L$  = load capacitance including jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_O$  of the pulse generator.

$t_r = t_f = 6$  ns; when measuring  $f_{max}$ , there is no constraint to  $t_r$  and  $t_f$  with 50 % duty factor.

Fig.22 Test circuit for measuring AC performance.

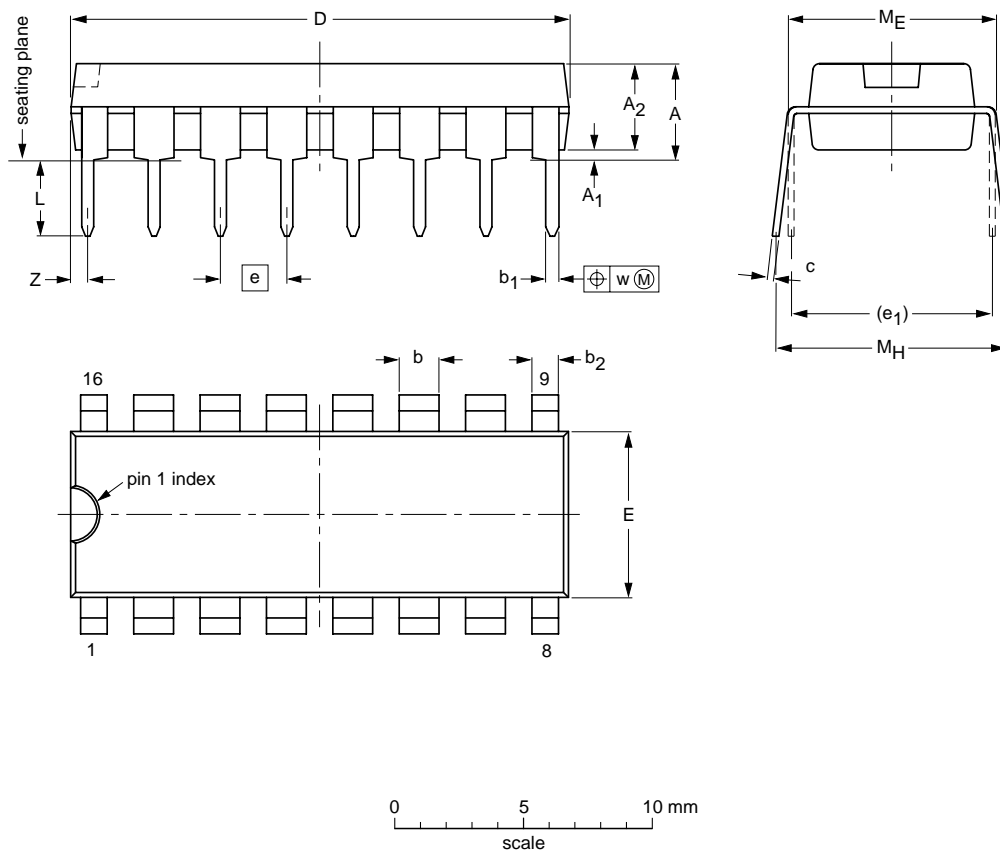
Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-9



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.32	0.38	3.56	1.65 1.40	0.51 0.41	1.14 0.76	0.36 0.20	19.3 18.8	6.45 6.24	2.54	7.62	3.81 2.92	8.23 7.62	9.40 8.38	0.254	0.76
inches	0.17	0.015	0.14	0.065 0.055	0.020 0.016	0.045 0.030	0.014 0.008	0.76 0.74	0.254 0.246	0.1	0.3	0.150 0.115	0.324 0.300	0.37 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

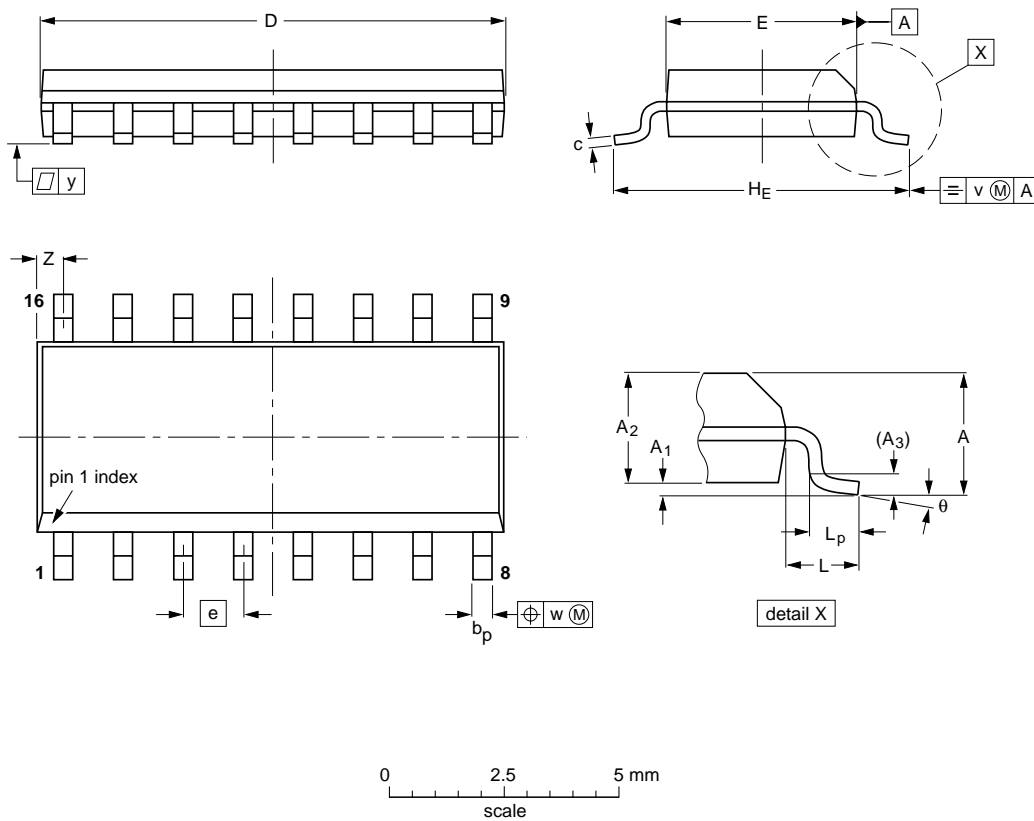
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT38-9					97-07-24 03-03-12

Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

SO16: plastic small outline package; 16 leads; body width 3.9 mm; body thickness 1.47 mm

SOT109-3



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.55 1.40	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.061 0.055	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

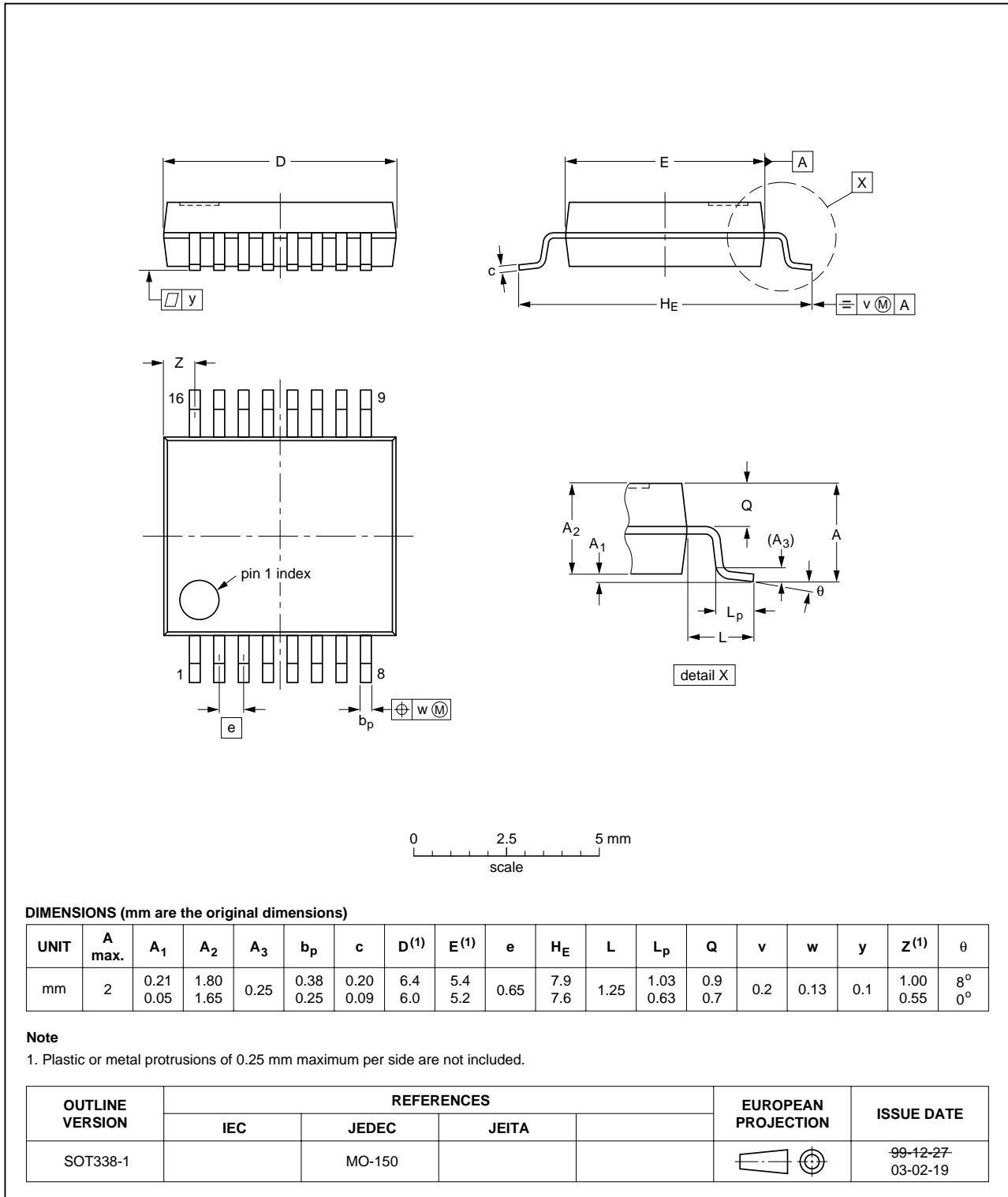
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-3		MS-012AC			98-12-23 03-02-19

Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

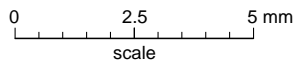
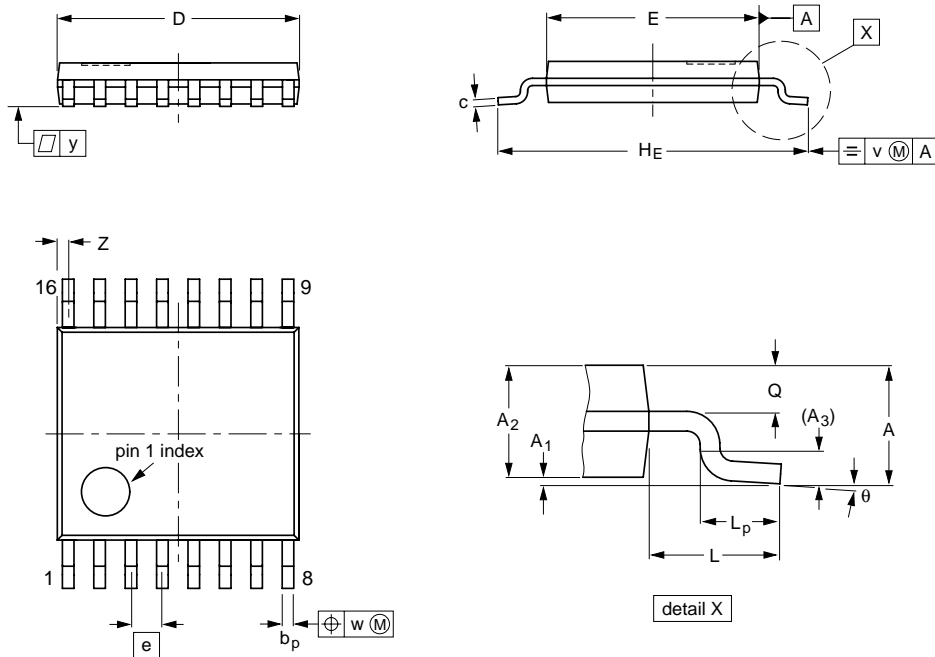


Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT403-1		MO-153			99-12-27 03-02-18

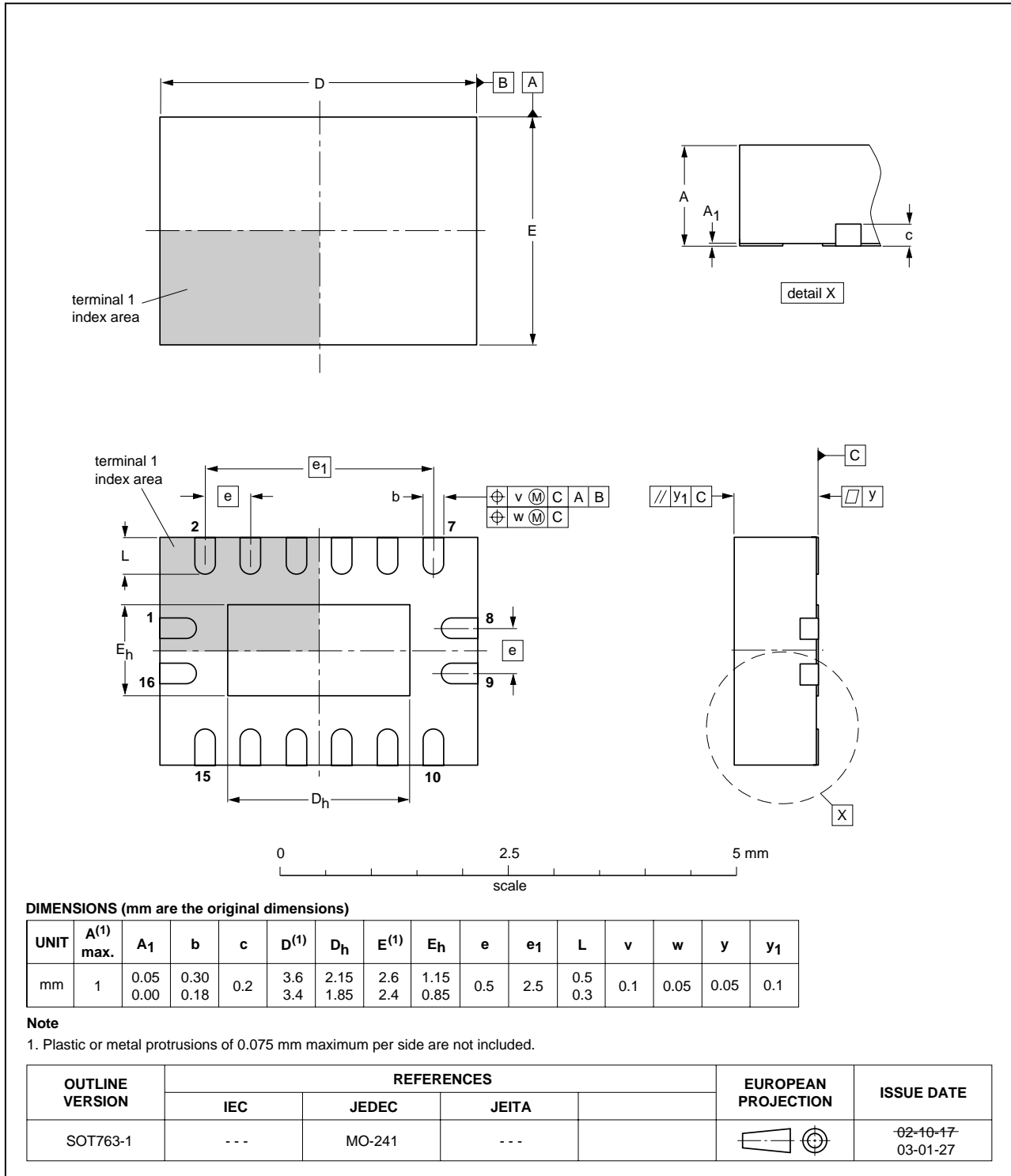


# Dual 4-channel analog multiplexer, demultiplexer

74HC4052; 74HCT4052

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm**

**SOT763-1**



Dual 4-channel analog multiplexer,  
demultiplexer

74HC4052; 74HCT4052

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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Printed in The Netherlands

R44/04/pp27

Date of release: 2004 Nov 11

Document order number: 9397 750 14189

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