Am2970

Dynamic Memory Timing Controller

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Provides complete timing control for 64K/256K memory systems which utilize the Am2968 Dynamic Memory Controller
- Supports extended cycle timing needed for byte-write operations
- Internal or external control of refresh
- Burst (up to 512-cycle), distributed, or hidden refresh
- Memory access/refresh request arbitration

GENERAL DESCRIPTION

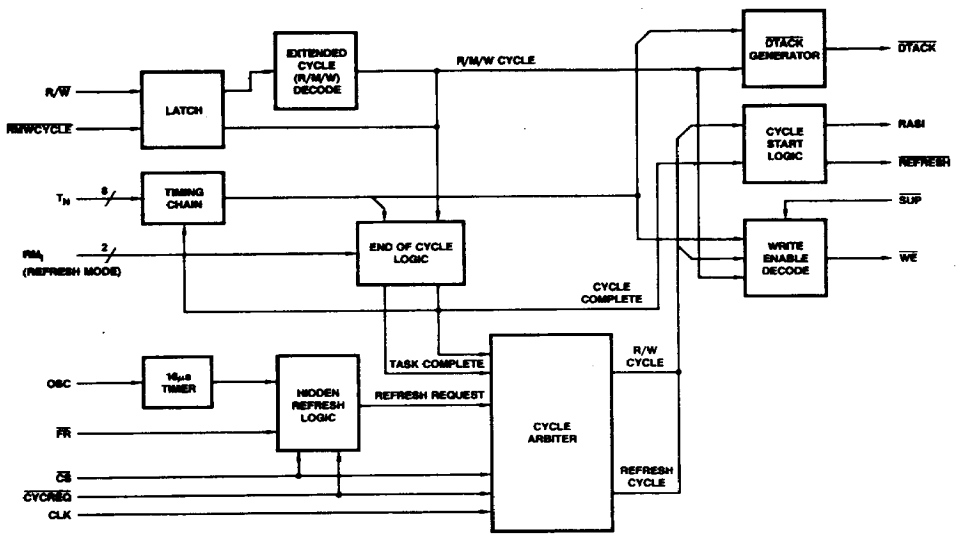
The Am2970 is a high-performance Memory Timing Controller (MTC). The Am2970 is designed to be used in memory systems which use the Am2968 Dynamic Memory Controller (DMC).

All of the control signals needed by the DMC are generated by the Am2970 MTC.

The Am2970 uses a delay-line to provide maximum flexibility to the memory system designer as well as allowing him to achieve maximum performance. The delay-line is the timing reference from which the MTC generates the control signals.

The Am2970 provides an internal refresh interval timer to generate refresh requests independent of the CPU. This guarantees proper refresh timing under all combinations of CPU and DMA requests.

BLOCK DIAGRAM

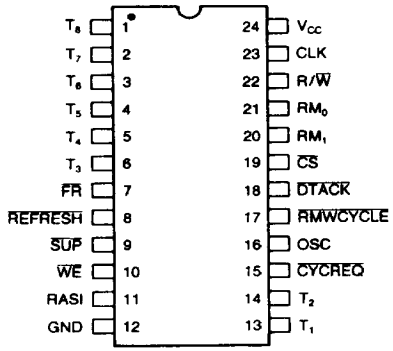


BD001131

RELATED PRODUCTS

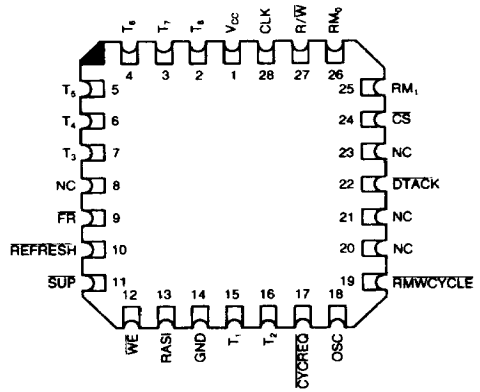
Part No.	Description
Am2968	Dynamic Memory Controller
Am2971	Programmable Event Generator

CONNECTION DIAGRAMS
Top View



CD009250

LCC*

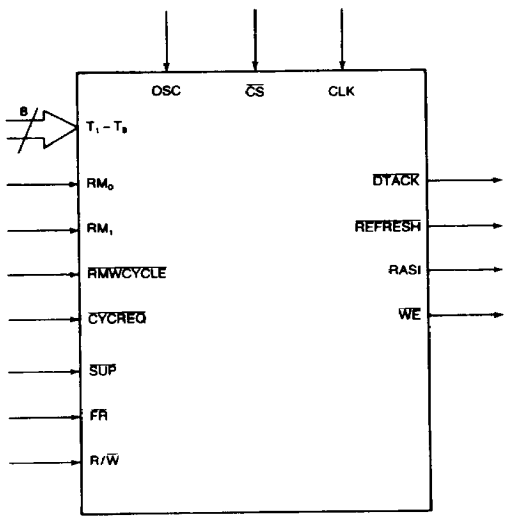


CD009261

* Same pinouts apply for PLCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002272

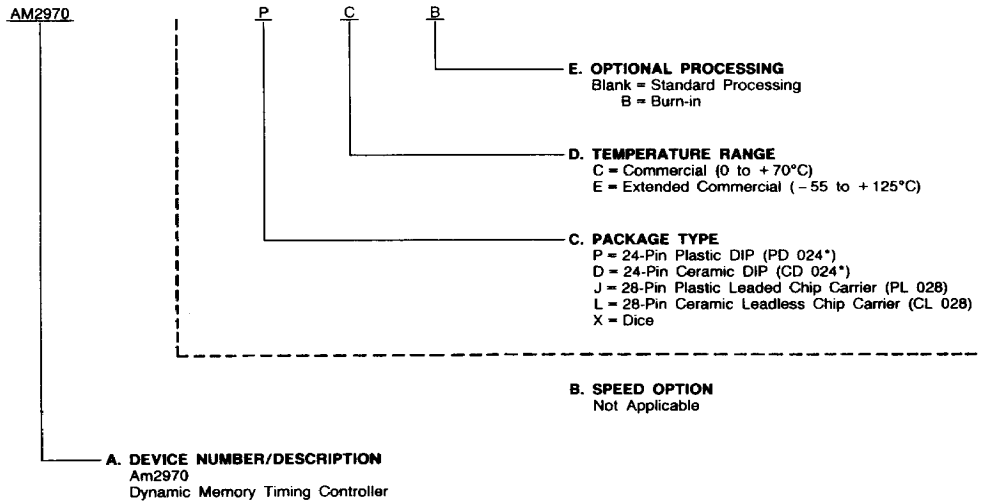
V_{CC} = Power Supply
GND = Ground

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2970	PC, PCB, DC, DCB, DE, DEB, JC, JCB, LC, XC

Valid Combinations

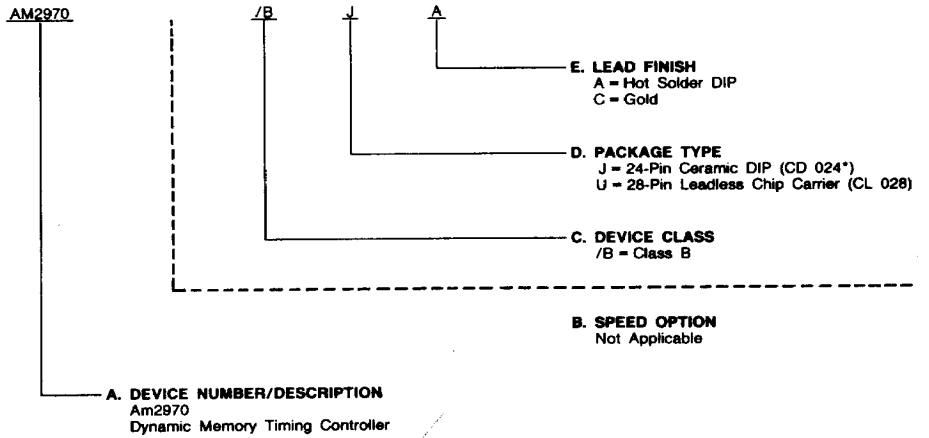
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

* Will also be available in slim (0.3") packages — To Be Announced.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2970	/BJA, /BUC

* Will also be available in a slim (0.3") package — To Be Announced.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$\overline{\text{RMWCYCLE}}$ Read/Modify/Write Cycle (Input)
This input indicates a byte operation is to be performed when HIGH, and a word operation when LOW. When $\overline{\text{RMWCYCLE}}$ is LOW, the Am2970 will provide an extended cycle so that a read-modify-write operation can be performed.

CLK Clock (Input)
For systems requiring synchronous arbitration of memory access and refresh requests, this input would receive the system clock. For asynchronous arbitration, this input must be tied HIGH.

$\overline{\text{CS}}$ Chip Select (Input)
When $\overline{\text{CS}}$ is LOW, the MTC is enabled. A memory read/write cycle can only be performed when $\overline{\text{CS}}$ is active, while refresh cycles occur independent of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is HIGH, all memory requests (HIGH-to-LOW transition of $\overline{\text{CYCREQ}}$) will be interpreted as refresh requests ("Hidden" refresh).

$\overline{\text{CYCREQ}}$ Cycle Request (Input)
When $\overline{\text{CS}}$ is LOW, this input will generate an internal memory request for the Am2970 on the HIGH-to-LOW transition of $\overline{\text{CYCREQ}}$.

$\overline{\text{DTACK}}$ Data Transfer Acknowledge (Output)
The HIGH-to-LOW transition of $\overline{\text{DTACK}}$ informs the CPU that a write cycle has begun, or that data will be on the system bus at the correct time during a read cycle.

$\overline{\text{FR}}$ Forced Refresh (Input)
This input is used to force a refresh cycle at user-designated times. The falling edge of $\overline{\text{FR}}$ latches an internal refresh request. If the memory is busy, the refresh is done at the completion of the current cycle.

$\overline{\text{REFRESH}}$ Refresh (Output)
This output should be connected to the MC_1 input of the Am2968. MC_0 of the Am2968 should be tied LOW. When MC_1 is HIGH, the Am2968 will perform a read/write cycle; when LOW, a refresh will be performed.

OSC Oscillator (Input)
This input signal is used to generate an internal refresh clock. It is this oscillator which initiates a refresh cycle if $\overline{\text{FR}}$ does not go active. The OSC signal may come from either external components (RC circuit) or a TTL-clock source.

$\overline{\text{RASI}}$ Row Address Strobe Input (Output)
This is connected to the RASI input of the Am2968 DMC. It is used to start a memory access for the DMC. The RASI output is also connected to the delay line to start the timing sequence. The rising edge of RASI initiates both actions.

RM_0, RM_1 Refresh Mode (Input)
These inputs control the type of refresh cycle the Am2970 is supposed to initiate. These modes are specified in Table 1.

R/$\overline{\text{W}}$ Read/Write (Input)
This input indicates a memory read request when HIGH, and a write request when LOW.

$\overline{\text{SUP}}$ Suppress (Input)
When $\overline{\text{SUP}}$ is driven LOW, it will inhibit access to memory by disabling $\overline{\text{WE}}$. It can be used to prevent illegal access in memory-access-protected systems.

T_1–T_8 Timing Taps (Inputs (8))
These inputs are the positive-edge triggered timing tap outputs from the timing reference (delay-line). They provide the necessary timing information for the Am2970 to control memory cycles. Definition of the eight timing taps is given in Table 2.

$\overline{\text{WE}}$ Write Enable (Output)
When $\overline{\text{WE}}$ is LOW, it causes data to be written into memory. $\overline{\text{WE}}$ is inhibited if $\overline{\text{SUP}}$ is LOW. This output can drive a 500-pF load.

V_{CC}, GND Power Pair
One each — V_{CC} and ground pins.

TABLE 1. REFRESH MODE SELECT TABLE

RM_1	RM_0	Refresh Mode
0	0	Not Burst (Distributed)
0	1	128-Cycle Burst
1	0	256-Cycle Burst
1	1	512-Cycle Burst

TABLE 2. TIMING TAP DEFINITION TABLE

Tap #	Function
1	Controls when $\overline{\text{DTACK}}$ will go active during read cycles.
2	Controls when $\overline{\text{DTACK}}$ will go active during read-modify-write cycles.
3	Identifies when data is available on the memory bus during write cycles.
4	Identifies when valid data is available on the memory bus during read-modify-write cycles.
5	Indicates that valid data is available from memory during read cycles.
6	Identifies when a new memory cycle may begin after a read or write cycle has been performed.
7	Controls when $\overline{\text{RAS}}$ outputs of DMC should go HIGH for read-modify-write cycles.
8	Identifies when a new memory cycle may begin after a read-modify-write cycle has been performed.

FUNCTIONAL DESCRIPTION

Architecture

The Am2970 MTC is designed to replace much of the MSI "glue" logic which is commonly necessary in controlling dynamic memory systems. It is responsible for controlling/arbitrating memory access and refresh, and handshaking with the processor. The Am2970 also provides an extended (Read/Modify/Write) cycle which is needed for byte operations.

Arbitration: Synchronous vs. Asynchronous

The Am2970 arbitrates between processor (read/write) and refresh requests for a memory cycle. If both the refresh and processor cycle are requested at the same time, the processor request is serviced first followed by the refresh request. It is possible for the arbiter to be either synchronous with the system clock, or asynchronous. Synchronous arbitration requires that the inputs requesting memory, $\overline{FR}$, and $\overline{CYCREQ}$, be clocked into the Am2970 by using the CLK input. In this mode, $\overline{CYCREQ}$ and $\overline{FR}$ are examined on the negative edge of CLK. When CLK is not used (tied HIGH), the Am2970 detects its absence and enters the asynchronous mode. In this mode the first memory request to occur will be serviced, but not until after an internal delay to avoid metastable states.

Refresh Operations

The Am2970 can support a variety of refresh schemes. The type of refresh is controlled via the RM_0, RM_1 inputs. Basic refresh types include distributed, as well as 128-, 256-, or 512-cycle burst.

The internal refresh request is controlled by the $\overline{FR}$ input, or the output of the internal oscillator as follows:

- In the burst mode of operation, the $\overline{FR}$ input is always the refresh clock.
- The $\overline{FR}$ input can also be used as the refresh clock in the distributed-refresh (non-burst) mode. However, the internal oscillator takes over as the refresh clock if it goes through three cycles without a LOW level appearing on the $\overline{FR}$ input. This provision allows the primary refresh clock ($\overline{FR}$) to be interrupted while it is in the HIGH logic state, and for refresh operations to be resumed at the internal-oscillator frequency.
- It is also possible to use the on-chip oscillator as the refresh clock in distributed-refresh mode. In this case, the $\overline{FR}$ input should be tied HIGH. However, since the on-chip oscillator is asynchronous to the external CLK input, it is necessary to provide a synchronous refresh clock via the $\overline{FR}$ input if synchronous arbitration is desired.

The Am2970 has the ability to increase memory bandwidth by inserting refresh requests when the processor is accessing other devices or performing I/O operations ($\overline{CYCREQ}$ = LOW, $\overline{CS}$ = HIGH). A hidden refresh can only be performed once every refresh-clock period, and occurs only with distributed refreshing. When a hidden refresh is performed, the Am2970 will skip the next refresh request. Figure 1 shows the timing involved to perform a hidden-refresh cycle.

Depending on the system configuration and operation, it is possible for the DRAM to appear "static," providing that a hidden refresh can be performed every refresh clock period.

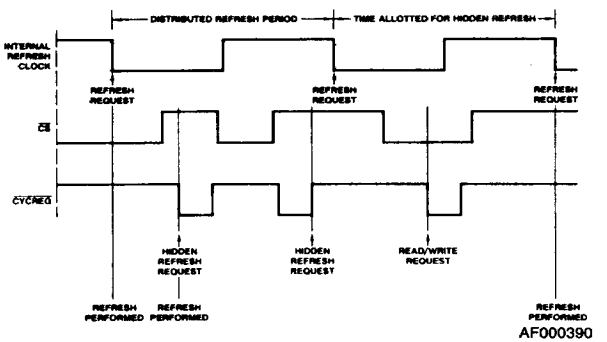


Figure 1. Hidden Refresh Cycle

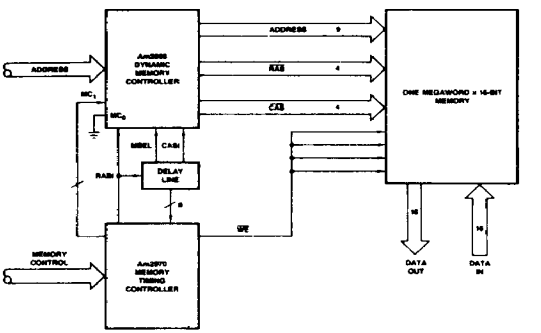


Figure 2. One Megaword Dynamic Memory System

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
DC Supply Voltage
to Ground Potential Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs for
HIGH Output State ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Output Current, Into Outputs ..... 30 mA
DC Input Current ..... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... 5.0 ±10%
Minimum ..... 4.50 V
Maximum ..... 5.50 V

Extended Commercial (E) and Military (M) Devices
Temperature
(T_A − E Devices) (T_C − M Devices) ... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5.0 ±10%
Minimum ..... 4.50 V
Maximum ..... 5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage on All Outputs Except $\overline{DTACK}$	V_{CC} = Min., I_{OH} = −1.0 mA	2.7		V
V_{OL}	Output LOW Voltage on All Outputs Except $\overline{WE}$	V_{CC} = Min., I_{OL} = 8 mA		0.5	V
	on $\overline{WE}$ Output	I_{OL} = 1 mA		0.5	
		I_{OL} = 12 mA		0.8	
V_{IH}	Input HIGH Voltage Except OSC	Guaranteed Input HIGH Voltage	2.0		V
V_{IL}	Input LOW Voltage Except OSC	Guaranteed Input LOW Voltage		0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA		−1.2	V
I_{IL}	Input LOW Current on $\overline{SUP}$, $\overline{CS}$ Inputs	V_{CC} = Max., V_{IN} = 0.5 V		−0.8	mA
	All Other Inputs Except OSC			−0.4	
I_{IH}	Input HIGH Current on $\overline{SUP}$ and $\overline{CS}$ Inputs	V_{CC} = Max., V_{IN} = 2.7 V		40	μA
	All Other Inputs Except OSC			20	
I_I	All Other Inputs Except OSC	V_{CC} = Max., V_{IN} = 5.5 V		100	μA
I_{SC}	Output Short-Circuit on All Outputs Except $\overline{DTACK}$	V_{CC} = Max., V_O = 0.0 V	−50	−200	mA
I_{CC}	Supply Current	V_{CC} = Max.		125	mA
I_{OX}	Output HIGH Current only on $\overline{DTACK}$ Output	V_{CC} = Min., V_{OH} = 5.5 V		250	μA

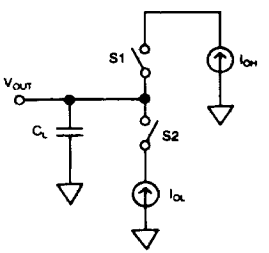
Notes: 1. V_{IH} and V_{IL} are tested for each input only once. Thereafter, hard HIGH and LOW levels are used for all other tests.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

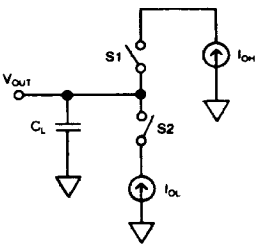
KS000010

SWITCHING TEST CIRCUITS



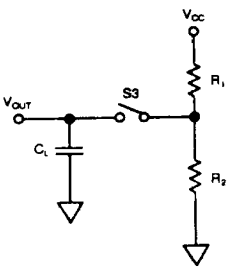
TC003131

A. RASI & $\overline{\text{REFRESH}}$ Outputs



TC003141

B. $\overline{\text{WE}}$ Output



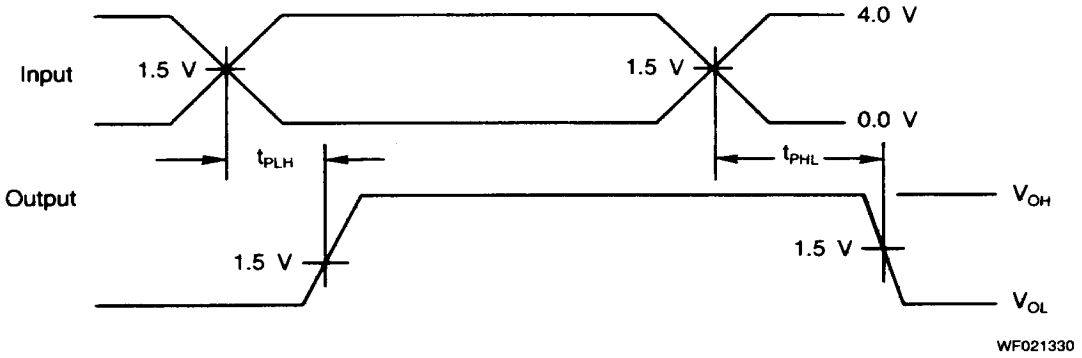
TC003151

C. $\overline{\text{DTACK}}$ Output (Open Collector)

TEST OUTPUT LOADS					
Test Circuit	R_1 (ohm)	R_2 (ohm)	C_L (pF)	I_{OH} (mA)	I_{OL} (mA)
A			50	−1	8
B			50, 150, 500	−1	12
C	680	1600	50		

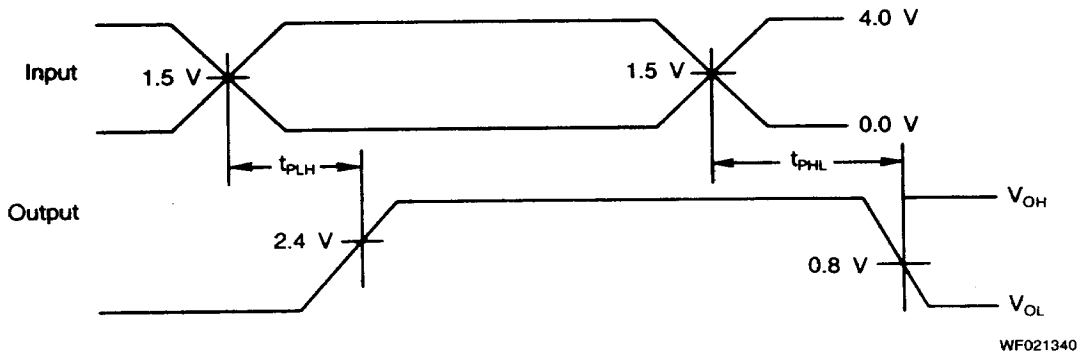
Notes: 1. C_L, the load capacitance, includes scope probe, wiring, and stray capacitance without the device in the test fixture.
2. S_1, S_2, and S_3 are open during all DC and functional testing.
3. During AC testing, switches are set as follows:
   1) S_3 is closed
   2) For V_{OUT} > 1.5 V, S_1 is closed and S_2 open
   3) For V_{OUT} < 1.5 V, S_1 is open and S_2 closed
4. $\overline{\text{DTACK}}$ Load:
   V_{CC} = 4.5, 5.0, and 5.5 V
   R_1 is selected to give I_{OL} (Max.) with V_{CC} = 5.5 V
   R_2 is selected to give V_{OUT} (DC) = 0.7 V_{CC} when the output $\overline{\text{DTACK}}$ is off

SWITCHING TEST WAVEFORMS



WF021330

RASI, $\overline{\text{REFRESH}}$, and $\overline{\text{DTACK}}$ Outputs



WF021340

$\overline{\text{WE}}$ Output

SWITCHING CHARACTERISTICS over operating range unless otherwise specified. (Note 1)

(Table continued on next page)

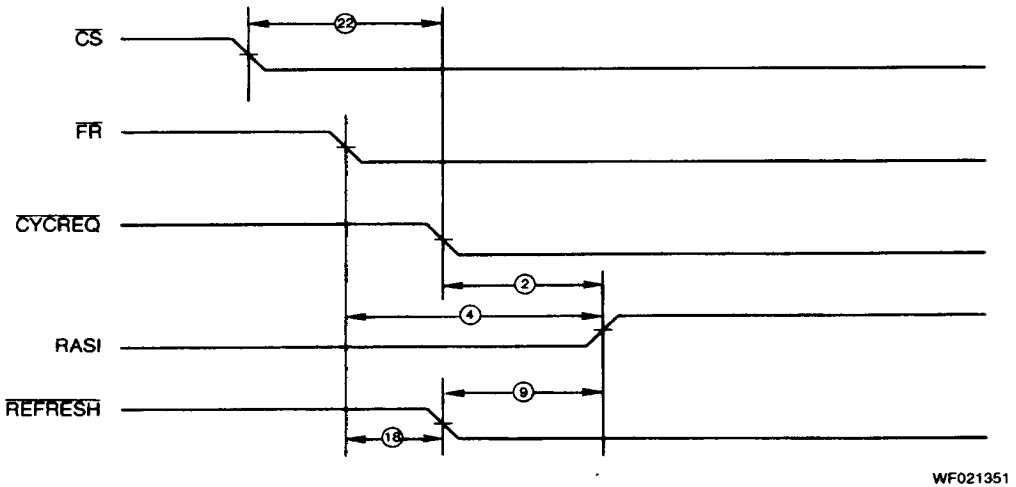
No.	Parameter Symbol	Parameter Description		Test Conditions		Min.	Max.	Units
		From	To					
1	t_{PLH}	CLK HIGH-to-LOW	RASI LOW-to-HIGH	Sync. Mode; Read/Write/Refresh			27	ns
2		$\overline{CYCREQ}$ HIGH-to-LOW		Async. Mode; Read/Write			36	
3				Hidden Refresh; ($\overline{CS}$ = 1)			50	
4		$\overline{FR}$ HIGH-to-LOW		Async. Mode; Refresh Cycles Only			55	
5		T_6 LOW-to-HIGH		Back-to-Back Cycles or Burst Refresh ($\overline{RMWCYCLE}$ = 1)			42	
6		T_8 LOW-to-HIGH		Back-to-Back Cycles or Burst Refresh ($\overline{RMWCYCLE}$ = 0)			43	
7	t_{PHL}	T_5 LOW-to-HIGH	RASI HIGH-to-LOW	All Modes ($\overline{RMWCYCLE}$ = 1)			26	ns
8		T_7 LOW-to-HIGH		All Modes ($\overline{RMWCYCLE}$ = 0)			27	
9	t_{SKEW}	$\overline{REFRESH}$ HIGH-to-LOW	RASI LOW-to-HIGH	Async./Arbitration Refresh Modes		0	12	ns
10	t_{PHL}	T_1 LOW-to-HIGH	$\overline{DTACK}$ HIGH-to-LOW	Read/Write Operations ($\overline{RMWCYCLE}$ = 1)			30	ns
11		T_2 LOW-to-HIGH		Read/Write Operations ($\overline{RMWCYCLE}$ = 0)			30	
12	t_{PLH}	$\overline{CYCREQ}$ LOW-to-HIGH	$\overline{DTACK}$ LOW-to-HIGH	Read/Write Operations			35	ns
13	t_{PHL}	T_3 LOW-to-HIGH	$\overline{WE}$ HIGH-to-LOW	Write Operation ($\overline{RMWCYCLE}$ = 1)	C_L = 50 pF		20	ns
					C_L = 150 pF		30	
					C_L = 500 pF		50	
14		T_4 LOW-to-HIGH		Write Operation ($\overline{RMWCYCLE}$ = 0)	C_L = 50 pF		20	
					C_L = 150 pF		30	
					C_L = 500 pF		50	
15	t_{PLH}	T_5 LOW-to-HIGH	$\overline{WE}$ LOW-to-HIGH	Write Operation ($\overline{RMWCYCLE}$ = 1)	C_L = 50 pF		35	ns
					C_L = 150 pF		45	
					C_L = 500 pF		65	
16		T_7 LOW-to-HIGH		Write Operation ($\overline{RMWCYCLE}$ = 0)	C_L = 50 pF		38	
					C_L = 150 pF		48	
					C_L = 500 pF		68	
17	t_{PHL}	$\overline{CYCREQ}$ HIGH-to-LOW	$\overline{REFRESH}$ HIGH-to-LOW	Hidden Refresh ($\overline{CS}$ = 1)			45	ns
18		$\overline{FR}$ HIGH-to-LOW		All Refresh Modes			50	
19	t_{PLH}	$\overline{CYCREQ}$ HIGH-to-LOW	$\overline{REFRESH}$ LOW-to-HIGH	Synchronous Arbitration			30	ns
20		T_6 LOW-to-HIGH		Distributive Refresh or End-of-Burst Refresh ($\overline{RMWCYCLE}$ = 1)			31	
21		T_8 LOW-to-HIGH		Distributive Refresh or End-of-Burst Refresh ($\overline{RMWCYCLE}$ = 0)			31	
22	t_{SET}	$\overline{CS}$ HIGH-to-LOW	$\overline{CYCREQ}$ HIGH-to-LOW	Hidden Refresh, Read/Write		6		ns
23	t_{SET}	$\overline{CYCREQ}$ HIGH-to-LOW	CLK HIGH-to-LOW	Sync. Mode; Read/Write		15		
24	t_{SET}	$\overline{FR}$ HIGH-to-LOW		Sync. Mode; Refresh		35		
25	t_{SET}	R/$\overline{W}$ (1 or 0)	T_3 LOW-to-HIGH	All Modes		6		ns
26	t_{HOLD}					10		
27	* t_{SET}	$\overline{SUP}$ (1 or 0)	T_3 LOW-to-HIGH	($\overline{RMWCYCLE}$ = 1)		5		ns
28	t_{SET}	$\overline{SUP}$ (1 or 0)	T_4 LOW-to-HIGH	($\overline{RMWCYCLE}$ = 0)		5		ns

SWITCHING CHARACTERISTICS

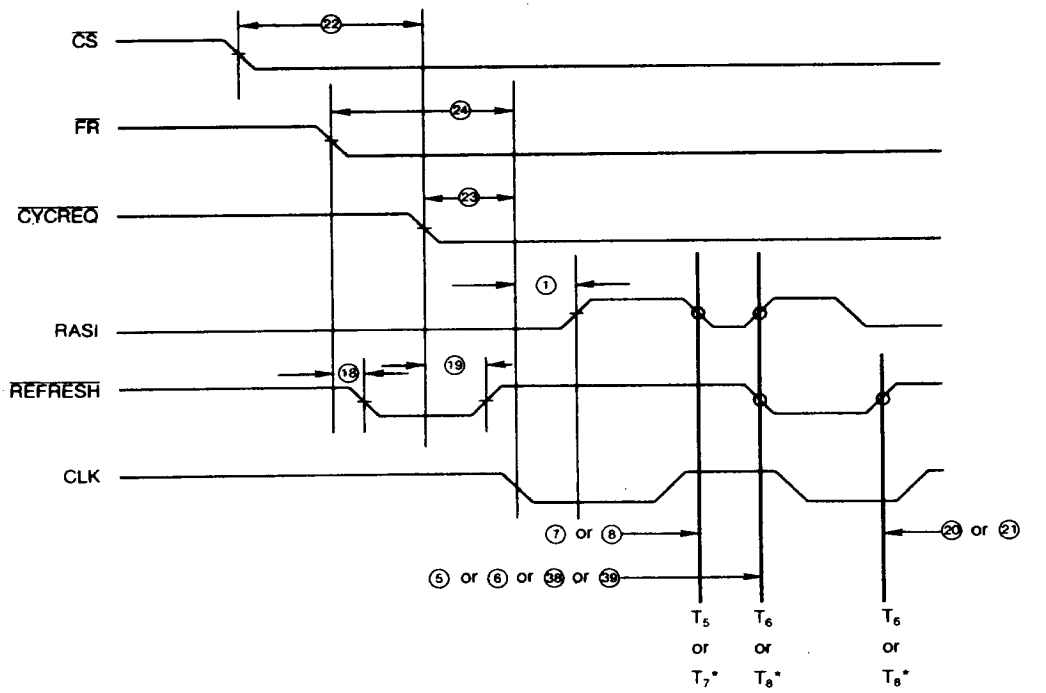
No.	Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
		From	To				
29	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T_5 LOW-to-HIGH	($\overline{RMWCYCLE}$ = 1)	30		ns
30	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T_7 LOW-to-HIGH	($\overline{RMWCYCLE}$ = 0)	32		ns
31	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T_1 LOW-to-HIGH		10		ns
32	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T_2 LOW-to-HIGH		15		ns
33	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T_3 LOW-to-HIGH		10		ns
34	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T_4 LOW-to-HIGH		10		ns
35	t_{HOLD}	$\overline{RMWCYCLE}$ (1 or 0)	T_5 LOW-to-HIGH		25		ns
36	t_{HOLD}	$\overline{RMWCYCLE}$ (1 or 0)	T_7 LOW-to-HIGH		25		ns
37	t_{PW}	$T_1 - T_8$	$T_1 - T_8$	All Cycles	10		ns
38	t_{PHL}	T_7 LOW-to-HIGH	$\overline{REFRESH}$ HIGH-to-LOW	Synchronous Arbitration ($\overline{RMWCYCLE}$ = 1)		37	ns
39		T_8 LOW-to-HIGH		Synchronous Arbitration ($\overline{RMWCYCLE}$ = 0)		37	

Notes: 1. Testing for parameters that apply for multiple cycles and/or modes is performed in one cycle or mode only. Not more than one output should be shorted at a time. Duration of short not to exceed one second.

SWITCHING WAVEFORMS (Cont'd.)



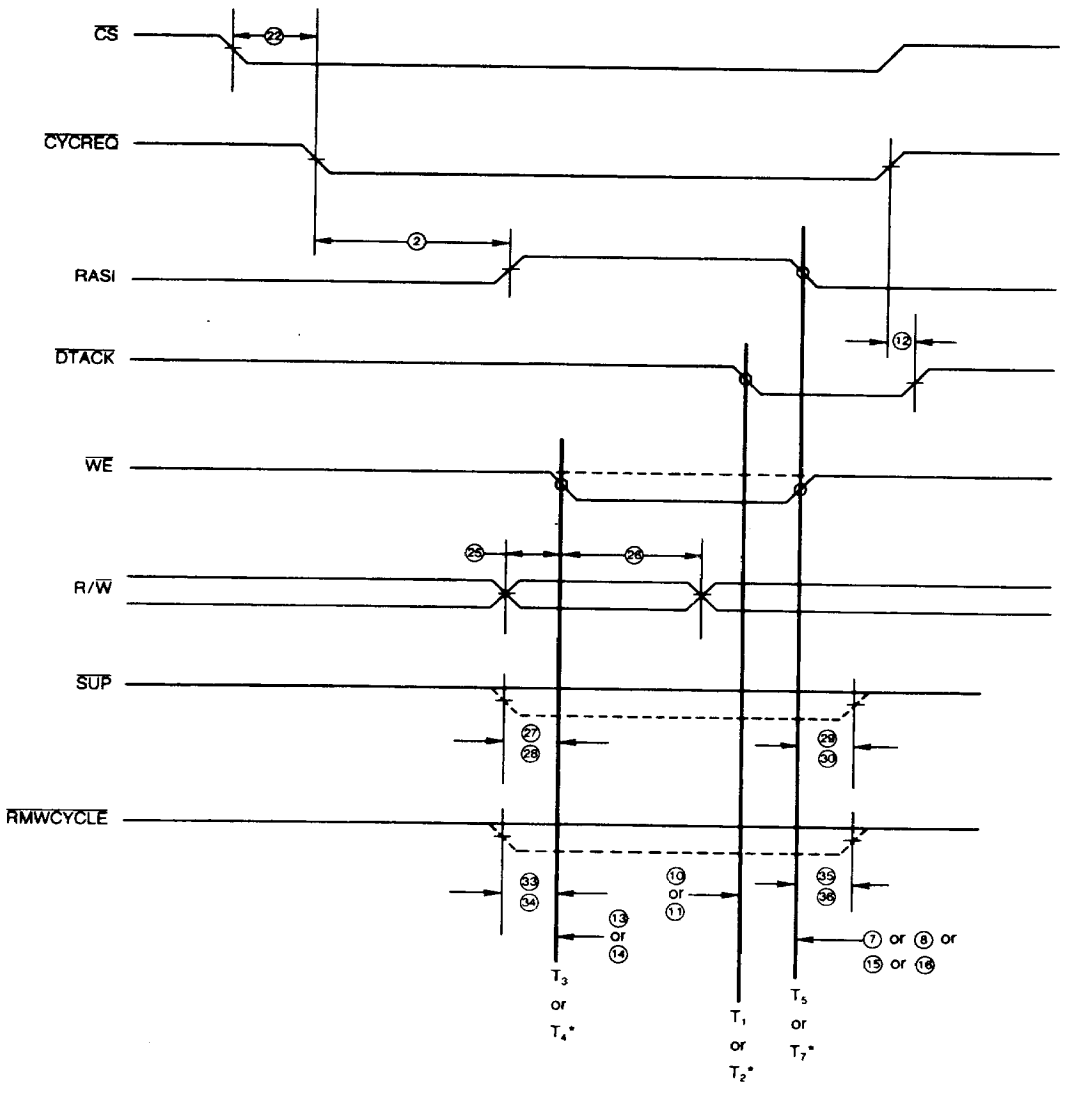
Asynchronous Arbitration



* Active when $\overline{RMWCYCLE} = 0$

Synchronous Arbitration

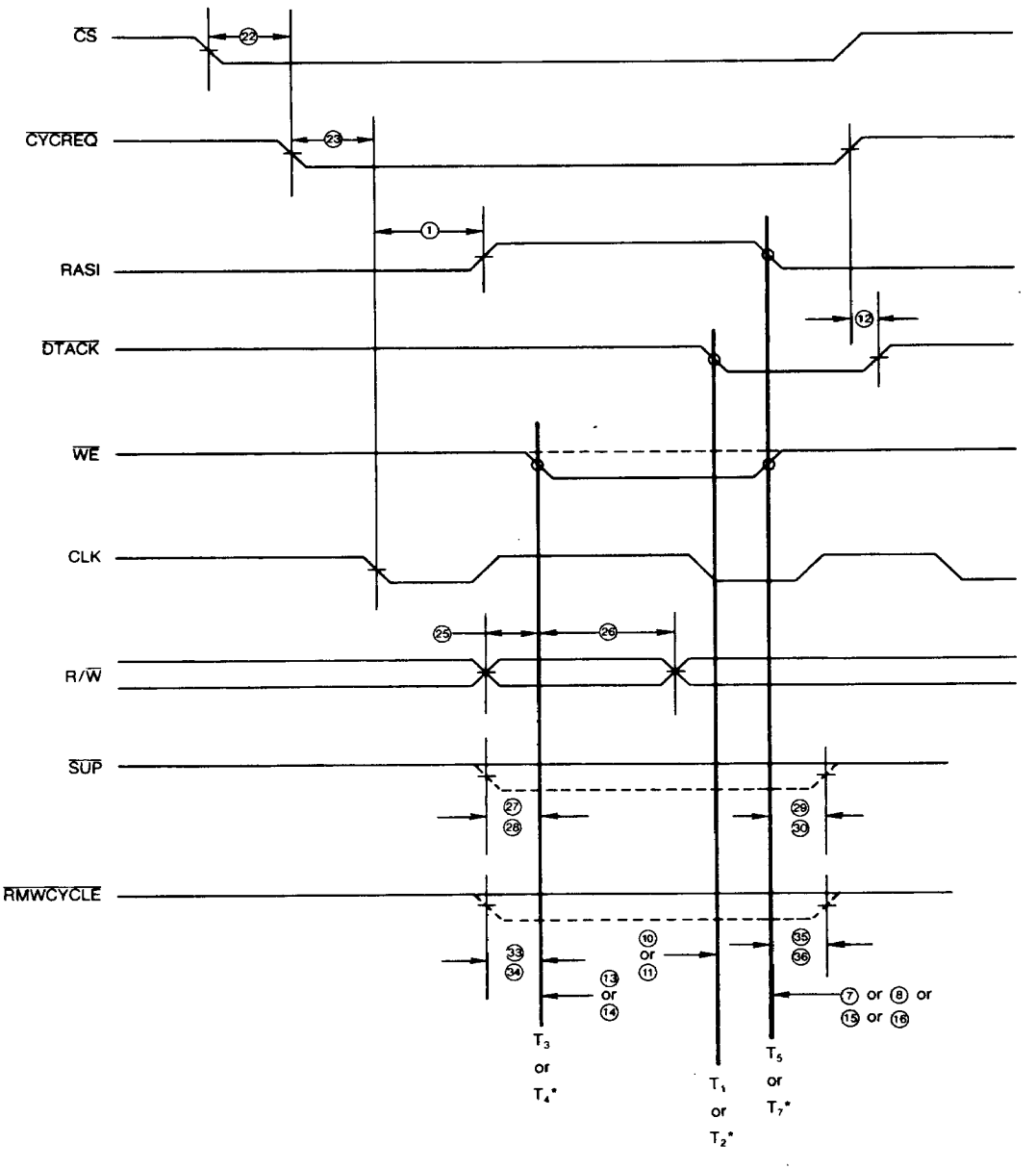
SWITCHING WAVEFORMS (Cont'd.)



* Active when $\overline{\text{RMWCYCLE}}$ = 0

Asynchronous Read/$\overline{\text{Write}}$
(With Read/Modify/Write)

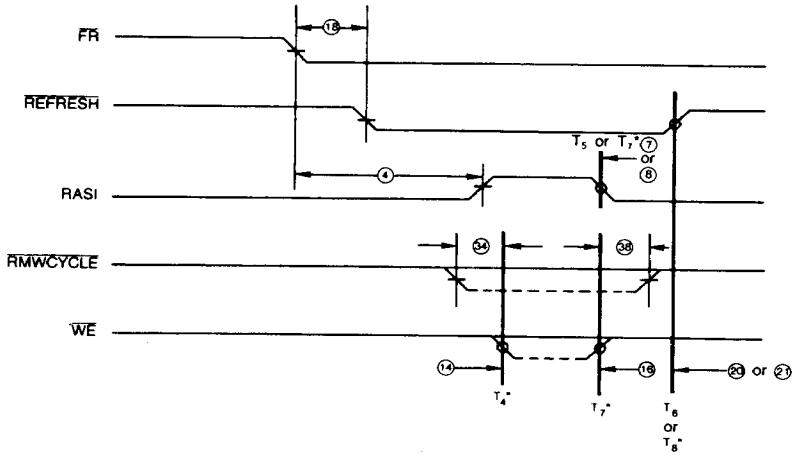
SWITCHING WAVEFORMS (Cont'd.)



* Active when $\overline{\text{RMWCYCLE}}$ = 0

Synchronous Read/$\overline{\text{Write}}$ (With Read/Modify/Write)

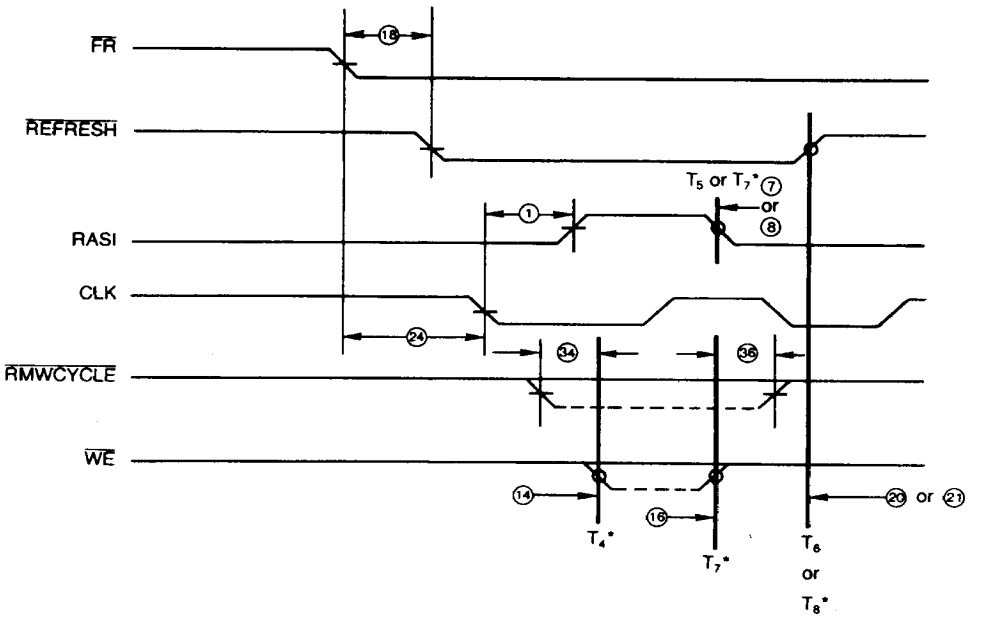
SWITCHING WAVEFORMS (Cont'd.)



WF021391

* Active when $\overline{\text{RMWCYCLE}} = 0$

Asynchronous Refresh (Shown with Read/Modify/Write)

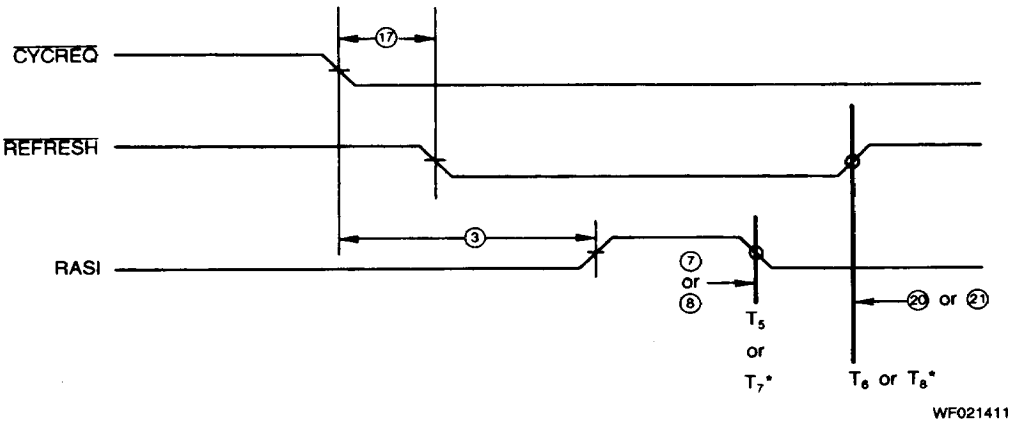


WF021401

* Active when $\overline{\text{RMWCYCLE}} = 0$

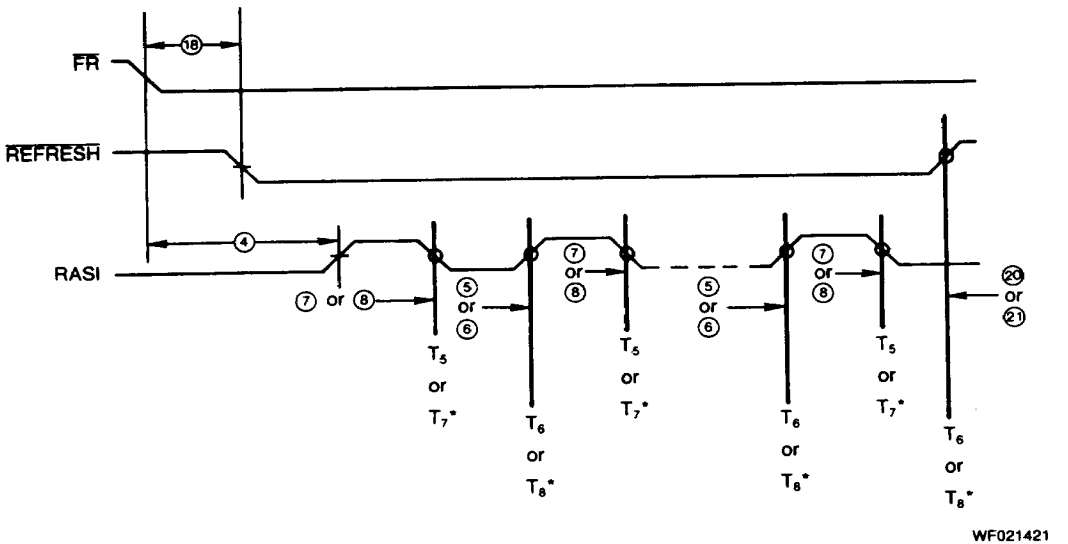
Synchronous Refresh (Shown with Read/Modify/Write)

SWITCHING WAVEFORMS



* Active when $\overline{RMWCYCLE} = 0$

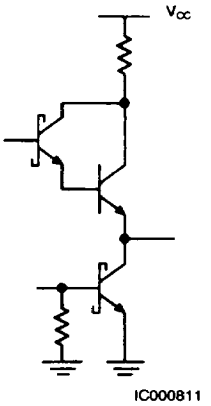
Hidden Refresh



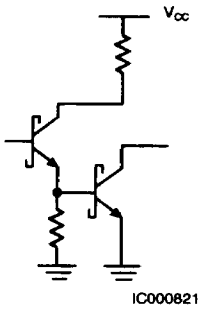
* Active when $\overline{RMWCYCLE} = 0$

Burst Refresh

INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS (Cont'd.)

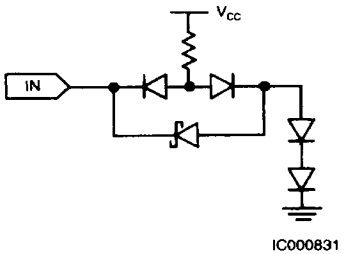


Typical Output

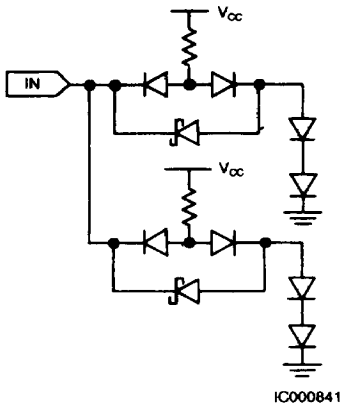


$\overline{\text{DTACK}}$ Output

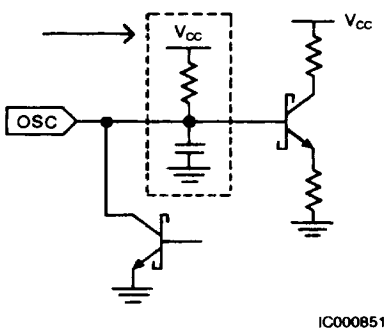
INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS



Typical Input



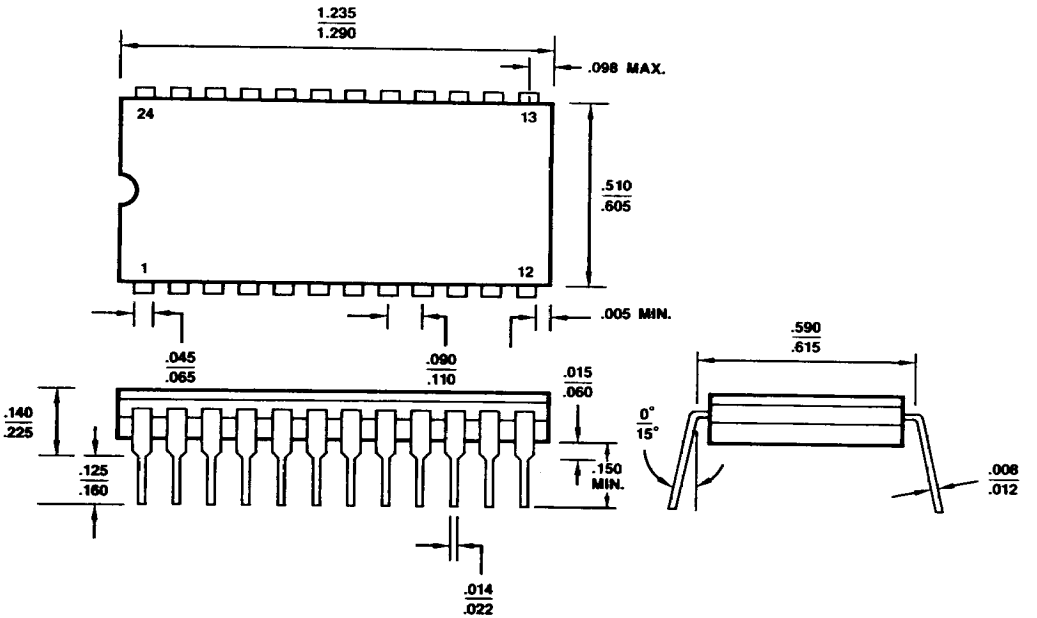
T_1, T_2, R/$\overline{W}$, $\overline{SUP}$, $\overline{CS}$ Inputs



OSC Input

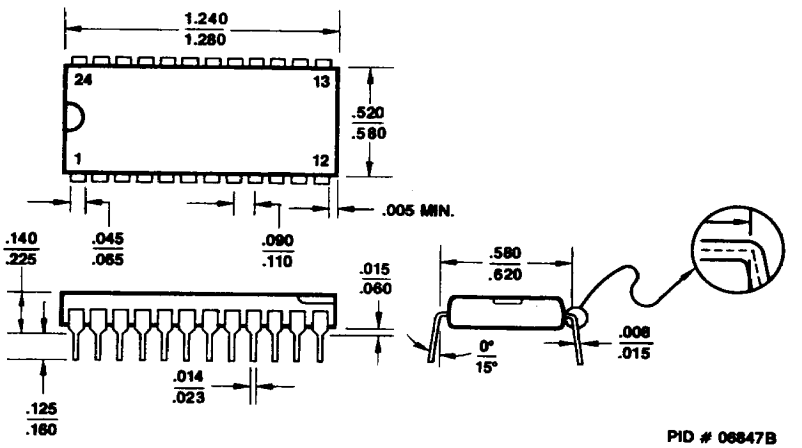
PHYSICAL DIMENSIONS (Cont'd.)

CD 024*



PID # 07156A

PD 024*

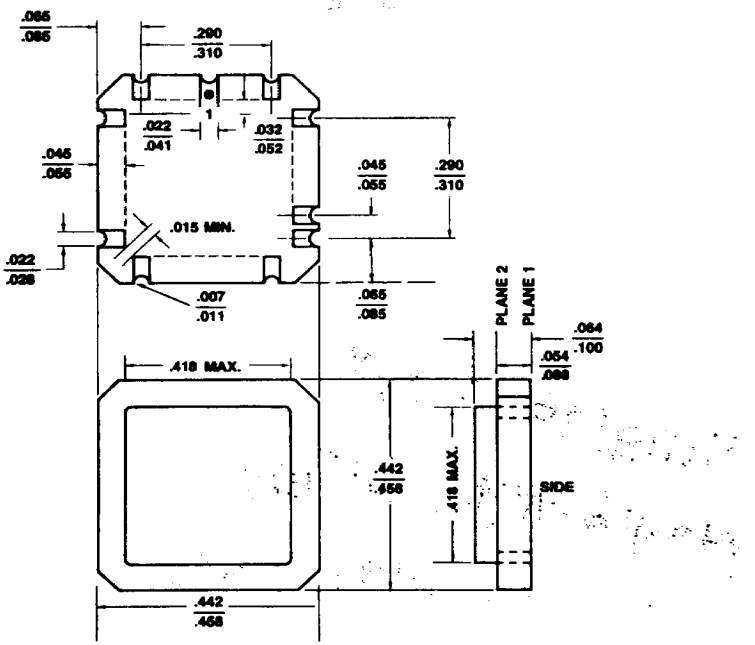


PID # 06847B

* Will also be available in slim (0.3") packages — To Be Announced.

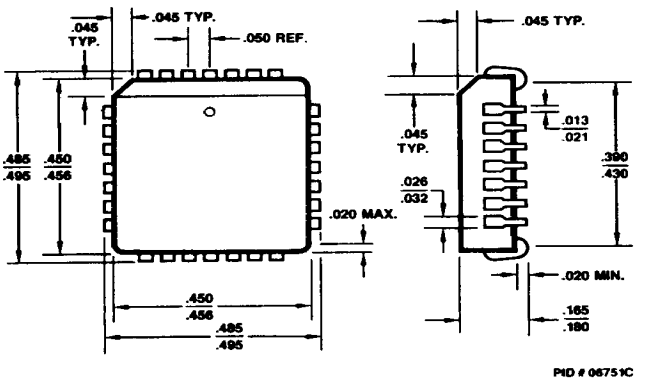
PHYSICAL DIMENSIONS

CL 028



PID # 06595C

PL 028



PID # 06751C

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