CAT29F150

1.5 Megabit CMOS 5V Only Sector Flash Memory

FEATURES

- **Fast Read Access Time: 90/120/150 ns**
- **Sectored Architecture:**
  - **One 16-KB Boot Sector**
    - **Top or Bottom Locations**
  - **Two 8-KB Sectors**
  - **One 32-KB Sector**
  - **Two 64-KB Sectors**
- **Hardware Data Protection**
- **Automatic Program and Erase Algorithms**
- **Commercial, Industrial and Automotive Temperature Ranges**
- **5V±10% Programming, Reading and Erase Voltage**
- **Electronic Signature**

- **100,000 Program/Erase Cycles and 10 Year Data Retention**
- **End of Write Detection**
  - **Toggle Bit**
  - **$\overline{\text{DATA}}$ Polling**
- **Standard Pinouts:**
  - **32-pin PLCC**
  - **32-pin TSOP**
- **Low Power CMOS Dissipation**
  - **Active Read: 30mA max.**
  - **Programming/Erase: 60mA max.**
  - **Standby: 1μA max.**
- **Hardware $\overline{\text{RESET}}$ Pin**

DESCRIPTION

The CAT29F150 is a high speed 192K X 8 electrically erasable and reprogrammable 5V only Flash memory ideally suited for applications requiring in-system or after sale code updates.
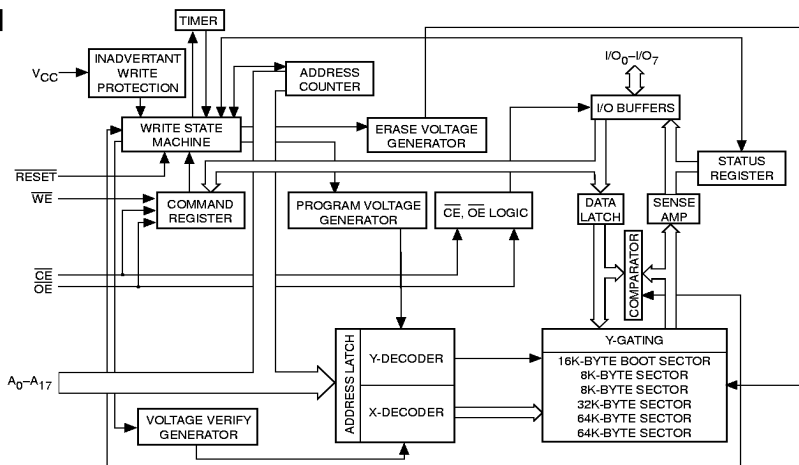
The CAT29F150 has a sectored architecture with one 16 KB Boot sector, two 8 KB sectors, one 32 KB sector and two 64 KB sectors. The Boot sector can be at the top or bottom of the memory map. All six sectors include a lock out feature against program and erase operations to guarantee data integrity.

The CAT29F150 is designed with a signature mode which allows the user to identify the IC manufacturer and device type. The CAT29F150 is also designed with on-chip Address Latches, Data Latches, Programming and Erase Algorithms. DATA polling and Toggle status bits signal the start and end of the self time write cycle. Additionally, the CAT29F150 features a $\overline{\text{RESET}}$ pin, which when set LOW will abort the program or erase operations.
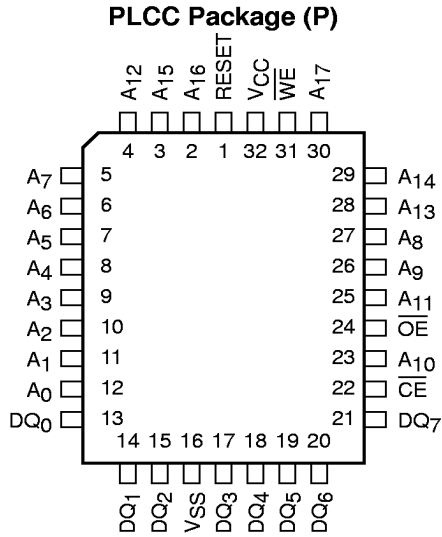
The CAT29F150 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin TSOP and PLCC packages.
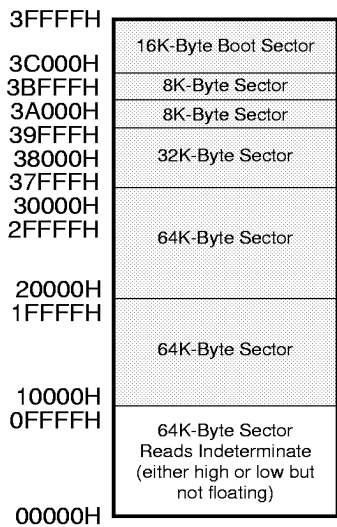
BLOCK DIAGRAM

29F150 F01

PIN CONFIGURATION

PLCC Package (P)

Top pins (left to right): A_{12}, A_{15}, A_{16}, $\overline{RESET}$, V_{CC}, $\overline{WE}$, A_{17} (pins 4 3 2 1 32 31 30)

Left side (top to bottom):
A_7	5
A_6	6
A_5	7
A_4	8
A_3	9
A_2	10
A_1	11
A_0	12
DQ_0	13

Right side (top to bottom):
29	A_{14}
28	A_{13}
27	A_8
26	A_9
25	A_{11}
24	$\overline{OE}$
23	A_{10}
22	$\overline{CE}$
21	DQ_7

Bottom pins (pins 14 15 16 17 18 19 20): DQ_1, DQ_2, V_{SS}, DQ_3, DQ_4, DQ_5, DQ_6

PIN FUNCTIONS

Pin Name	Type	Function
A_0–A_{17}	I/P	Address inputs for memory addressing
I/O_0–I/O_7	I/O	Data Input/Output
$\overline{CE}$	Input	Chip Enable
$\overline{OE}$	Input	Output Enable
$\overline{WE}$	Input	Write Enable
$\overline{RESET}$	Input	Reset
V_{CC}		Voltage Supply
V_{SS}		Ground

TSOP Package (T)

Left side (top to bottom, pins 1–16):
A_{11}	1
A_9	2
A_8	3
A_{13}	4
A_{14}	5
A_{17}	6
$\overline{WE}$	7
V_{CC}	8
$\overline{RESET}$	9
A_{16}	10
A_{15}	11
A_{12}	12
A_7	13
A_6	14
A_5	15
A_4	16

Right side (top to bottom, pins 32–17):
32	$\overline{OE}$
31	A_{10}
30	$\overline{CE}$
29	I/O_7
28	DQ_6
27	DQ_5
26	DQ_4
25	DQ_3
24	V_{SS}
23	DQ_2
22	DQ_1
21	DQ_0
20	A_0
19	A_1
18	A_2
17	A_3

MEMORY MAP

CAT29F150T

Address	Sector
3FFFFH – 3C000H	16K-Byte Boot Sector
3BFFFH – 3A000H	8K-Byte Sector
39FFFH – 38000H	8K-Byte Sector
37FFFH – 30000H	32K-Byte Sector
2FFFFH – 20000H	64K-Byte Sector
1FFFFH – 10000H	64K-Byte Sector
0FFFFH – 00000H	64K-Byte Sector Reads Indeterminate (either high or low but not floating)

CAT29F150B

Address	Sector
3FFFFH – 30000H	64K-Byte Main Block Reads Indeterminate (either high or low but not floating)
2FFFFH – 20000H	64K-Byte Sector
1FFFFH – 10000H	64K-Byte Sector
0FFFFH – 08000H	32K-Byte Sector
07FFFH – 06000H	8K-Byte Sector
05FFFH – 04000H	8K-Byte Sector
03FFFH – 00000H	16K-Byte Boot Sector

29F150 F02

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −55°C to +95°C

Storage Temperature .... −65°C to +150°C

Voltage on Any Pin with
Respect to Ground[1] .... −2.0V to +V_{CC} + 2.0V
(except A9, $\overline{OE}$ and $\overline{RESET}$)

Voltage on Pin A_9, $\overline{OE}$ and $\overline{RESET}$ with
Respect to Ground .... −2.0V to +14.0V

V_{CC} with Respect to Ground[1] .... −2.0V to +7.0V

Package Power Dissipation
Capability (T_A = 25°C) .... 1.0 W

Lead Soldering Temperature (10 secs) .... 300°C

Output Short Circuit Current[2] .... 200 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Method
N_{END}[3]	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}[3]	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V_{ZAP}[3]	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}[3][4]	Latch-Up	100		mA	JEDEC Standard 17

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C_{IN}[3]	Input Pin Capacitance		8	pF	V_{IN} = 0V
C_{OUT}[3]	Output Pin Capacitance		12	pF	V_{OUT} = 0V
C_{IN2}[3]	Control Pin Capacitance		9	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} +1V.
(5) The minimum DC Input Voltage on pins A_9, $\overline{OE}$ and $\overline{RESET}$ is -0.5V. During voltage transitions, A_9, $\overline{OE}$ and $\overline{RESET}$ may undershoot to -2.0V for periods of less than 20ns. Maximum DC input on A_9 is 12.5V which may overshoot to 14.0V for periods up to 20ns.

D.C. OPERATING CHARACTERISTICS

V_{CC} = +5V ±10%, unless otherwise specified

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{LI}	Input Leakage Current		±1.0	µA	V_{IN} = V_{CC} or V_{SS} V_{CC} = 5.5V
I_{LO}	Output Leakage Current		±1	µA	V_{OUT} = V_{CC} or V_{SS}, V_{CC} = 5.5V
I_{SB1}	V_{CC} Standby Current CMOS		1	µA	$\overline{CE}$ = V_{CC} ±0.5V = $\overline{RESET}$ V_{CC} = 5.5V, $\overline{OE}$ = V_{IH}
I_{SB2}	V_{CC} Standby Current TTL		400	µA	$\overline{CE}$ = $\overline{RESET}$ = V_{IH}, V_{CC} = 5.5V
I_{CC1}	V_{CC} Active Read Current		30	mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}
I_{CC2}[1]	V_{CC} Program/Erase Current		60	mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} Program/Erase in Progress
I_{CC4}	V_{PP} Reset Current		1	µA	V_{CC} = 5.5V $\overline{RESET}$ = V_{SS} ±0.5V
V_{IL}	Input Low Level	−0.5	0.8	V	
V_{OL}	Output Low Level	0.7 x V_{CC}	0.45	V	I_{OL} = 12mA, V_{CC} = 4.5V
V_{IH1}	Input High Level CMOS		V_{CC}+0.3	V	
V_{OH2}	Output High Level CMOS	V_{CC}-0.4		V	I_{OH} = -100µA, V_{CC} = 4.5V
V_{ID}	Voltage for Signature and Temporary Sector Unprotect	11.5	12.5	V	V_{CC} = 5V
V_{OH1}	Output High Level CMOS	0.85 V_{CC}		V	V_{CC} = 4.5V I_{OH} = -2.5mA
IL_{IT}	Input Leakage Current -High Voltage		50	µA	V_{CC} = 5.5V A_9 = $\overline{OE}$, $\overline{RESET}$ = 12.5V
V_{IH2}	Input High Level TTL	2	V_{CC}+0.5	V	
V_{OH3}	Output High Level TTL	2.4		V	

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

SUPPLY CHARACTERISTICS

| Symbol	Parameter	Limits		Unit
		Min	Max.	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	3.2	4.2	V
V_{CC}	V_{CC} Supply Voltage	4.5	5.5	V

A.C. CHARACTERISTICS, Read Operation

V_{CC} = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	29F150-12		29F150-15		29F150-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	120		150		200		ns
t_{ELQV}	t_{CE}	$\overline{CE}$ Access Time		120		150		200	ns
t_{AVQV}	t_{ACC}	Address Access Time		120		150		200	ns
t_{GLQV}	t_{OE}	$\overline{OE}$ Access Time		35		50		50	ns
t_{AXQX}	t_{OH}	Output Hold from Address $\overline{OE}/\overline{CE}$ Change	0		0		0		ns
t_{GHQZ}	t_{DF}[1][2]	$\overline{OE}$ High to Output High-Z		20		30		30	ns
t_{EHQZ}	t_{HZ}[1][2]	$\overline{CE}$ High to Output High-Z		20		30		30	ns
	t_{READY}[1]	$\overline{RESET}$ Pin Low to Read Mode		20		20		20	μs

Figure 1. A.C. Testing Input/Output Waveform[3][4][5][6]
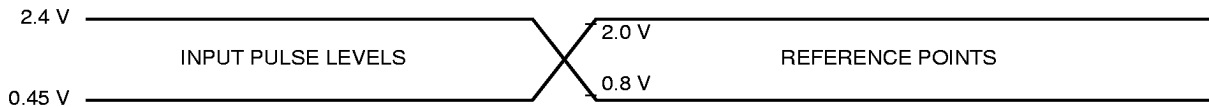
5096 FHD F03

Figure 2. A.C. Testing Load Circuit (example)
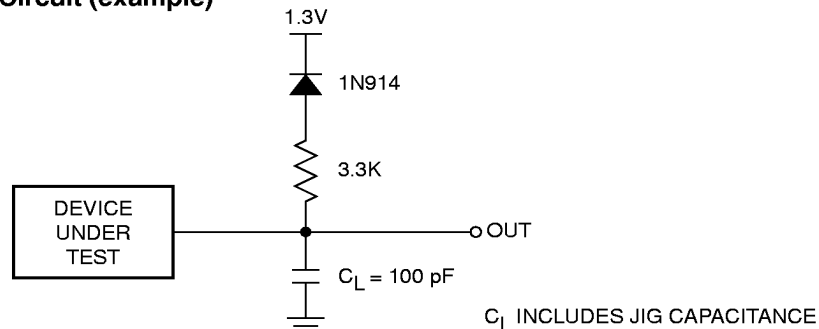
5108 FHD F04

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
(3) Input Rise and Fall Times (10% to 90%) = 20 ns.
(4) Input Pulse Levels = 0.45V and 2.4V.
(5) Input and Output Timing Reference = 0.8V and 2.0V.
(6) Output Load: ITTL gate and 100pF.

A.C. CHARACTERISTICS, Program/Erase Operation

$V_{CC} = +5V \pm 10\%$

JEDEC Symbol	Standard Symbol	Parameter	29F150-12		29F150-15		29F150-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	45		45		45		ns
t_{DVWH}	t_{DS}	Data Setup Time	45		45		45		ns
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	$\overline{WE}$ Pulse Width	45		45		45		ns
t_{WHDL}	t_{WPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}	—	Duration of Programming Operations	16		16		16		μs
t_{WHWH2}	—	Duration of Erase Operations (Sector)	1		1		1		Sec
	t_{OES}[1]	Output Enable Setup Time	0		0		0		ns
	t_{OEH}[1]	$\overline{OE}$ Hold Time	0		0		0		ns
	t_{GHWL}	READ Recovery Time Before WRITE ($\overline{OE}$ HIGH to $\overline{WE}$ LOW)	0		0		0		ns
	t_{VCS}[1]	V_{CC} Setup Time	50		50		50		μs
	t_{VIDR}	Rise Time to V_{ID}	500		500		500		ns
	t_{RP}	$\overline{RESET}$ Pulse Width	500		500		500		ns
	t_{RSP}	$\overline{RESET}$ Setup Time	4		4		4		μs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ERASE AND PROGRAMMING PERFORMANCE[10]

Parameter	29F150-12			29F150-15			29F150-20			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Sector Erase Time		1.0	15		1.0	15		1.0	15	Sec
Chip Program Time		3.6	25		3.6	25		3.6	25	Sec
Byte Program Time		7	1000		7	1000		7	1000	μs
Chip Erase Time		8	120		8	120		8	120	Sec

FUNCTION TABLE[1]

Mode	Pins					Notes
	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	
Output Disable	X	V_{IL}	V_{IH}	V_{IH}	High-Z	
Standby	V_{IH}	V_{IH}	X	X	High-Z	
Signature (MFG)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	31H	$A_0 = A_1 = A_6 = V_{IL}$, $A_9 = 12V$
Signature (Device)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	DAH=29F150T DBH=29F150B	$A_0 = V_{IH}$, $A_9 = 12V$ $A_1 = A_6 = V_{IL}$
Write Cycle	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	During Write Cycle
Enable Sector Protect	V_{IH}	V_{IL}	V_{ID}	V_{IL}	X	$A_6 = V_{IL}$ $A_9 = 12V$
Verify Sector Protect	V_{IH}	X	X	X	O1H	$A_0 = A_6 = V_{IL}$ $A_1 = V_{IH}$, $A_9 = 12V$ $A_{13} - A_{17} = $ Sector Addr.
Temporary Sector Unprotect	V_{ID}	X	X	X	X	
Reset	V_{IL}	X	X	X	HIGH-Z	

WRITE COMMAND TABLE

Commands are written into the command register in one to six write cycles. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	First Bus Cycle			Second Bus Cycle			Third Bus Cycle			Fourth Bus Cycle			Fifth Bus Cycle			Sixth Bus Cycle		
	Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Read/Reset	Write	X	F0H															
Erase Suspend/ Erase Resume	Write	X	B0H	Write	X	30H												
Chip Erase	Write	555H	AAH	Write	AAAH	55H	Write	555H	80H	Write	555H	AAH	Write	AAAH	55H	Write	555H	10H
Sector Erase	Write	555H	AAH	Write	AAAH	55H	Write	555H	80H	Write	555H	AAH	Write	AAAH	55H	Write	Sect Addr.	30H
Byte Program	Write	555H	AAH	Write	AAAH	55H	Write	555H	A0H	Write	A_{IN}	D_{IN}						
Read Sig. (MFG)	Write	555H	AAH	Write	AAAH	55H	Write	555H	90H	Read	0000H	31H						
Read Sig. (DEV)	Write	555H	AAH	Write	AAAH	55H	Write	555H	90H	Read	0001H	DAH-29F150T DB-29F150B						
READ/RESET	Write	555H	AAH	Write	AAAH	55H	Write	555H	F0H	Read	A_{IN}	D_{OUT}						

Note:
(1) Logic Levels: X = Logic 'Do not care' (V_{IH}, V_{IL}, V_{PPL}, V_{PPH})

READ OPERATIONS

Read Mode

The CAT29F150 memory can be read from any of its sectors by sending the Read Command Mode to the command register.

CAT29F150 automatically resets to Read Mode upon initial device power up. A read operation is performed with both $\overline{CE}$ and $\overline{OE}$ low and $\overline{WE}$ high. The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 18 address pins. The respective timing waveforms for the read operation are shown in Figure 2. Refer to the AC Read Characteristics for specific timing parameters.

Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of the device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A9 or by sending an instruction to the command register (see write operations).

The conventional method is entered as a regular read mode by driving the $\overline{CE}$ and $\overline{OE}$ low (with $\overline{WE}$ high), and applying the required high voltage on address pin A9 while A0, A1 and A6 are V_{IL} level and the rest of address are don't cares.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on Outputs I/O_7 to I/O_0:

Catalyst Code = 0011 0001(31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O_7 to I/O_0:

CAT29F150T = 1101 1010(DAH)

CAT29F150B = 1101 1011(DBH)

A Read cycle from address XX02H (A_{13}-A_{17} set to the desired sector) retrieves 01H for a protected sector and 00H for a non-protected sector.

Standby Mode

With $\overline{CE}$ and $\overline{RESET}$ at a logic-high level, the CAT29F150 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. Also, when the $\overline{RESET}$ pin is low, the CAT29F150 is in a standby mode ($\overline{CE}$ is don't care). The outputs are placed in a high-impedance state independent of the $\overline{OE}$ status.

Figure 3. A.C. Timing for Read Operation
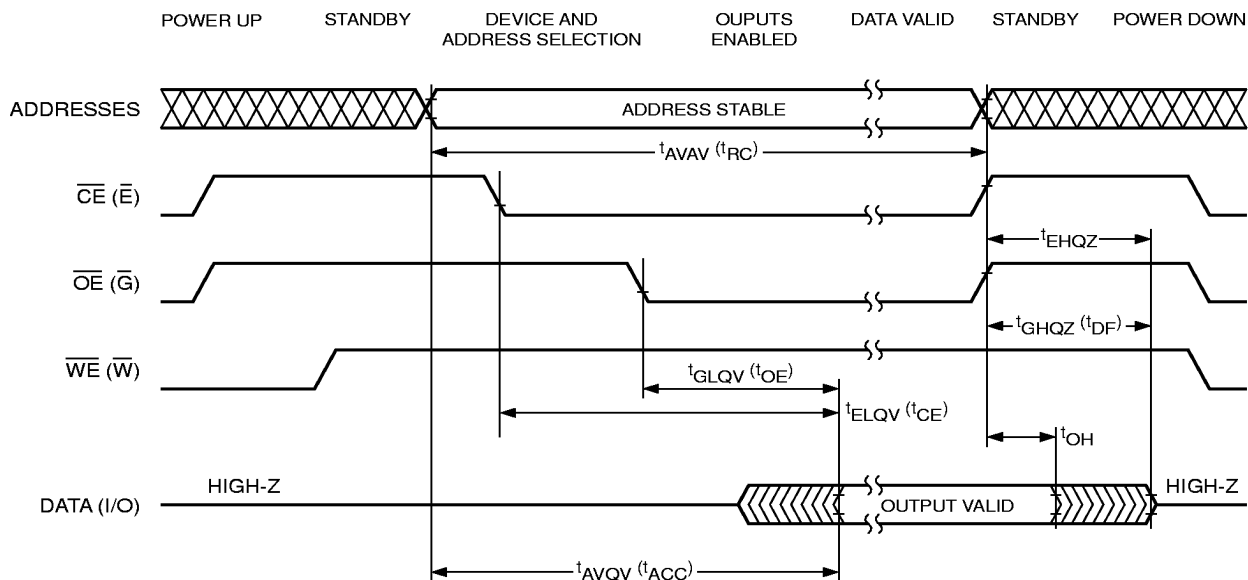
29F150 F05

WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

Read Array

The device can be put into a Read Mode by initiating a write cycle Read/Reset Command on the data bus. The device is also in a standard Read Mode after the initial device power up. This eliminates any accidental writes during power up or power down. The device remains in the Read Mode until command register contents are changed.

Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the command sequence into the command register. A read cycle from address XX00H with $\overline{CE}$ and $\overline{OE}$ low (and $\overline{WE}$ high) will output the device signature. A_{12}-A_{17} are don't cares for this operation.

Catalyst Code = Catalyst Code = 0011 0001 (31H)

A Read cycle from address XX01H retrieves the binary code for the device on outputs I/O_7 to I/O_0:

CAT29F150T = 1101 1010 (DAH)
CAT29F150B = 1101 1011 (DBH)

A Read cycle from address XX02H (A_{13}-A_{17} set to the desired sector) retrieves 01H for a protected sector and 00H for a non-protected sector.

To terminate the operations, it is necessary to write another valid command into the register.

Program/Erase

Programming and erasing of the CAT29F150 is done by sending the command sequence as shown in Write Command Table to the command register. The command register is written by driving the $\overline{CE}$ and $\overline{WE}$ Low and $\overline{OE}$ High. Address inputs are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. Refer to AC characteristics and waveforms (Program/Erase) for specific timing parameters.

Sector Protection

All the six sectors can be protected in any combination by following the sequence in the function table. It is possible to determine if a certain sector is protected or not. A Read cycle from address XX02H (A_{13}-A_{17} set to the desired sector) retrieves 01H for a protected sector

and 00H for a non-protected sector. The protected sectors can be temporarily unprotected by applying 12V to the $\overline{RESET}$ pin (Refer to figure for details). This enables writing or erasing the protected sector by specifying the sector address. Once the 12V is removed from the $\overline{RESET}$ pin the CAT29F150 goes back its original state.

Byte Programming

Byte programming is done using four write commands. The first two commands are used as unlock write commands. The third write command is the program set up command. The fourth write command is used to send the address and the data information. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. The rising edge initiates programming. The Byte programming is done using the embedded programming algorithm. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

Any command written to the chip during the programming algorithm will be ignored. As soon as the programming is done, the device resets to a read mode. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Chip Erase

Chip erase is done using six write commands. The first two commands are unlock write commands. The third write command is Erase Setup command. This is followed by two more commands which are unlock write commands. The sixth command is the chip erase command. The rising edge of $\overline{CE}$ or $\overline{OE}$ initiates erasing. Chip erasing is done using the Embedded erasing algorithm. This algorithm does not require all locations to be programmed before the chip is erased, since it automatically programs and verifies all locations to a all zero pattern before it starts the chip erase. As soon as the erasing is done, the device resets to a read mode.

Sector Erase

Sector erase is done using six write commands. The first two commands are unlock write commands. The third write command is Erase Setup command. This is followed by two more commands which are unlock write commands. The sixth command is the sector erase command. The address part of the sixth write command specifies the sector address. The address can be anywhere within the sector that needs to be erased. The sector address is latched on the falling edge of $\overline{WE}$, while the command 30H is latched on the rising edge of $\overline{WE}$. The sector erase begins after a time out of 80 ms from the rising edge.

Multiple sectors can be erased sequentially by writing the six write commands . This sequence is followed with writes of the Sector Erase command to addresses in other sectors to be sequentially erased. The time between writes must be less than 80 ms. After the complete sequence, the sector erase begins after a time out of 80 ms from the last $\overline{WE}$ or $\overline{CE}$ rising edge. If another falling edge occurs with the 80 ms time-out window the timer will be reset. Any command other than Sector Erase or Erase Suspend during the sector erase time out does not execute, resets the device to the read mode, and cancels the previous sector erase command.

Sector erasing is done using the Embedded erasing algorithm. This algorithm does not require all locations to be programmed before the chip is erased, since it automatically programs and verifies all locations to a all zero pattern before it starts the chip erase. When performing sector erase, sectors that are protected or not selected for erasure will not be changed. As soon as the erasing is done, the device resets to a read mode.

Erase Suspend

The Erase Suspend Command allows erase sequence interruption in order to read data from or program data to another sector of memory not being erased (takes 20 ms to suspend the erase operation). Writing the erase suspend command during the sector erase time out results in termination of the time out period and suspension of the erase operation. The Erase suspend command is valid during erase operation only and the device defaults to a read mode until it receives another command. Any command other read, program or erase resume commands written during the erase suspend mode will be ignored. Sending the Erase Resume command (30H) will resume the erase operation.

WRITE OPERATION STATUS

$\overline{DATA}$ Polling

$\overline{DATA}$ Polling is provided to indicate the completion of write or erase cycle. $\overline{DATA}$ Polling is active during the programming, Erasing, Erase Suspend and sector erase time out. Once these functions are initiated, attempting to read the last byte written will output the complement of that data on I/O_7 until the function is completed. Upon completion of the functions, all I/Os will output true data during a read cycle.

$\overline{DATA}$ Polling is valid after the rising edge of $\overline{WE}$ or $\overline{CE}$ during the last write command of the sequence of that function (e.g. sixth $\overline{WE}$ or $\overline{CE}$ rising of edge for a erase cycle). $\overline{DATA}$ Polling can be done at an address within a sector that is being programmed or erased. $\overline{DATA}$ polling may give an inaccurate result if the address used is in a protected sector.

Toggle Bit

In addition to the $\overline{DATA}$ Polling feature, the device offers an additional method for determining the completion of write or erase cycle. While a write or erase cycle is in progress, reading data from the device will result in I/O_6 toggling between one and zero. However, when the erase or write cycle is complete, I/O_6 stops toggling and valid data can be read from the device. Toggle Bit function is also valid during Erase Suspend/Resume command and sector erase time out window. When the part has entered erase suspended mode, I/O_6 will stop toggling. The user must use the address of a sector Not being erased when reading I/O_6 to determine if the erase operation has been suspended.

Toggle Bit is valid after the rising edge of $\overline{WE}$ or $\overline{CE}$ during the last write command of the sequence of that function (e.g. sixth $\overline{WE}$ or $\overline{CE}$ rising of edge for a erase cycle).

Exceeded Timing Limits

The CAT29F150 features a program or erase failure indicator. I/O_5 will produce a "1" (Failure Condition) when the specified limits for program or erase times have been exceeded. The $\overline{CE}$ circuit will partially power down the device under these conditions. The failure condition may also result if a user tries to program a "1" to a location that was previously programmed to a "0". If timing limits are exceeded, reset the device.

Sector Erase Timer

After the six command sequence for the sector erase, the sector erase time out will begin. I/O_3 will remain low until the time out is complete. If $\overline{DATA}$ Polling or the Toggle Bit indicates the device has been written with a sector Erase Command, I/O_3 may be used to determine if the sector erase timer window is still open. If I/O_3 is at "1", attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is complete. If I/O_3 is at "0", the device will accept additional sector erase commands.

Erase Toggle Bit

In the Erase (chip or sector) operation, I/O_2 will toggle with $\overline{OE}$ or $\overline{CE}$ when read is attempted. For a sector erase operation, I/O_2 will not toggle if the read address is not within the sector that is being erased. For the Multiple Sector Erasing, I/O_2 can be used to indicate which sector is being erased. Also, if I/O_5 is at "1" during Multiple Sector Erasing, I/O_2 toggling will help detect which sector exceeded timing limits.

OTHER FEATURES

Hardware $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ pin, when set to low will reset any operation that is in progress and sets the CAT29F150 to a read mode. The $\overline{\text{RESET}}$ pin must be kept low for at least 500ns. When $\overline{\text{RESET}}$ is low, the device will be in the standby mode for the duration of pulse (20ms) and all I/O pins are tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted.

Hardware Protection

The following is a list of hardware data protection features that are incorporated into the CAT29F150.

a) The internal command register for the CAT29F150 is reset to the Read Mode on power up. This offers protection against accidental programming or erasing caused by spurious system level signals that may exist during power up/down transitions.

b) The CAT29F150 requires multiple commands before a user can erase or program into the device. For example a write instruction requires four commands.

c) Vcc sense provides for write protection when Vcc falls V_{LKO} voltage level.

d) Noise pulses of less than 5ns on the $\overline{\text{WE}}$, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ inputs will not result in a write cycle.

e) Write inhibited is activated by holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high.

f) Power up of the device with $\overline{\text{CE}}$ low, $\overline{\text{WE}}$ low and $\overline{\text{OE}}$ high will not accept commands on the rising edge of $\overline{\text{WE}}$. The device is in a read mode on power up.

Figure 4. Automated Program Algorithm
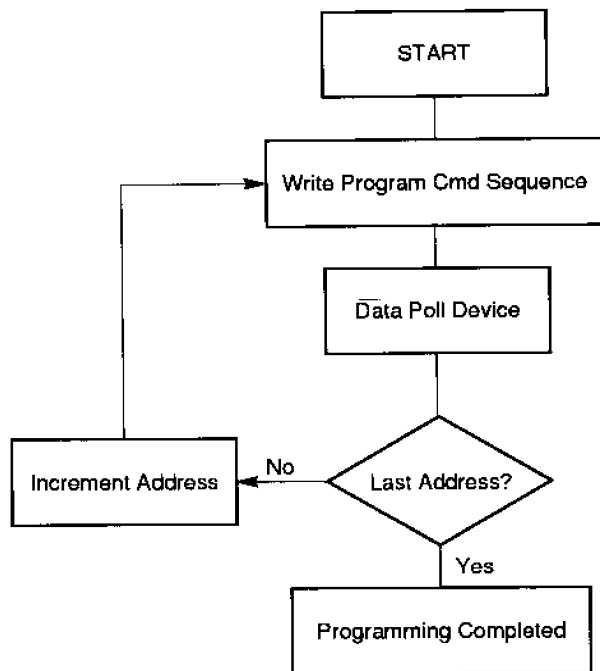
Bus Operation	Sequence	Comments
Standby*		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{DATA}}$ Polling to Verify Programming
Read		Compare Data Output to Data Expected

* Device is either powered-down in erase inhibit or in program inhibit.

Figure 5. Embedded Erase Algorithm

Bus Operation	Sequence	Comments
Standby*		
Write	Erase	
Read		$\overline{DATA}$ Polling to Verify Erasure
Read		Compare Output to FFH

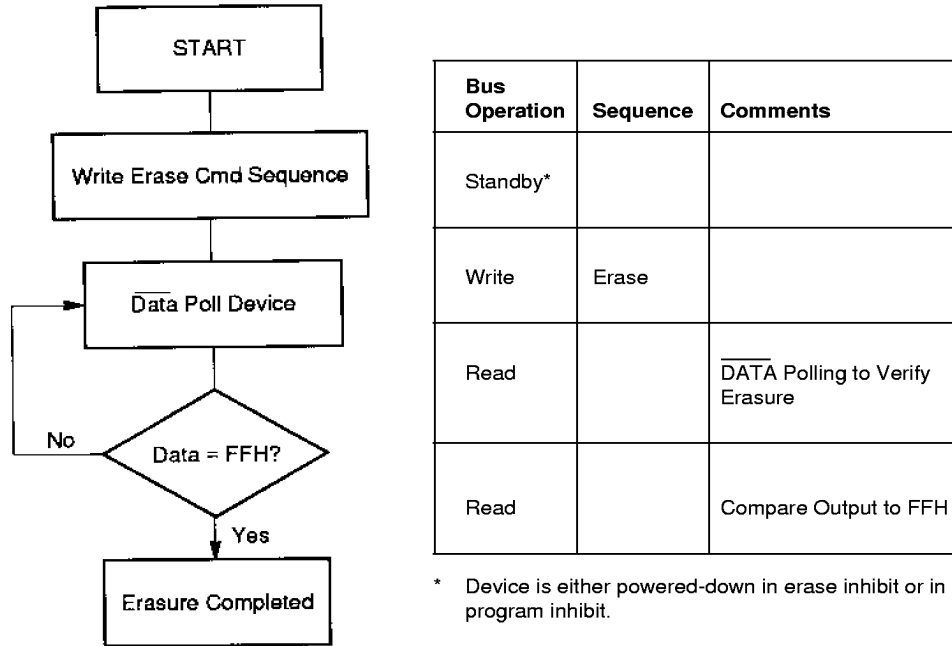*   Device is either powered-down in erase inhibit or in program inhibit.
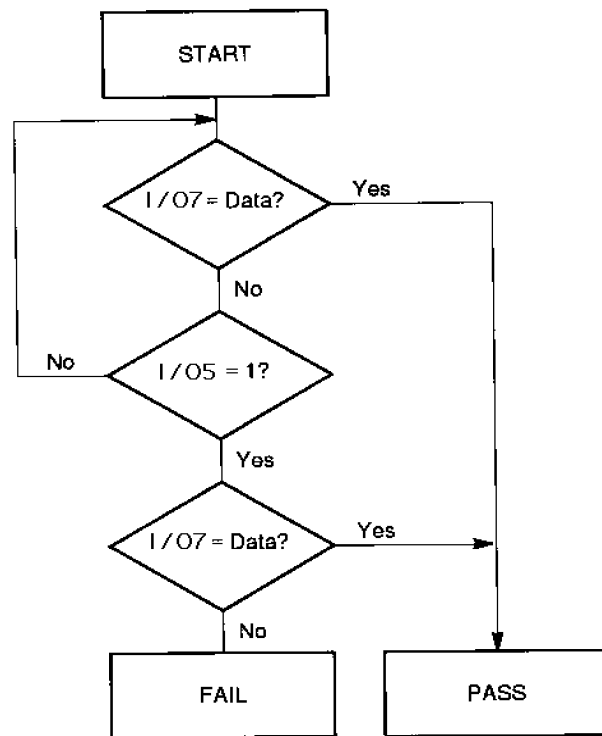
Figure 6. DATA Polling Algorithm
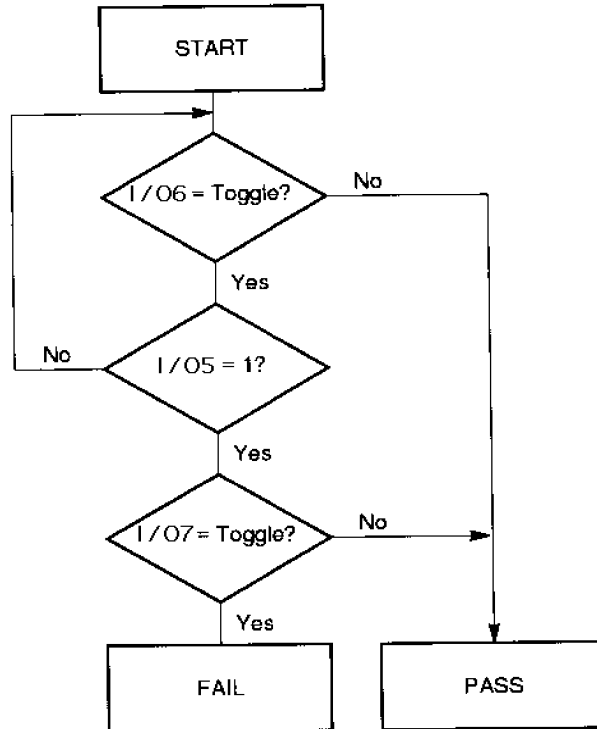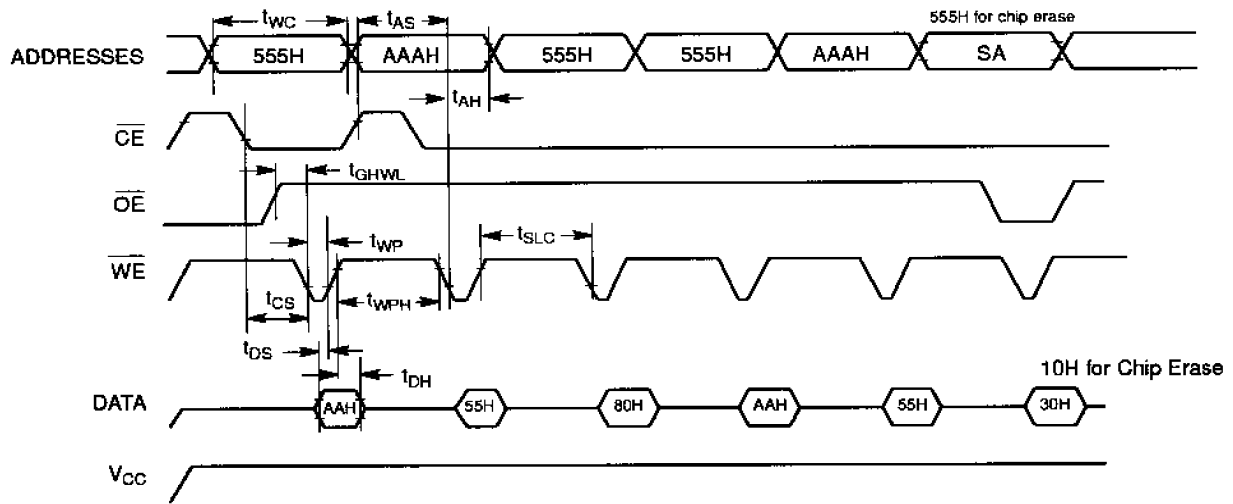
Figure 7. Toggle Bit Algorithm

Figure 8. Temporary Sector Unprotect Algorithm
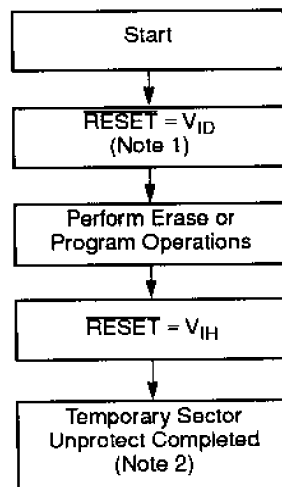
Note 1:   All protected sectors unprotected
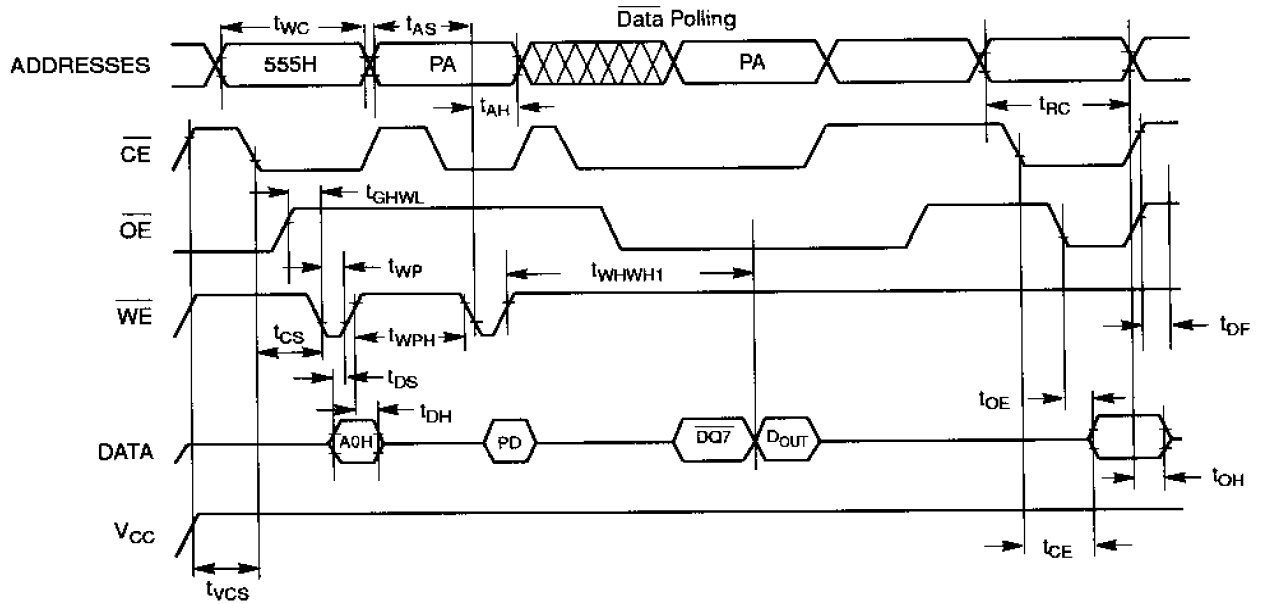Note 2:   All previously protected sectors are protected once again

Figure 10. AC Waveform for Chip/Sector Erase Operations

Note: SA is the sector address for Sector Erase.
                     Addresses = don't care for Chip Erase

Figure 11. Program Operation Timings

Note 1:   I/O$_7$ is the output of the complement of the data written to the device
Note 2:   D$_{OUT}$ is the output of the data written to the device
Note 3:   PA is the address of the memory location to be programmed
Note 4:   PD is the data to be programmed at the byte address
Note 5:   Drawing shows the last two cycles of a two-bus sequence

Figure 12. AC Waveforms for $\overline{DATA}$ Polling During Automated Algorithm Operations
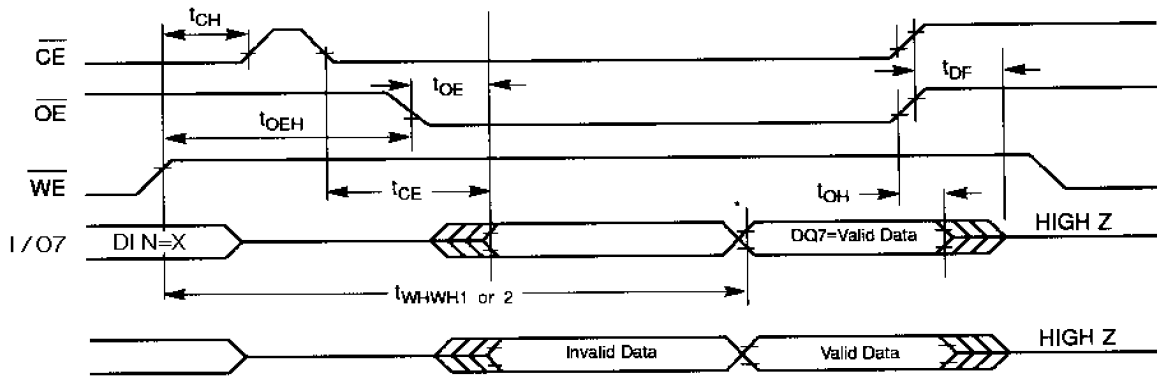

Figure 13. AC Waveforms for Toggle Bit During Automated Algorithm Operations
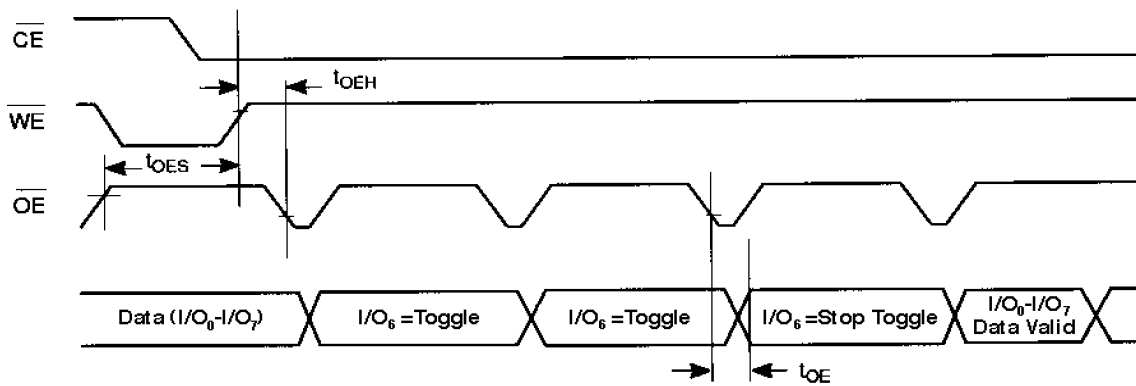
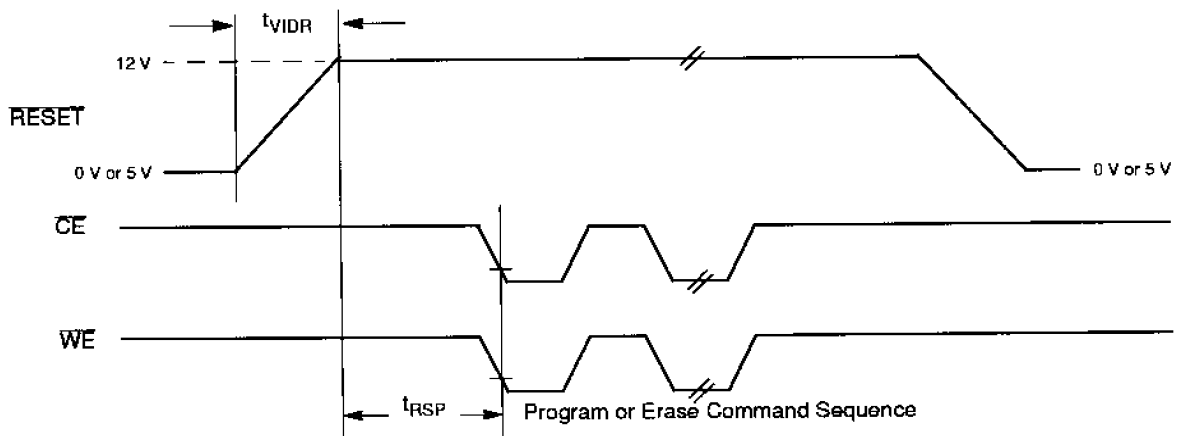**Figure 14. Temporary Sector Unprotect Timing Diagram**
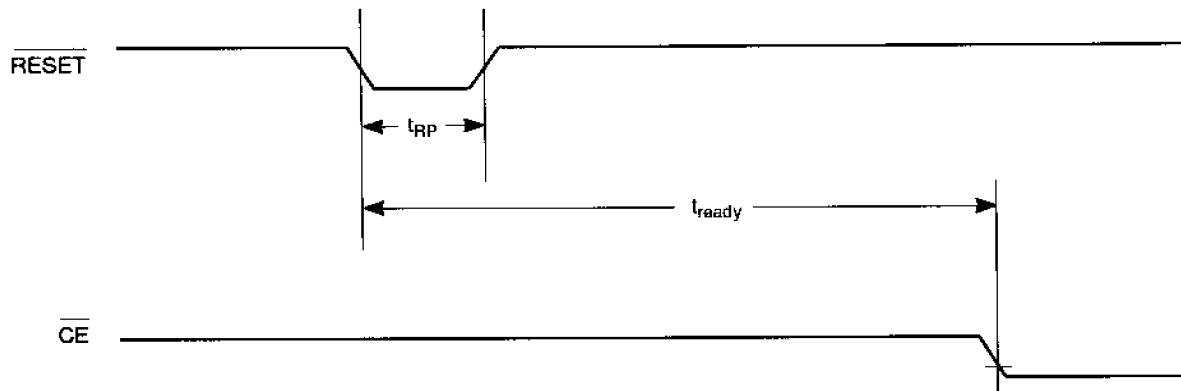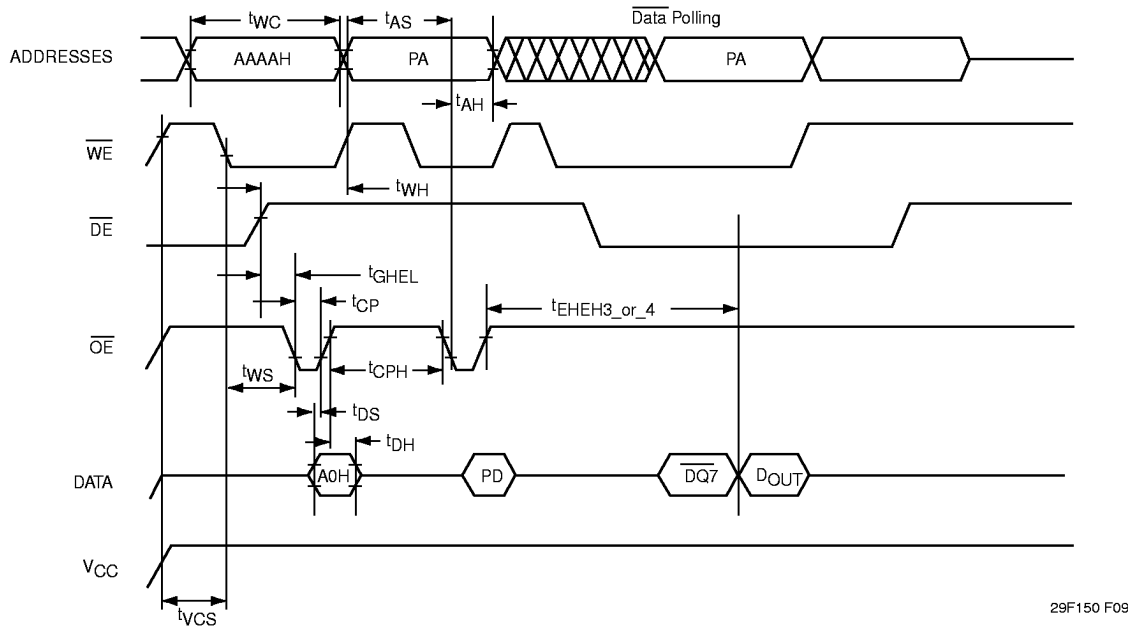

Figure 15. RESET Timing Diagram

Figure 16. Alternate CE Controlled Write Operation Timings

29F150 F09

Note 1:   PA is the address of the memory location to be programmed
Note 2:   PD is the data to be programmed at the byte address
Note 3:   I/O$_7$ is the output of the complement of the data written to the device
Note 4:   D$_{OUT}$ is the output of the data written to the device
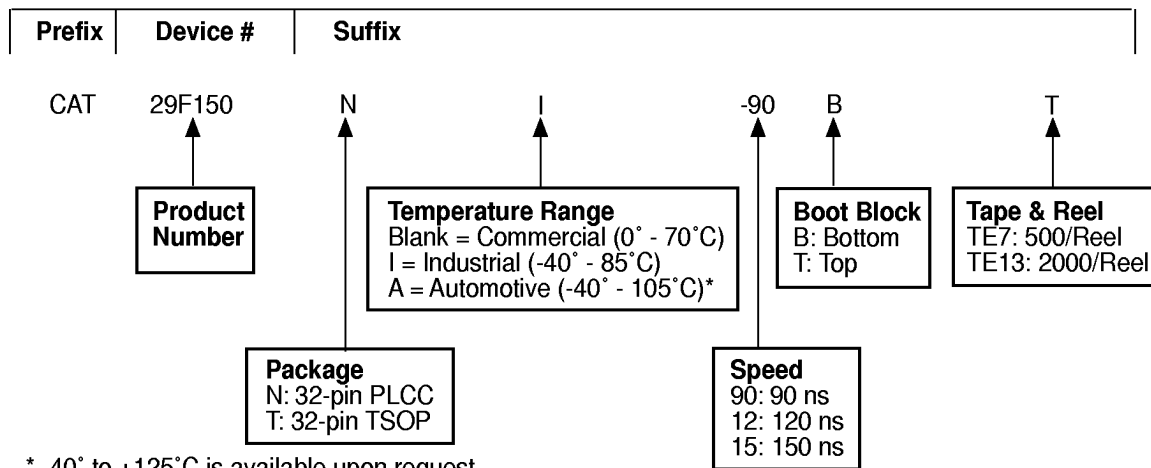Note 5:   Drawing shows the last two bus cycles of a four-bus sequence

ALTERNATE $\overline{CE}$ CONTROLLED WRITES

JEDEC Symbol	Standard Symbol	Parameter	29F150-12 Min.	Max.	29F150-15 Min.	Max.	29F150-20 Min.	Max.	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	45		45		45		ns
t_{DVEH}	t_{DS}	Data Setup Time	45		45		45		ns
t_{EHDX}	t_{DH}	Data Hold Time	0		0		0		ns
t_{ELEL}	t_{WS}	$\overline{WE}$ Setup Time	0		0		0		ns
t_{EHEH}	t_{WH}	$\overline{WE}$ Hold Time	0		0		0		ns
t_{ELEH}	t_{CP}	$\overline{WE}$ Pulse Width	45		45		45		ns
t_{EHDL}	t_{CPH}	$\overline{WE}$ High Pulse Width	20		20		20		ns
t_{WHWH1}	—	Duration of Programming Operations	16		16		16		µs
t_{WHWH2}	—	Duration of Erase Operations (Sector)	1		1		1		Sec
	t_{OES}[1]	Output Enable Setup Time	0		0		0		ns
	t_{OEH}[1]	$\overline{OE}$ Hold Time	0		0		0		ns
	t_{GHEL}	READ Recovery Time Before WRITE ($\overline{OE}$ HIGH to $\overline{WE}$ LOW)	0		0		0		ns
	t_{VCS}[1]	V_{CC} Setup Time	50		50		50		µs
	t_{VIDR}	Rise Time to V_{ID}	500		500		500		ns
	t_{RP}	$\overline{RESET}$ Pulse Width	500		500		500		ns
	t_{RSP}	$\overline{RESET}$ Setup Time	4		4		4		µs

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

ORDERING INFORMATION

Prefix	Device #	Suffix

CAT 29F150 N I -90 B T

Product Number

Package
N: 32-pin PLCC
T: 32-pin TSOP

Temperature Range
Blank = Commercial (0˚ - 70˚C)
I = Industrial (-40˚ - 85˚C)
A = Automotive (-40˚ - 105˚C)*

Speed
90: 90 ns
12: 120 ns
15: 150 ns

Boot Block
B: Bottom
T: Top

Tape & Reel
TE7: 500/Reel
TE13: 2000/Reel

* -40˚ to +125˚C is available upon request

29F150 F13