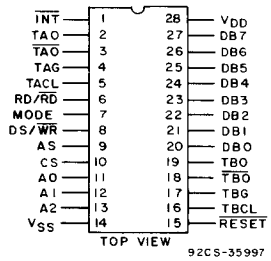


TERMINAL ASSIGNMENT

CMOS Dual Counter-Timer

Features:

- *Compatible with general-purpose and multiplexed address and data bus microprocessor systems*
- *Will accept separate read and write signals or a common read/write signal with data strobe*
- *Two 16-bit down-counters and two 8-bit control registers*
- *5 modes including a versatile variable-duty cycle mode*
- *Programmable gate-level select*
- *Two-complemented output pins for each counter-timer*
- *Software-controlled interrupt output*

The RCA-CDP6848 and CDP6848C$^{\Delta}$ are dual counter-timers consisting of two 16-bit programmable down counters that are independently controlled by separate control registers. The value in the registers determine the mode of operation and control functions. Counters and registers are directly addressable in memory space by many general-industry-type microprocessors.

Each counter-timer can be configured in five modes with the additional flexibility of gate-level control. The control registers in addition to mode formatting, allow software start and stop, interrupt enable, and an optional read control that allows a stable readout from the counters. Each counter-timer has software control of a common interrupt output with an interrupt status register indicating which counter-timer has timed out.

In addition to the interrupt output, true and complemented outputs are provided for each counter-timer for control of peripheral devices.

The CDP6848 and CDP6848C are functionally identical. They differ in that the CDP6848 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP6848C has a recommended operating voltage range of 4 to 6.5 volts. These types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

$^{\Delta}$Formerly RCA Dev. Type No. TA11430 and TA11430C, respectively.

Table I - Mode Description

	Mode	Function	Application
1	Timeout	Outputs change when clock decrements counter to "0"	Event counter
2	Timeout Strobe	One clockwide output pulse when clock decrements counter to "0"	Trigger pulse
3	Gate-Controlled One Shot	Outputs change when clock decrements counter to "0". Retriggerable	Time-delay generation
4	Rate Generator	Repetitive clockwide output pulse	Time-base generator
5	Variable-Duty Cycle	Repetitive output with programmed duty cycle	Motor control

CDP6848, CDP6848C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to Vss terminal)
- CDP6848 ..... -0.5 to +11 V
- CDP6848C ..... -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
- For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
- For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
- For T_A = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types ..... 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPE D ..... -55 to +125°C
- PACKAGE TYPE E ..... -40 to +85°C

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP6848			CDP6848C			
					Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	µA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
		9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level	V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	µA
			0, 10	10	—	—	±2	—	—	—	
Operating Current	I_{DD1}Δ	—	0, 5	5	—	1.5	3	—	1.5	3	mA
		—	0, 10	10	—	6	12	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A=25° C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 µA.

ΔOperating current is measured at 200 kHz for V_{DD}=5 V and 400 kHz for V_{DD}=10 V, with open outputs.

CDP6848, CDP6848C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS				UNITS
		CDP6848		CDP6848C		
		Min.	Max.	Min.	Max.	
DC Operating Voltage Range		4	10.5	4	6.5	V
Input Voltage Range		Vss	VDD	Vss	VDD	
Maximum Clock Input Rise or Fall Time	tr, tf	—	5	—	5	μs
Minimum Clock Pulse Width	tWL, tWH	200	—	200	—	ns
Clock Input Frequency	fCL	DC	Δ	DC	•	MHz

Δ VDD = 9.5, fCL = 2.5 MHz
• VDD = 4.75 V, fCL = 1 MHz

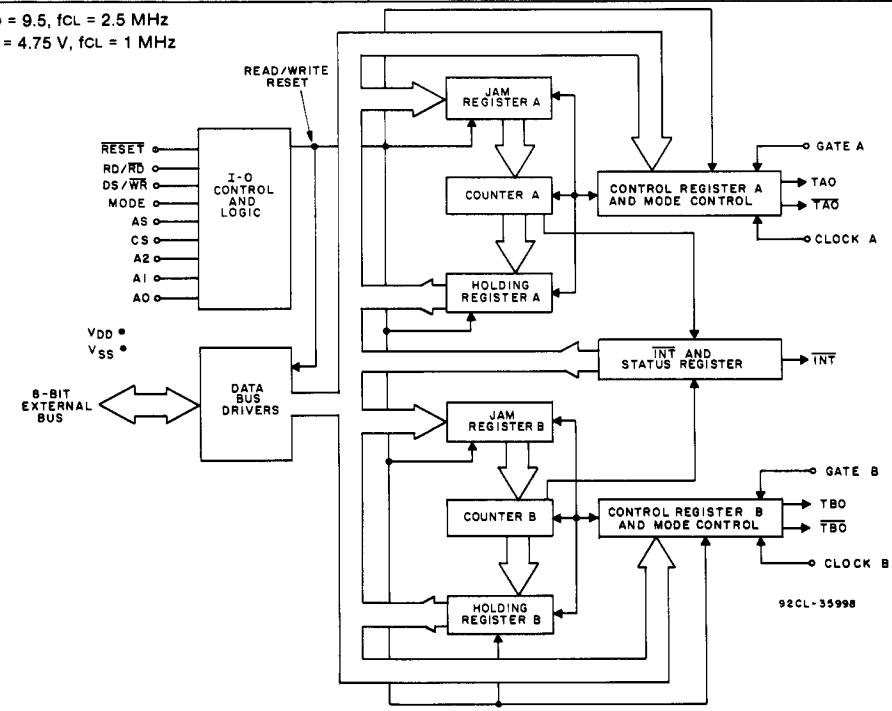


Fig. 1 - Functional diagram CDP6848 and CDP6848C.

Functional Definitions for CDP6848 and CDP6848C Terminals

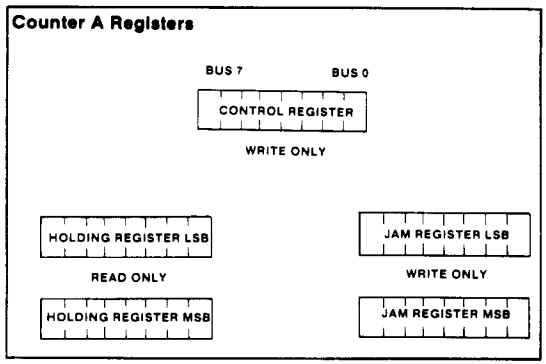
TERMINAL	USAGE	TERMINAL	USAGE
VDD-Vss	Power	CS	Active high input that enables device
DB0-DB7	Data to and from device	INT	Low when counter is "0"
DS/WR, RD/RD	Directional control signals	RESET	When active, TAO, TBO are low, TAO, TBO are high. Interrupt status register is cleared counter A and B are stopped.
A0, A1, A2	Address that select counters or registers		
TACL, TBCL	Clocks used to decrement counters		
TAG, TBG	Gate inputs that control counters		
TAO, TAO	Complemented outputs of Timer A	MODE	Determine the operation of the directional control Mode = 0 requires a 8085 interface Mode = 1 requires a CDP6805 interface
TBO, TBO	Complemented outputs of Timer B		
ADDRESS STROBE	Latches the address on pins A0, A1, and A2		

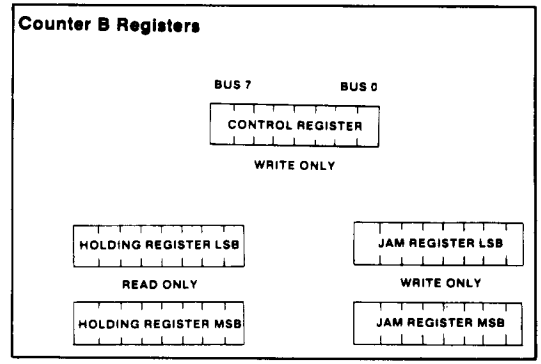
CDP6848, CDP6848C

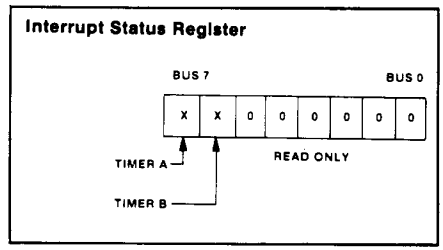
REGISTER TRUTH TABLE

ADDRESS			ACTIVE		REGISTER OPERATION
A2	A1	A0	DS/$\overline{WR}$	$\overline{RD}$	
1	1	0	X		Write Counter A MSB
1	1	0		X	Read Counter A MSB
0	1	0	X		Write Counter A LSB
0	1	0		X	Read Counter A LSB
1	0	0	X		Control Register A
1	1	1	X		Write Counter B MSB
1	1	1		X	Read Counter B MSB
0	1	1	X		Write Counter B LSB
0	1	1		X	Read Counter B LSB
1	0	1	X		Control Register B
1	0	0		X	Interrupt Status Register
1	0	1		X	
0	0	0			Not Used
0	0	1			Not Used

PROGRAMMING MODEL







Functional Description — See Fig. 1

The dual counter-timer consists of two programmable 16-bit down counters, separately addressable and controlled by two independent 8-bit control registers. The word in the control register determines the mode and type of operation that the counter-timer performs. Writing to or reading from a counter or register is enabled by selective addressing during a write or read cycle. The data is placed on the data bus by the microprocessor during the write cycle or read from the counter during the read cycle. Data to and from the counters and to the control registers is in binary format.

Each counter-timer consists of three parts. The first is the counter itself, a 16-bit down counter that is decremented on the trailing edge (high to low transition) of the clock input. The second is the jam register that receives the data when the counter is written to. The word in the control register determines when the jam register value is placed into the counter. The third part is the holding register that places the counter value on the data bus when the counter is read.

When the counter has decremented to zero, three events occur. The first involves the common interrupt output pin that, if enabled, becomes active low. The second is the setting of a bit in the interrupt status register. This register can be read to determine which counter-timer has timed out. The third event is the logic change of the complemented output pins.

In addition to the clock input used to decrement the counter, a gate input is available to enable or initiate operation. The counter-timers are independent and can have different mode operations.

Write Operation

The counters and registers are separately addressable and are programmed via the data bus when the chip is selected with the DS/$\overline{WR}$ pin active. Normal sequencing requires that the counter jam register be loaded first with the required value (most significant and least significant byte in any order), and then the control register be accessed and loaded with the control word. The trailing edge of the DS/$\overline{WR}$ pulse will latch the control word into the control register and cause the counter to be jammed with its initial value. The counter will decrement on the trailing edge of succeeding clocks until it reaches zero. The output levels will then change, and if enabled, the interrupt output will become active and the appropriate timer bit will be set in the interrupt status register. The interrupt output and the interrupt status register can be cleared (to their inactive state) by addressing the control register with the DS/$\overline{WR}$ line active. For example, if counter A times out, control register A must be accessed to reset the interrupt output high and reset the timer A bit in the status register low. Timer B bit in the status register will be unaffected.

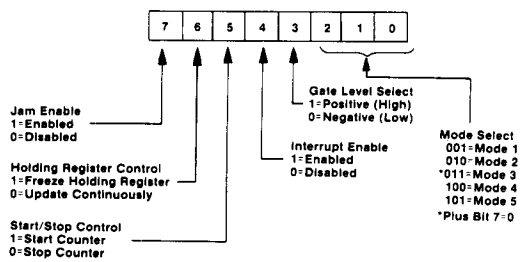
Read Operation

Each counter has a holding register that is continuously being updated by the counter and is accessed when the counter is addressed during read cycles. Counter reads are accomplished by halting the holding register and then reading it, or by reading the holding register directly. If the holding register is read directly, data will appear on the bus. However, if the clock decrements the counter between the two read operations (most and least significant byte), an inaccurate value will be read. To preclude this from happening, writing a "1" into bit 6 of the control register and then addressing and reading the counter will result in a stable reading. This operation prevents the holding register from being updated by the counter and does not affect the counter's operation.

To guarantee a valid read after a jam of the counter, the device must be clocked at least one time with the gate enabled in modes 1, 2, 4, and 5.

The interrupt status register is read by addressing either control register with the $\overline{RD}$ line active. A "1" in bit 7 indicates Timer A has timed out and a "1" in bit 6 indicates Timer B has timed out. Bits 0-5 are zeros.

Control Register



Bits 0, 1 and 2 — Mode Selects—See Mode Timing Diagrams (Figs. 2, 3, 4, 5 and 6).

	Bit 7	Bit 2	Bit 1	Bit 0
Mode 1 — Timeout	—	0	0	1
Mode 2 — Timeout Strobe	—	0	1	0
Mode 3 — Gate Controlled One Shot	0	0	1	1
Mode 4 — Rate Generator	—	1	0	0
Mode 5 — Variable-Duty Cycle	—	1	0	1
No Mode selected. Counter outputs unaffected.	—	0	0	0

Note: When selecting a mode, the timer outputs TAO and TBO are set low, and $\overline{TAO}$ and $\overline{TBO}$ are set high. If bits 0, 1 and 2 are all zero's when the control register is loaded, no mode is selected, and the counter-timer outputs are unaffected.

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Bit 3 — Gate level select — All modes require an enabling signal on the gate to allow counter operation. This enabling signal is either a level or pulse (edge). Positive gate level or edge enabling is selected by writing a "1" into this bit and negative (low) enabling is selected when bit 3 is "0". The gate level must be true (Gate pin TAG or TBG = Bit 3 Control Register) when JAM Register is loaded.

Bit 4 — Interrupt enable — Setting this bit to "1" enables the $\overline{INT}$ output, and setting it to "0" disables it. When reset, the $\overline{INT}$ output is at a high level. If the interrupt enable bit in the control register is enabled and the counter decrements to zero, the $\overline{INT}$ output will go low and will not return high until the counter-timer is reset or the selected control register is written to. Example: If timer B times out, control register B must be accessed to reset the $\overline{INT}$ output high. If the interrupt enable bit is set to "0", the counter's timeout will have no effect on the $\overline{INT}$ output.

In mode 5, the variable-duty cycle mode, the $\overline{INT}$ pin will become active low when the MSB in the counter has decremented to zero.

Bit 5 — Start/stop control — This bit controls the clock input to the counter and must be set to "1" to enable it. Writing a "0" into this location will halt operation of the counter. Operation will not resume until the bit is set to "1".

Bit 6 — Holding register control — Since the counter may be decrementing during a read cycle, writing a "1" into this location will hold a stable value in the hold register for subsequent read operations. Rewriting a "1" into bit 6 will cause an update in the holding register on the next trailing clock edge. If this location contains a "0", the holding register will be updated continuously by the value in the counter.

Bit 7 — Jam enable — When this bit is set to "1" during a write to the control register, the value in the jam register will be placed into the counter. The counter outputs TAO and TBO will be set high and $\overline{TAO}$ and $\overline{TBO}$ will be set low on the next trailing clock edge. If bit 0, 1, or 2 is equal to 1 (i.e. valid mode) then counting begins with the next clock edge. Setting this bit to "0" will leave the counter value unaffected. This location should be set to "0" any time a write to the control register must be performed without changing the preset counter value.

In mode 3, the hardware start is enabled by writing a "0" into bit 7. If a "1" is written to bit 7, the timeout will start immediately and mode 3 will resemble mode 1.

Changing Counter Values

Each counter must be stopped to reliably/load it from the Jam Register. A counter can be stopped by:

- An external reset,
- Timeout in Modes 1, 2, and 3 (Modes 4 and 5 properly reload and continue running at timeout),
- A write to the control register with Bit 7 = 0 (no JAM), Bit 5 = 1 (Start), and (Bit 2 + Bit 1 + Bit 0) = 1 (valid Mode select).

Once stopped, the counter can be jammed with a write to the control register with Bit 7 = 1 (Jam), Bit 5 = 1 (Start), and Bit 2 + Bit 1 + Bit 0) = 1. The Gate level must be true (match the value written in the control register) in modes 1, 2, 4, and 5.

NOTE: The outputs are cleared. (TXO = 0 and $\overline{TXO}$ = 1) with a write to the control register with (Bit 2 + Bit 1 + Bit 0) = 1.

MODE DESCRIPTIONS

Mode		Control Register	Gate Control
1	Timeout	X X X X X 0 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 1:

After the count is loaded into the jam register and the control register is written to with the jam-enable bit high, TXO goes high and $\overline{TXO}$ goes low. The input clock decrements the counter. When it reaches zero, TXO goes low and $\overline{TXO}$ goes high, and if enabled, the interrupt output is set low. When the control is decremented to 00H, the outputs (TAO and $\overline{TAO}$) will change logic level, the next clock will set the counter to FFFFH. Additional clocks are ignored.

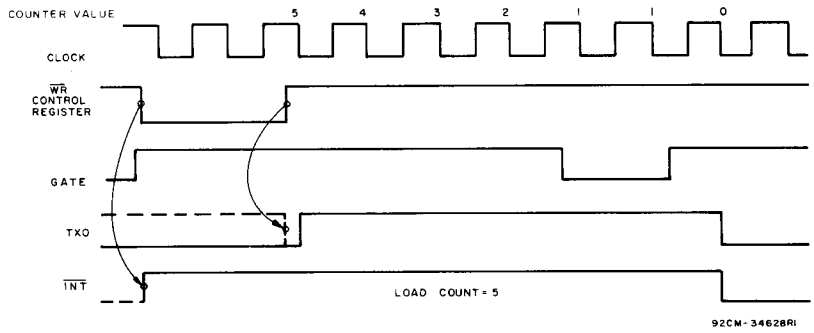

Fig. 2 - Timeout (mode 1) timing waveforms.

	Mode	Control Register	Gate Control
2	Timeout Strobe	X X X X X 0 1 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 2:

Operation of this mode is the same as mode 1, except the outputs will change for one clock period only and then return to the condition of TXO high and $\overline{TXO}$ low.

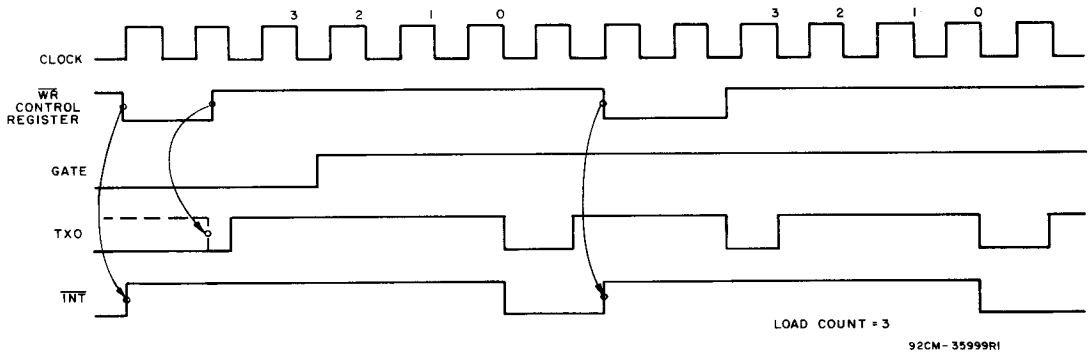

Fig. 3 - Timeout strobe (mode 2) timing waveforms.

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Mode		Control Register	Gate Control
3	Gate Controlled One Shot	0 X X X X 0 1 1 BUS 7 BUS 0	Selectable Positive or Negative Going Edge Initiates Operation

Mode 3:

After the jam register is loaded with the required value, the gate edge will initiate this mode. TXO will be set high, and $\overline{TXO}$ will be set low. The clock will decrement the counter. When zero is reached, TXO will go low and $\overline{TXO}$ will be high, and the interrupt output will be set low. The counter is retriggerable: While the counter is decrementing, a gate edge or write to the control register with the jam-enable bit high, will load the counter with the jam register value and restart the one-shot operation. The jam register value cannot be changed for proper retriggering prior to timeout.

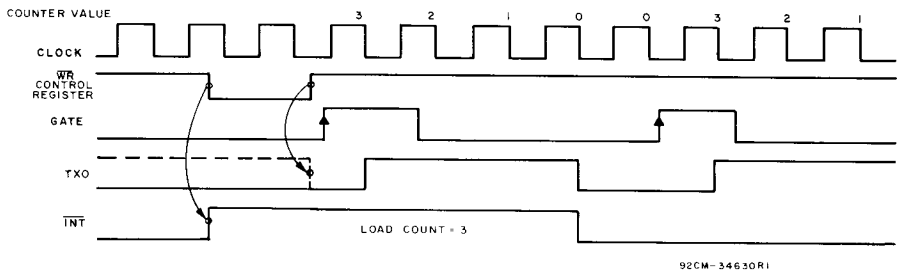


Fig. 4 - Gate controlled one-shot (mode 3) timing waveforms.

Note:
In order to avoid unwanted starts when selecting mode 3 or 4, the gate signal must be set to the opposite level that will be programmed.

Mode		Control Register	Gate Control
4	Rate Generator	X X X X X 1 0 0 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 4:

A repetitive clock-wide output pulse will be output, with the time between pulses equal to the counter's value, (trailing edge to leading edge).

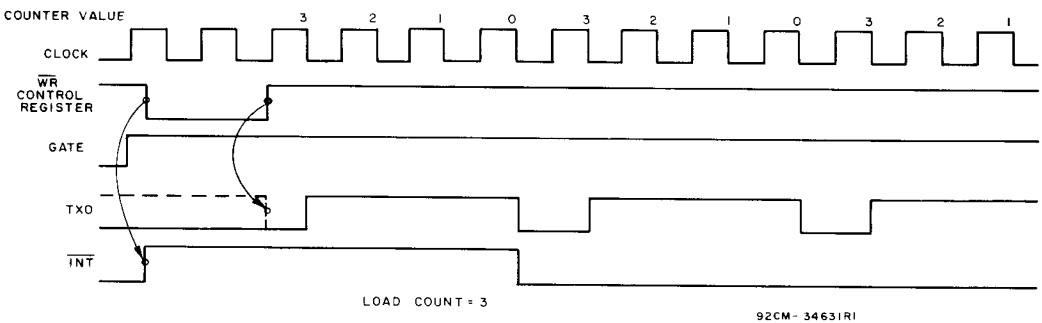


Fig. 5 - Rate generators (mode 4) timing waveforms.

Mode		Control Register	Gate Control
5	Variable Duty Cycle	X X X X X 1 0 1 BUS 7 BUS 0	Selectable High or Low Level Enables Operation

Mode 5:

After the mode is initiated, the outputs will remain at one level until the clock decrements the least significant byte of the counter to N+1. The outputs will then change level and the counter decrements the most significant byte to N+1. The process will then repeat, resulting in a repetitive output with a duty cycle directly controlled by the value in the counter. The output period will be equal to LSB+MSB+2.

The interrupt output will become active after the MSB is loaded into the counter and decrements to zero.

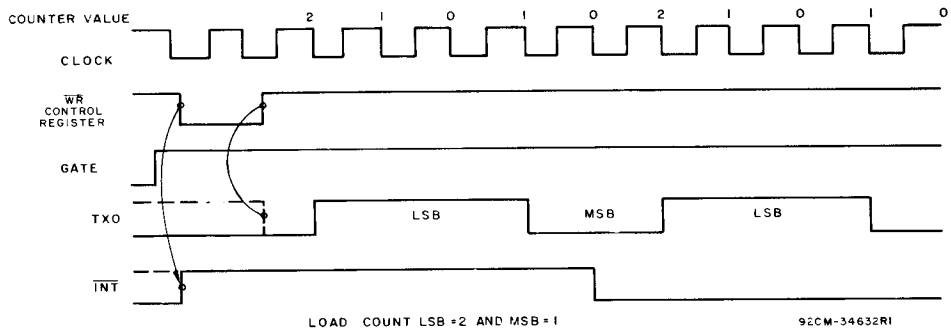


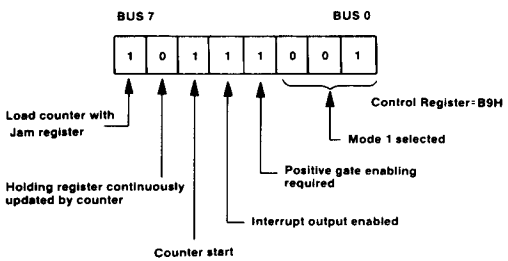
Fig. 6 - Variable-duty cycle (mode 5) timing waveforms.

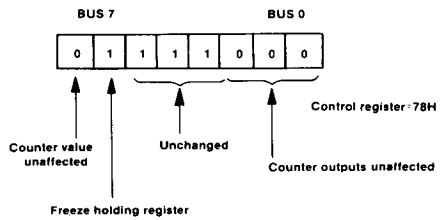
Setting the Control Register

The following will illustrate a counter write and subsequent reads that places stable, accurate values on the data bus from the counter-timer.

The counter is addressed and the required values are loaded into the jam register with two write operations. The control register is addressed next and loaded with B9H.

The counter will now decrement with each input clock pulse. Assuming the counter has not decremented to zero and its value is to be read without affecting the counter's operation, a write to the control register is performed. 78H is loaded into the control register.





The counter is addressed and read operations are performed.

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Function Pin Definition

DB7-DB0 — 8 bit bidirectional bus used to transfer binary information between the microprocessor and the dual counter-timer.

VDD, VSS — Power and ground for device.

A0, A1, and A2 — Addresses used to select counters or registers.

AS — Address Strobe, the addresses on Pins A0, A1, and A2 are latched by the trailing edge of the signal on the address strobe pin.

Mode — Controls data transfer to and from counter-timer. The level on this pin determines the operation of the RD/$\overline{RD}$ and DS/$\overline{WR}$ signals.

RD/$\overline{RD}$ and DS/$\overline{WR}$ — A low level on the mode pin places the device in mode = 0. This mode is used when an 8085 type processor is interfaced to the counter-timer. Active low signals enable the pin functions. The device is written to when DS/$\overline{WR}$ is low. Data is latched on the trailing edge (low to high transition); RD/$\overline{RD}$ must be high. Read operations occur when RD/$\overline{RD}$ is low; DS/$\overline{WR}$ must remain high.

A high level on the mode select pin places the device in mode = 1. This mode selects the CDP6805 processor interface. Write cycles are performed when DS/$\overline{WR}$ is high and data is latched on the trailing edge of the signal (high to low transition); RD/$\overline{RD}$ must be low. Read operations occur when DS/$\overline{WR}$ is high; RD/$\overline{RD}$ must be high.

Note: All read and write cycles require that a valid address was latched and CS is high.

TACL, TBCL — Clocks used to decrement the counter.

TAG, TBG — Gate inputs used to control counter.

TAO, $\overline{TAO}$ — Complemented outputs of Timer A.

TBO, $\overline{TBO}$ — Complemented outputs of Timer B.

$\overline{INT}$ — Common interrupt output. Active when counter decrements to zero.

$\overline{RESET}$ — Active low signal that resets counter outputs (TAO, TBO low, $\overline{TAO}$, $\overline{TBO}$ high). The interrupt output is set high and the status register is cleared.

CS — Chip Select, an active high signal that enables the device. It is not latched.

BUS TIMING (V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted), see Figs. 8 and 10.

IDENTIFIER NO.	CHARACTERISTIC		MIN.	MAX.	UNITS
(1)	Cycle Time	t_{cyc}	953	DC	ns
(3)	Pulse Width DS/$\overline{WR}$ or RD/$\overline{RD}$ Low	PWEH	325	—	
(4)	Clock Rise and Fall Time	tr, tf	—	30	
(8)	R/$\overline{W}$ Hold Time	tRWH	10	—	
(13)	R/$\overline{W}$ Setup Time Before DS/$\overline{WR}$	tRWS	15	—	
(14)	Chip Select to Valid Read Data	tACS	400	—	
(15)	Chip Select Hold Time	tCH	0	—	
(18)	Read Data Hold Time	tDHR	10	350	
(21)	Write Data Hold Time	tDHW	50	—	
(24)	Muxed Address Valid Time to AS/ALE Fall	tASL	60	—	
(25)	Muxed Address Hold Time	tAHL	50	—	
(27)	Pulse Width AS/ALE High	PWASH	100	—	
(28)	Delay Time AS/ALE to DS/$\overline{WR}$ Rise	tASED	90	—	
(30)	Peripheral Output Data Delay Time From DS/$\overline{WR}$ or $\overline{RD}$	tDDR	20	400	
(31)	Peripheral Data Setup Time	tDSW	100	—	

Note: Designations ALE, $\overline{RD}$ and $\overline{WR}$ refer to signals from non-6805 type microprocessors.

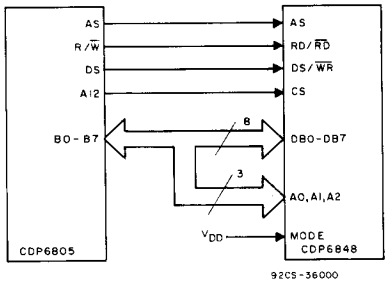


Fig. 7 - Typical CDP6805 system using the CDP6848.

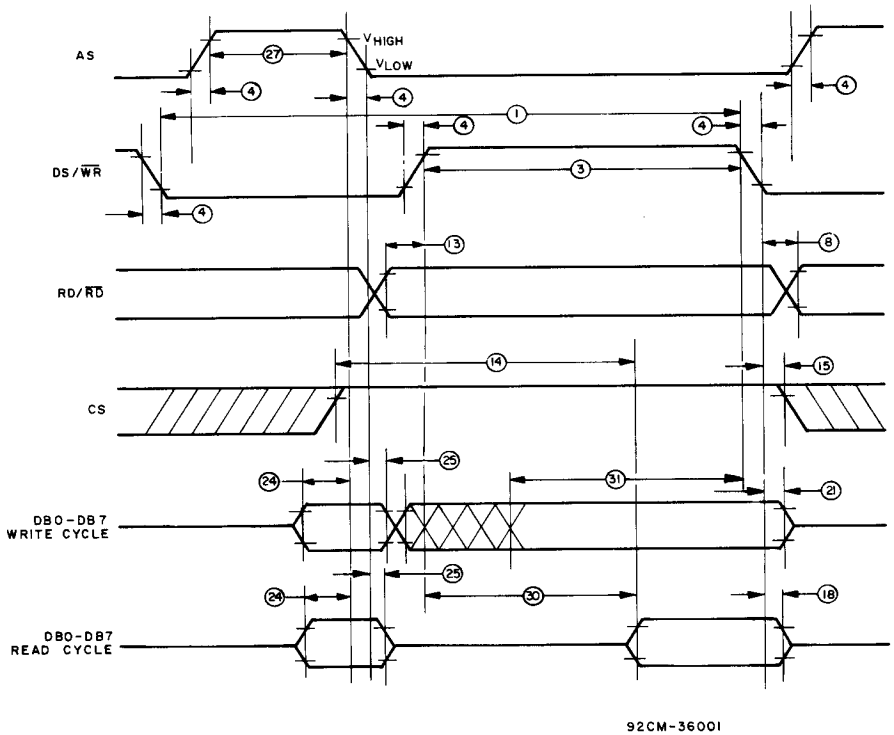


Fig. 8 - Bus timing waveforms.

CDP6848, CDP6848C

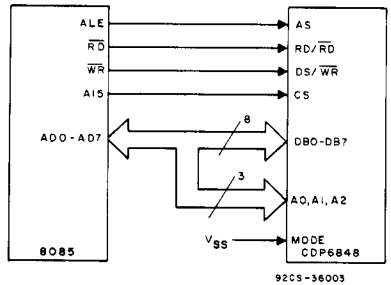


Fig. 9 - Typical 8085 system using the CDP6848.

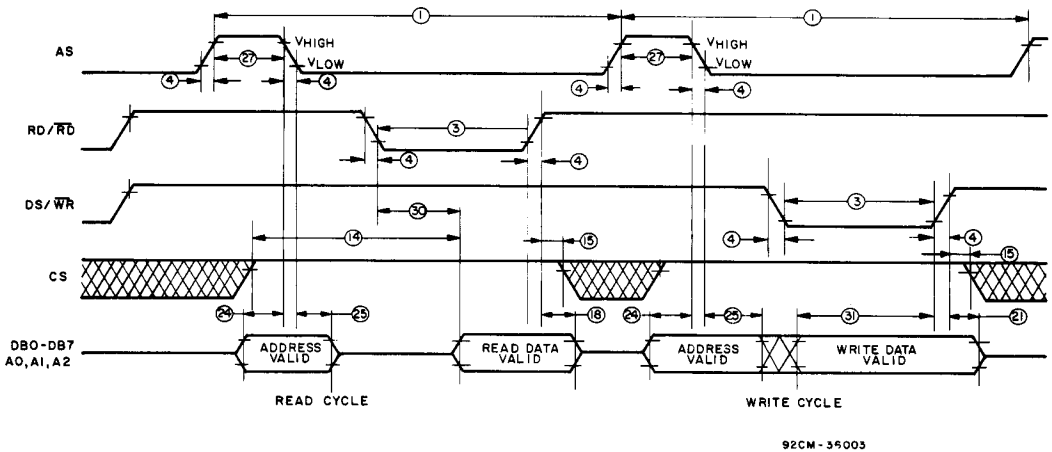


Fig. 10 - Bus timing waveforms.

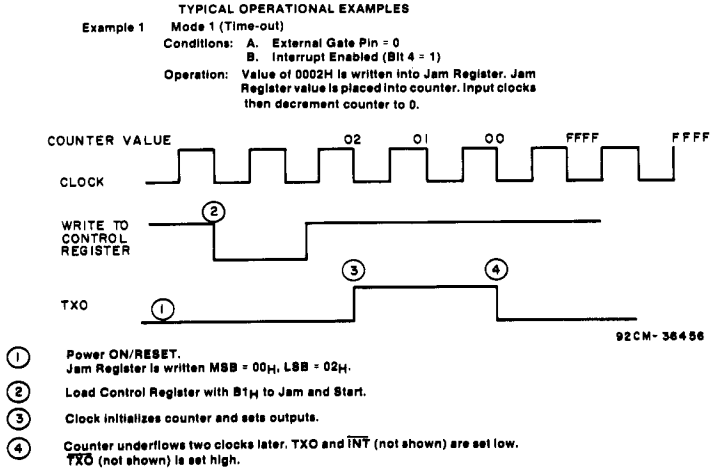


Fig. 11 - Timeout (mode 1) timing waveforms.

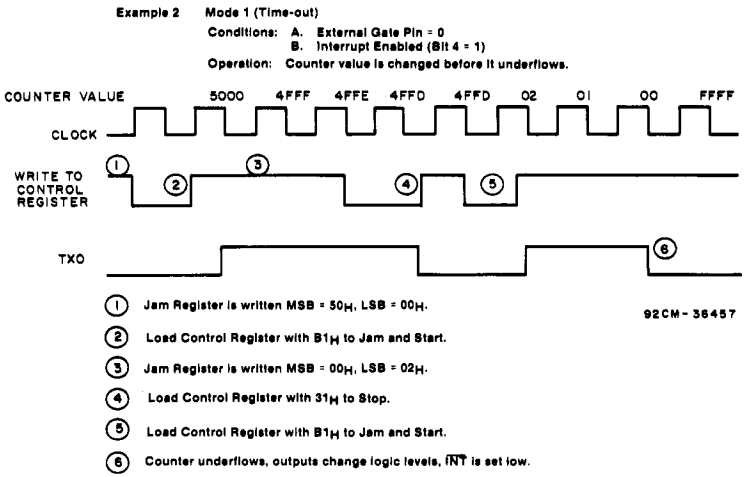


Fig. 12 - Timeout (mode 1) timing waveforms.

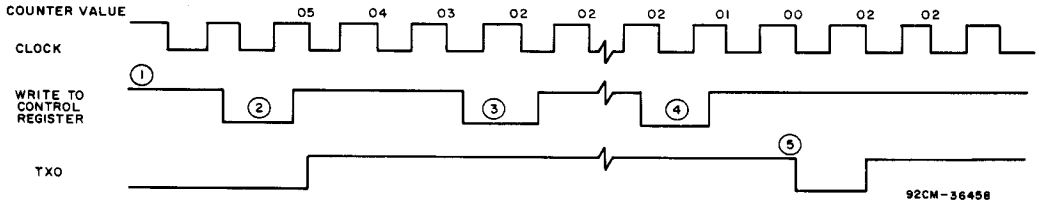
CDP6848, CDP6848C

TYPICAL OPERATION EXAMPLES (Cont'd)

Example 3 Mode 2 (Time-out Strobe)

Conditions: A. External Gate Pin = 1
B. Interrupt Disabled (Bit 4 = 0)

Operation: Before counter underflows, it is stopped and restarted without changing its value.



(1) Jam Register is written MSB = 00_H, LSB = 05_H.

(2) Load Control Register with AA_H.

(3) Load Control Register with 08_H. Start/Stop Bit 5 = 0.

(4) Load Control Register with 28_H.

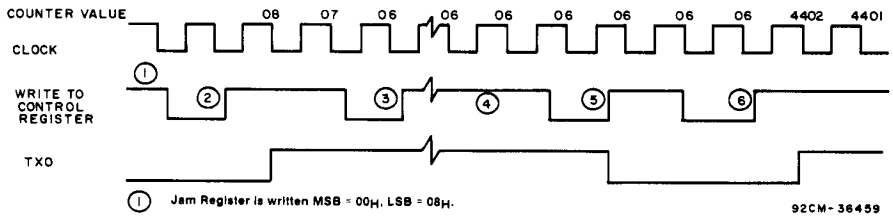
(5) Counter underflows and returns high on next clock.

Fig. 13 - Timeout strobe (mode 2) timing waveforms.

Example 4 Mode 2 (Time-out Strobe)

Conditions: A. External Gate Pin = 1
B. Interrupt Disabled (Bit 4 = 0)

Operation: Counter is stopped and a new Jam Register value is placed in counter before it underflows.



(1) Jam Register is written MSB = 00_H, LSB = 08_H.

(2) Load Control Register with AA_H.

(3) Load Control Register with 08_H. Counter is stopped.

(4) Jam Register is loaded MSB = 44_H, LSB = 02_H.

(5) Load Control Register with $2A_H$ to Stop.

(6) Load Control Register with AA_H. Counter is Enabled to Jam and Start.

Fig. 14 - Timeout strobe (mode 2) timing waveforms.

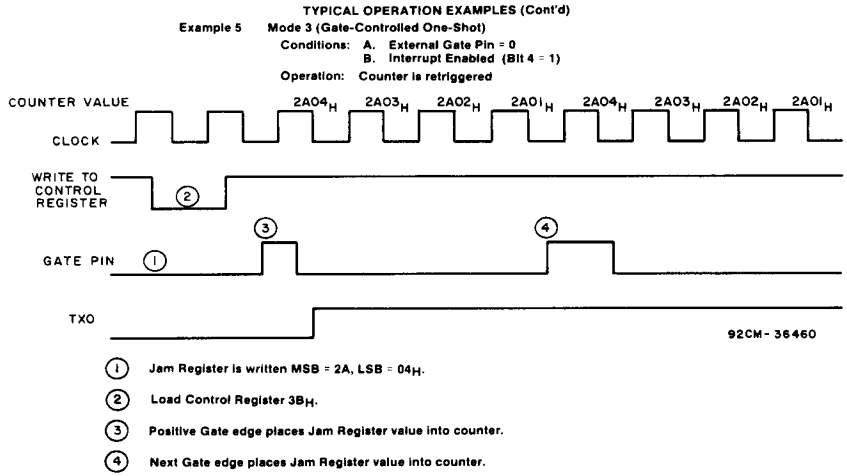


Fig. 15 - Gate controlled one-shot (mode 3) timing waveforms.