DG884

Siliconix incorporated

T-51-11

8 x 4 Wideband/Video Crosspoint Array

SILICONIX INC

FEATURES

- 8 Inputs, 4 Outputs
- Wide Bandwidth (300 MHz)
- Very Low Crosstalk (–85 dB @ 5 MHz)
- On-Board TTL-compatible Latches with Readback
- Optional Negative Supply Input
- Low $r_{DS(ON)}$ (90 Ω max)
- ESD Protection > ±4000 V

BENEFITS

- Reduced Board Space
- Improved System Bandwidth
- Improved Channel Off-isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss

APPLICATIONS

- Wideband Signal Routing and Multiplexing
- High-end Video Systems
- µP-controlled Systems
- Direct Coupled Systems
- ATE Systems
- Digital Video Routing

DESCRIPTION

The DG884 is a digitally selectable 8 x 4 crosspoint array designed for wideband operation. On-chip TTL-compatible crosspoint selection logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low ON resistance and low capacitance of the DG884 make it ideal for wideband data multiplexing and video and audio signal routing in analog and/or digital video systems. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

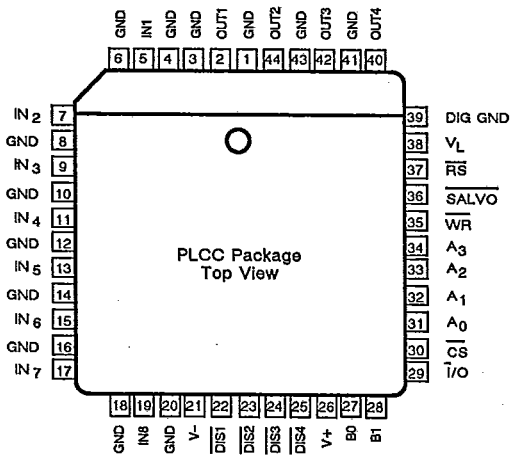
The DG884 is built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of OFF isolation. Crosstalk is reduced to –85 dB at 5 MHz on the DG884 by including a ground line between each adjacent signal path.

The DG884 is available in 44-pin leaded chip carrier and 40-pin DIP packages for operation over the industrial, D suffix (–40 to 85°C) temperature range, and for military, A suffix (–55 to 125°C) operation.

PIN CONFIGURATION

DG884 Quad J-Lead Packages

Order Numbers:
PLCC-44: DG884DN
CLCC-44: DG884AM



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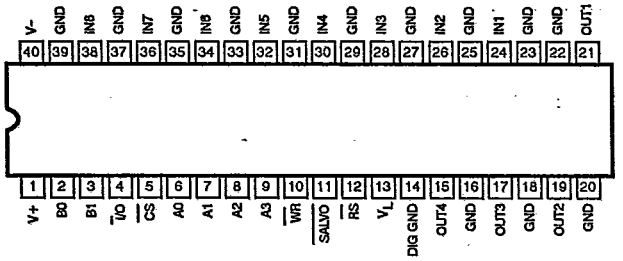
PIN CONFIGURATION

T-51-11

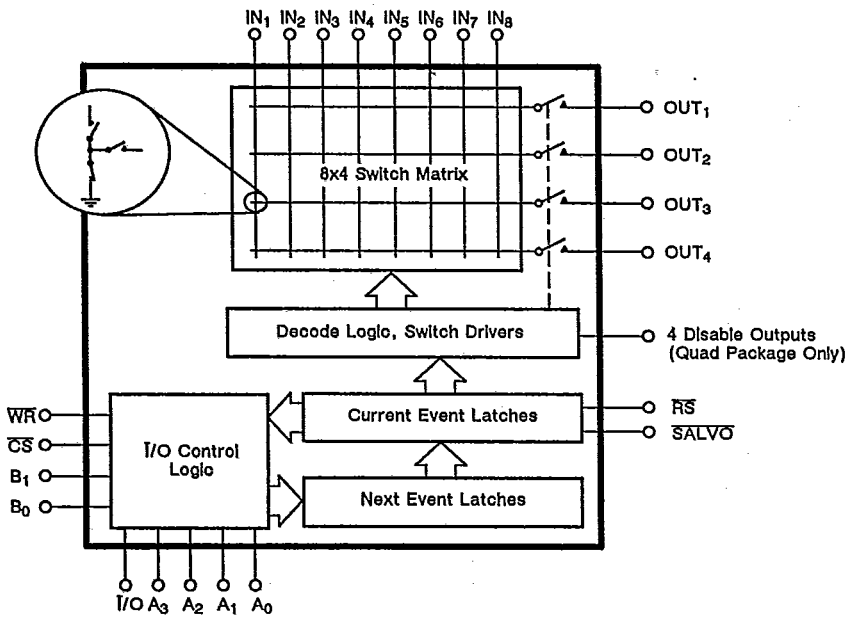
DG884 Dual-In-Line Package

Order Numbers:
Plastic: DG884DJ
Side Braze: DG884AP



FUNCTIONAL BLOCK DIAGRAM

DG884 Block Diagram



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TRUTH TABLE

$\overline{RS}$	I/O	$\overline{CS}$	$\overline{WR}$	$\overline{SALVO}$	ACTIONS
1	0	X	1	0	Data in all next event latches is simultaneously loaded into the current event latches, i.e., all new crosspoint addresses change simultaneously when $\overline{SALVO}$ goes low (↓)
1	0	1	0	1	No Change
1	0	0	0	1	Next event latches loaded as defined in table below
1	1	1	1	1	A_0, A_1, A_2, A_3 – High Impedance
1	1	0	1	1	A_0, A_1, A_2, A_3 become outputs and reflect the contents of the current event latches. B_0, B_1 determine which current event latches are being read
0	X	X	1	1	All crosspoints opened
1	0	0	0	X	Next event latches are transparent
1	0	0	X	0	Current event latches are transparent
1	0	0	0	0	Both next and current event latches are transparent

ALL OTHER STATES ARE NOT ALLOWED

NOTE: when $\overline{WR}$ = 0 next event latches are transparent
when $\overline{WR}$ = ↑ data in next event latches is latched in

NEXT EVENT LATCHES TRUTH TABLE

$\overline{WR}$	B_1	B_0	A_2	A_1	A_0	A_3	NEXT EVENT LATCHES
0	0	0	0	0	0	1	IN_1 to OUT_1 Loaded
			0	0	1		IN_2 to OUT_1 Loaded
			0	1	0		IN_3 to OUT_1 Loaded
			0	1	1		IN_4 to OUT_1 Loaded
			1	0	0		IN_5 to OUT_1 Loaded
			1	0	1		IN_6 to OUT_1 Loaded
			1	1	0		IN_7 to OUT_1 Loaded
			1	1	1		IN_8 to OUT_1 Loaded
			X	X	X	0	Turn Off OUT_1 Loaded
	0	1	0	0	0	1	IN_1 to OUT_2 Loaded
			0	0	1		IN_2 to OUT_2 Loaded
			0	1	0		IN_3 to OUT_2 Loaded
			0	1	1		IN_4 to OUT_2 Loaded
			1	0	0		IN_5 to OUT_2 Loaded
			1	0	1		IN_6 to OUT_2 Loaded
			1	1	0		IN_7 to OUT_2 Loaded
			1	1	1		IN_8 to OUT_2 Loaded
			X	X	X	0	Turn Off OUT_2 Loaded
	1	0	0	0	0	1	IN_1 to OUT_3 Loaded
			0	0	1		IN_2 to OUT_3 Loaded
			0	1	0		IN_3 to OUT_3 Loaded
			0	1	1		IN_4 to OUT_3 Loaded
			1	0	0		IN_5 to OUT_3 Loaded
			1	0	1		IN_6 to OUT_3 Loaded
			1	1	0		IN_7 to OUT_3 Loaded
			1	1	1		IN_8 to OUT_3 Loaded
			X	X	X	0	Turn Off OUT_3 Loaded
	1	1	0	0	0	1	IN_1 to OUT_4 Loaded
			0	0	1		IN_2 to OUT_4 Loaded
			0	1	0		IN_3 to OUT_4 Loaded
			0	1	1		IN_4 to OUT_4 Loaded
			1	0	0		IN_5 to OUT_4 Loaded
			1	0	1		IN_6 to OUT_4 Loaded
			1	1	0		IN_7 to OUT_4 Loaded
			1	1	1		IN_8 to OUT_4 Loaded
			X	X	X	0	Turn Off OUT_4 Loaded

ABSOLUTE MAXIMUM RATINGS

T-51-11

V+ to GND ..... -0.3 V to +19 V
V+ to V- ..... -0.3 V to +19 V
V- to GND ..... -10 V to +0.3 V
Digital Inputs ..... (V- minus 0.3 V) to (V+ plus 0.3 V) or 20 mA, whichever occurs first
V_S, V_D ..... (V- minus 0.3 V) to (V- plus 14 V) or 20 mA, whichever occurs first
CURRENT (any terminal) Continuous ..... 20 mA
CURRENT (S or D) Pulsed 1 ms 10% duty ..... 40 mA

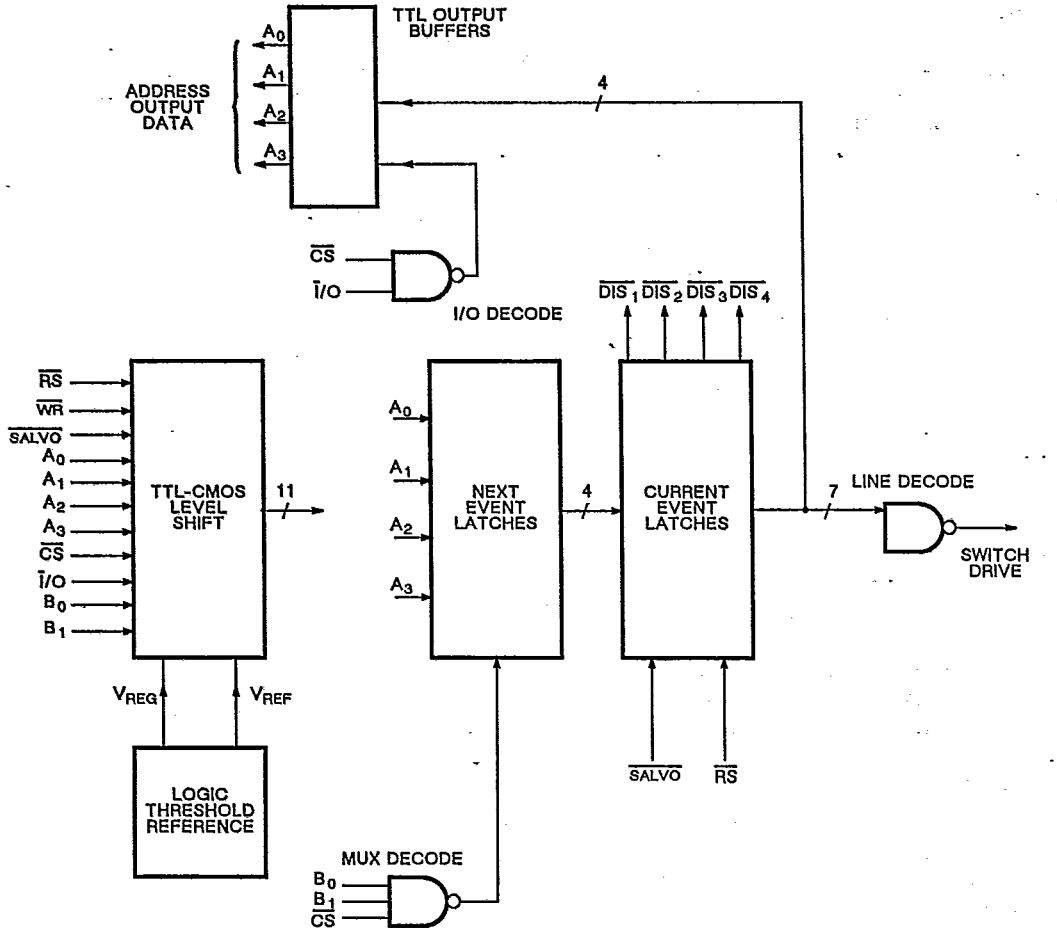
Storage Temperature (A Suffix) .....-65 to 150°C
(D Suffix) .....-65 to 125°C

Operating Temperature (A Suffix) .....-55 to 125°C
(D Suffix) .....-40 to 85°C

Power Dissipation (Package)*
40-Pin Plastic DIP** ..... 625 mW
40-Pin Side Braze DIP*** ..... 1200 mW
44-Pin Quad J Lead Plastic**** ..... 450 mW
44-Pin Quad J Lead Hermetic*** ..... 1200 mW

* All leads welded or soldered to PC board.
** Derate 8.3 mW/°C above 75°C
*** Derate 16 mW/°C above 75°C
**** Derate 6 mW/°C above 75°C

CONTROL CIRCUITRY



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ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −3 V, V_L = +5 V, GND = 0 V, $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, $\overline{I/O}$ = 0.8 V, $\overline{RS}$ = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=−55,−40°C		A SUFFIX −55 to 125°C		D SUFFIX −40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Analog Signal Range*	V_{ANALOG}	V− = −5 V	1		−5	8	−5	8	V
Drain – Source ON Resistance	$r_{DS(ON)}$	I_S = −10 mA, V_S = 0 V, V_{AIL} = 0.8 V, V_{AIH} = 2.4 V, Sequence each switch ON	1,3	45		90		90	Ω
			2			120		120	
Resistance Match Between Channels	$\Delta r_{DS(ON)}$		1			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 8 V, V_D = 0 V, $\overline{RS}$ = 0.8 V	1		−20	20	−20	20	nA
			2,3		−200	200	−200	200	
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = 0 V, V_D = 8 V, $\overline{RS}$ = 0.8 V	1		−20	20	−20	20	
			2,3		−200	200	−200	200	
Total Switch ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_S = V_D$ = 8 V	1		−20	20	−20	20	
			2,3		−2000	2000	−200	200	
DIGITAL INPUT/OUTPUT									
$\overline{DIS}$ Pin Sinking	I_{DIS}		1	1.5					mA
Address Output Current	I_{AO}	V_{AO} = 2.7 V	1,2,3		−200		−200		µA
		V_{AO} = 0.4 V	1,2,3			400		400	
Input Voltage High	V_{AIH}		1,2,3		2		2		V
Input Voltage Low	V_{AIL}		1,2,3			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V or 2 V or 15 V	1,3	0.1	−1	1	−1	1	µA
			2		−10	10	−10	10	
DYNAMIC									
ON State Input Cap.[c]	$C_{S(ON)}$	See Figure 11, 1 in, 4 out		120				160	pF
		1 in, 1 out						40	
OFF State Input Cap.[c]	$C_{S(OFF)}$	See Figure 12	1	8		20		20	
OFF State Output Cap.[c]	$C_{D(OFF)}$		1	10		20		20	
Break-Before-Make Interval	t_{OPEN}	See Figure 4	1,2,3			10		10	ns
$\overline{SALVO}$ Turn ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, 50% Control to 90% Output, See Figure 2	1,3			300		300	
			2			500		500	
$\overline{SALVO}$ Turn OFF Time	t_{OFF}		1,3			150		150	
			2			300		300	

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ELECTRICAL CHARACTERISTICS [a]

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PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −3 V, V_L = +5 V, GND = 0 V, $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, $\overline{I/O}$ = 0.8 V, $\overline{RS}$ = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP	TYP[d]	A SUFFIX −55 to 125°C MIN[b]	A SUFFIX −55 to 125°C MAX[b]	D SUFFIX −40 to 85°C MIN[b]	D SUFFIX −40 to 85°C MAX[b]	UNIT
DYNAMIC (Cont'd)									
Charge Injection	Q	See Figure 5	1	−100					pC
Matrix Disabled Crosstalk (See Figure 8)	$XTALK_{(DIS)}$	R_{IN} = R_L = 75 Ω, f = 5 MHz	1	−82					dB
Adjacent Input Crosstalk (See Figure 9)	$XTALK_{(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	1	−85					dB
All Hostile Crosstalk (See Figure 7)	$XTALK_{(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	1	−60					dB
Bandwidth	BW	R_L = 50 Ω, See Figure 6	1	300					MHz
SUPPLY									
Positive Supply Current	I+		1,2 3	1.5		3 6		3 6	mA
Negative Supply Current	I−		1,2 3	−1.5	−3 −5		−3 −5		mA
Digital GND Supply Current	I_{DG}	All Channels ON or OFF with address inputs at GND or V+	1,2,3	−275	−750		−750		µA
Logic Supply Current	I_L		1,2,3	200		500		500	µA
Functional Check of Max Operating Supply Voltage Range	V+ to V−	See Figure 10 Functional Test Only	1,2,3		13	18	13	18	V
	V− to GND		1,2,3		−5.5	−3	−5.5	−3	V
	V+ to GND		1,2,3		10	15	10	15	V
TIMING									
Write Data Time	t_{WD}	See Figure 1	1,2,3		50				ns
Minimum Pulse Width	t_{MPW}		1,2,3		200				ns
Data Write Time	t_{DW}		1,2,3		100				ns
Chip Select Valid Time	t_{CSV}		1,2,3		100				ns
Chip Select Hold Time	t_{CSH}		1,2,3		100				ns
Minimum $\overline{SALVO}$ Width	t_{MSW}		1,2,3		200				ns

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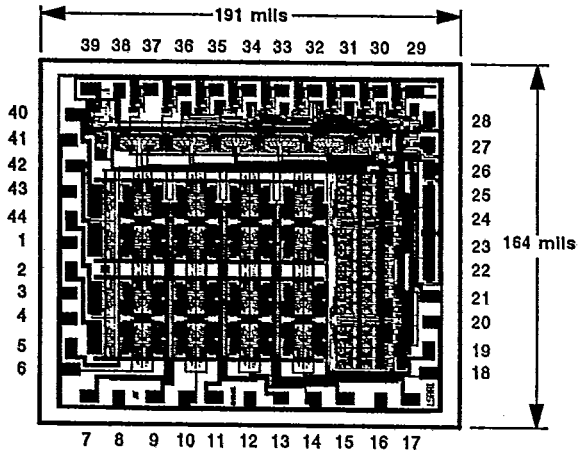
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -3 V, V_L = +5 V, GND = 0 V, $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, I/O = 0.8 V, $\overline{RS}$ = 2.4 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
TIMING (Cont'd)									
SALVO Hold Time	t_{SH}	See Figure 1	1,2,3		200		200		ns
Input Output Time	t_{IO}		1		200		200		
Address Output Time	t_{AO}		1		200		200		
Reset/Write Time	t_{RW}		1,2,3		50		50		
Address Tristate Time	t_{AZ}		1	50					
Address Input Time	t_{AI}		1		200		200		

NOTES: a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY at 25°C, not guaranteed nor subject to production testing.
e. Analog signal range is measured from the GND pin to the designated Source (input) pin, and indicates the limits of functionality. Performance limits are only guaranteed for stated test conditions.

DIE TOPOGRAPHY



LSAA-1
728 PMOS Transistors
3 p+ resistors
3 NPN Transistors
821 NMOS Transistors
20 diodes

Pad No.	Function	Pad No.	Function
1	GND	31	A0
2	OUT1	32	A1
3	GND	33	A2
4	GND	34	A3
5	IN1	35	$\overline{WR}$
6	GND	36	$\overline{SALVO}$
7	IN2	37	$\overline{RS}$
8	GND	38	V_L
9	IN3	39	GND
10	GND	40	OUT4
11	IN4	41	GND
12	GND	42	OUT3
13	IN5	43	GND
14	GND	44	OUT2
15	IN6		
16	GND		
17	IN7		
18	GND		
19	IN8		
20	GND		
21	V- (Substrate)		
22	DS1		
23	DS2		
24	DS3		
25	DS4		
26	V+		
27	B0		
28	B1		
29	I/O		
30	$\overline{CS}$		

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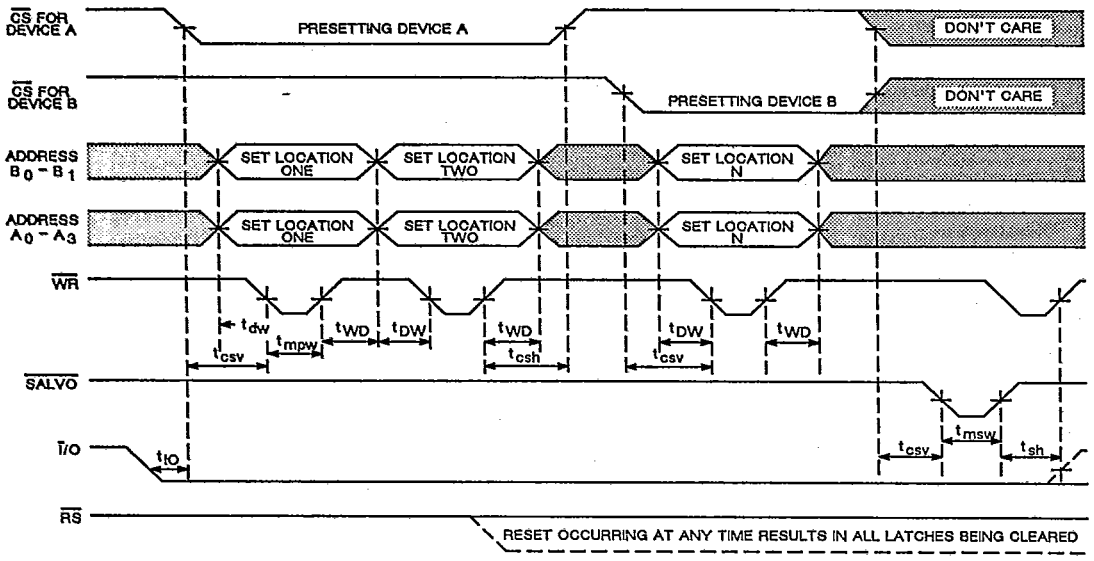
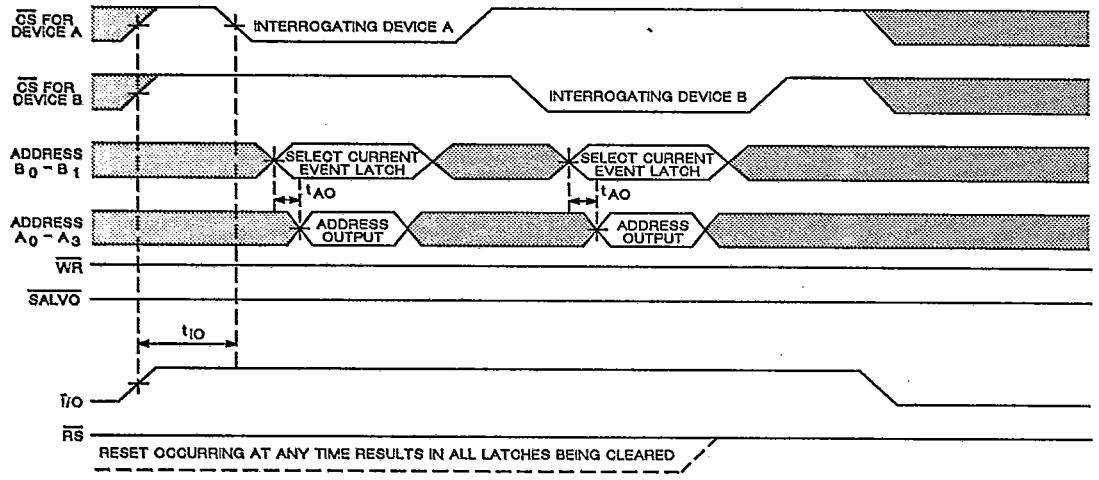


Input Timing Requirements



Address Output Timing Requirements

Figure 1

2

SALVO TURN ON/OFF TIME TEST CIRCUIT

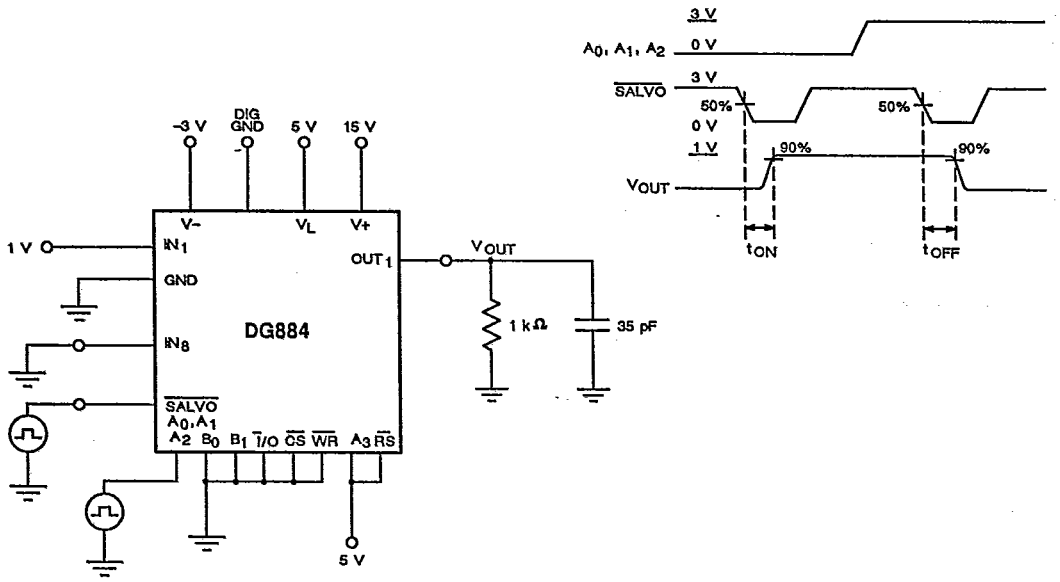


Figure 2

WR TURN ON TIME TEST CIRCUIT

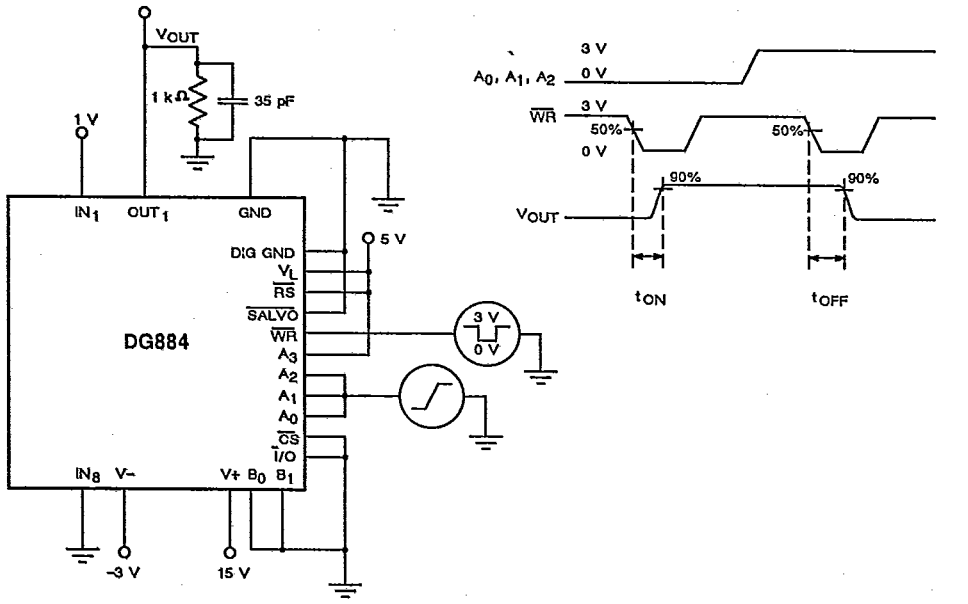


Figure 3

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TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT

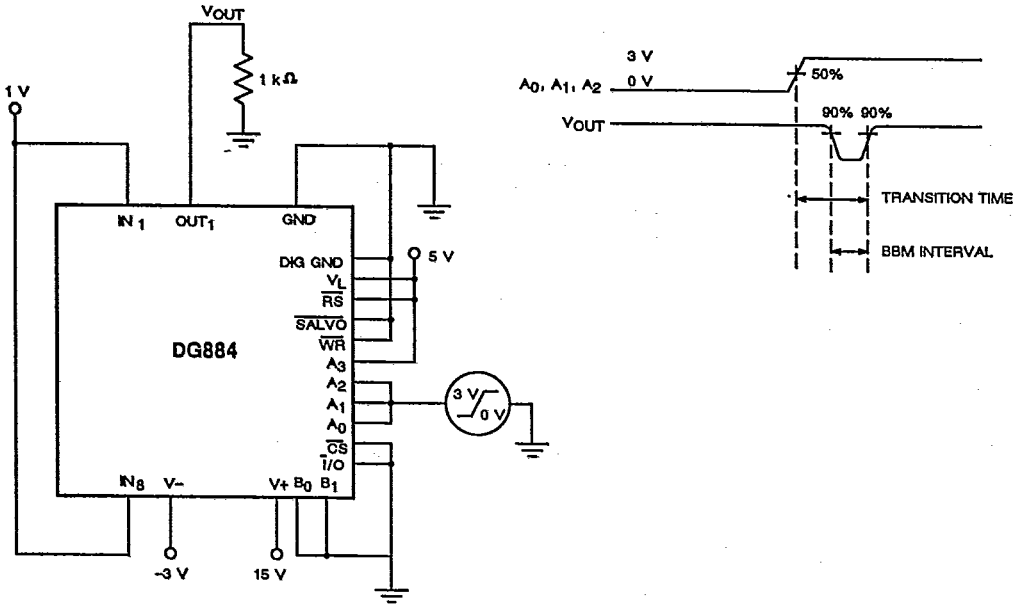


Figure 4

CHARGE INJECTION TEST CIRCUIT

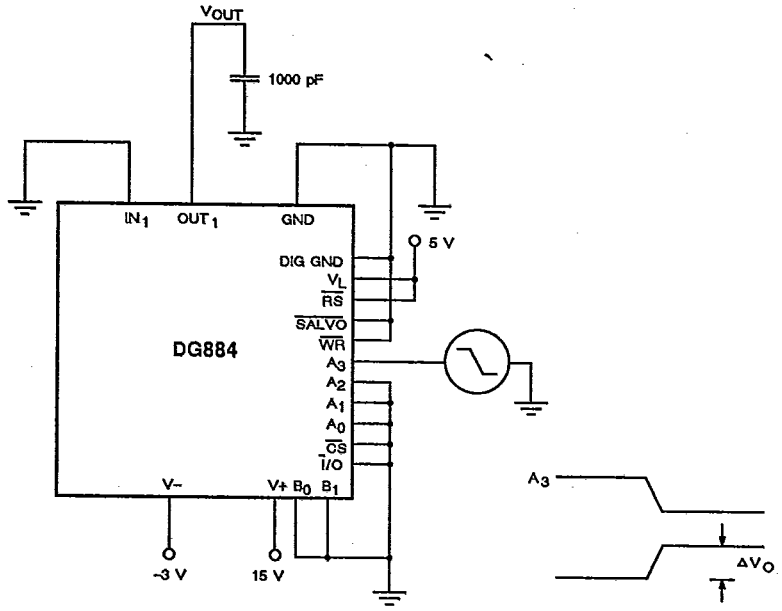


Figure 5

-3 dB BANDWIDTH TEST CIRCUIT

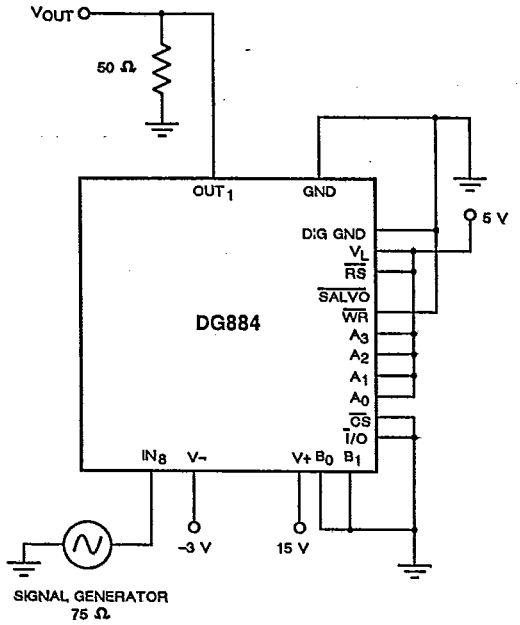


Figure 6

ALL HOSTILE CROSSTALK – XTALK (AH)

Any one input to any one output
All remaining inputs connected to remaining outputs
IN_2 to OUT_2, IN_3 to OUT_3 etc.

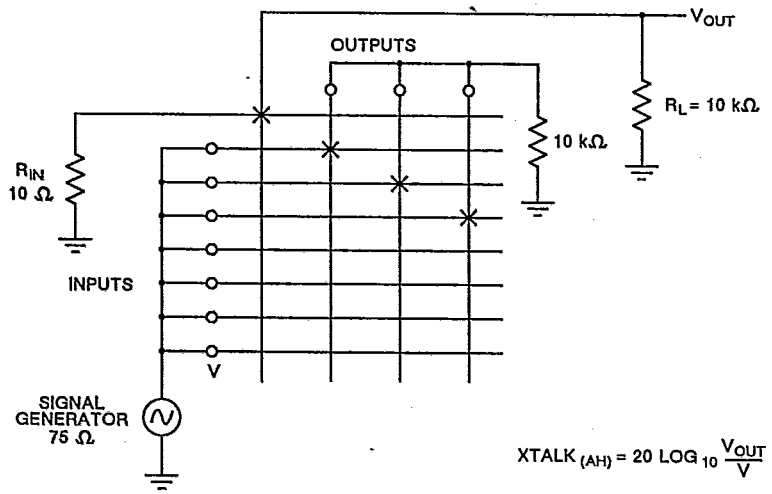


Figure 7

MATRIX DISABLED CROSSTALK – XTALK (DIS)

All crosspoints open

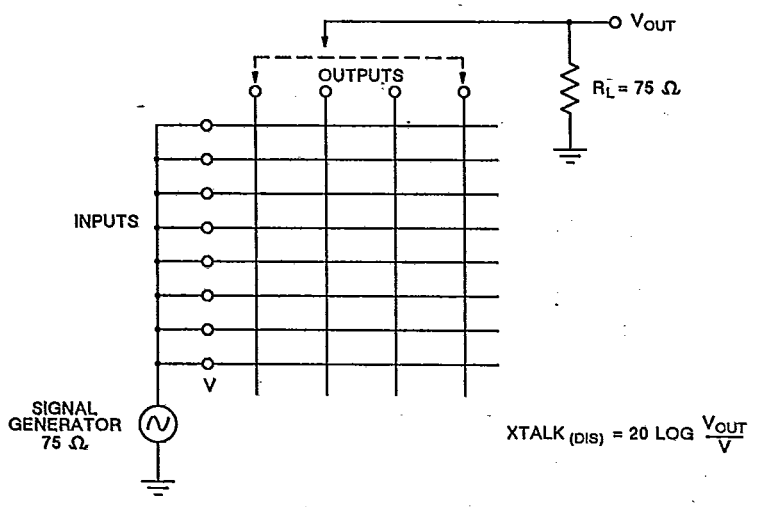


Figure 8

ADJACENT INPUT CROSSTALK – XTALK (AI)

Any input or output pin to adjacent input or output pin

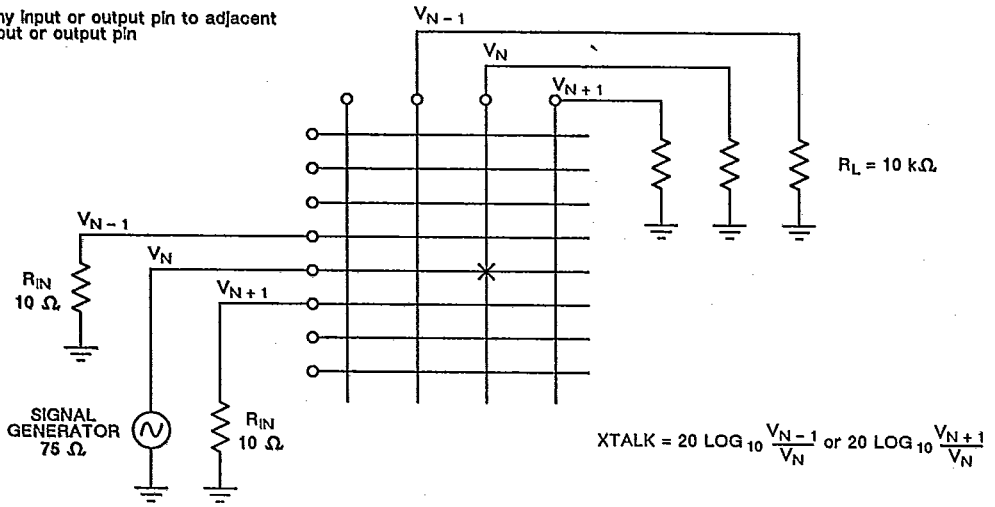


Figure 9

2

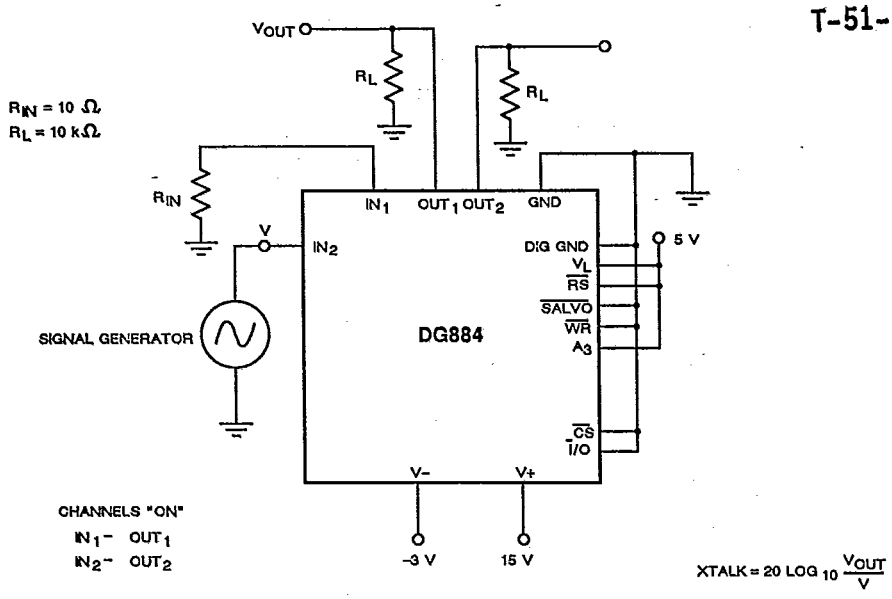


Figure 10

ON STATE INPUT CAPACITANCE

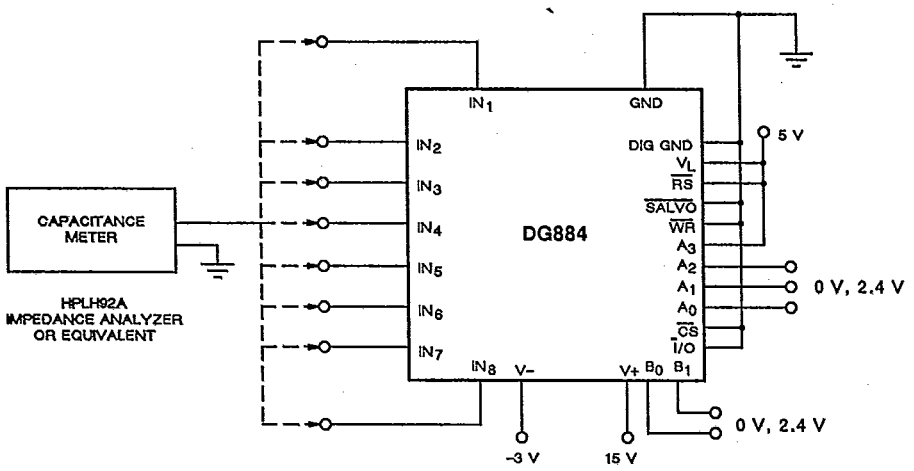


Figure 11

OFF STATE INPUT/OUTPUT CAPACITANCE

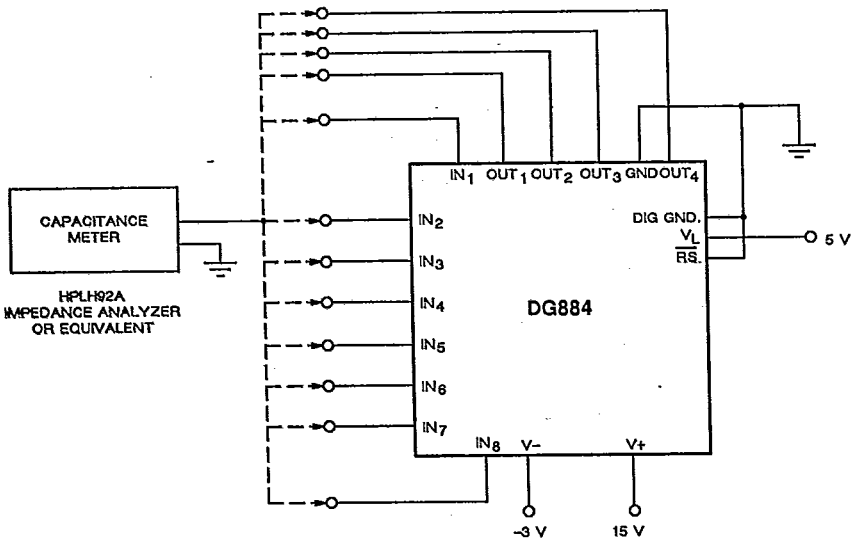
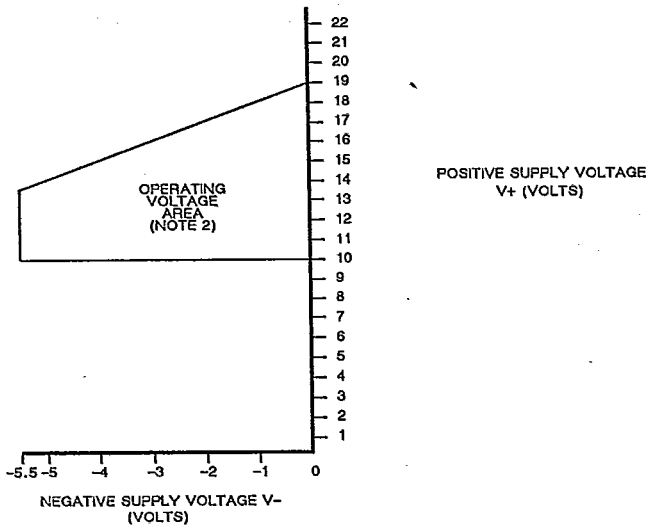


Figure 12

OPERATING VOLTAGE RANGE

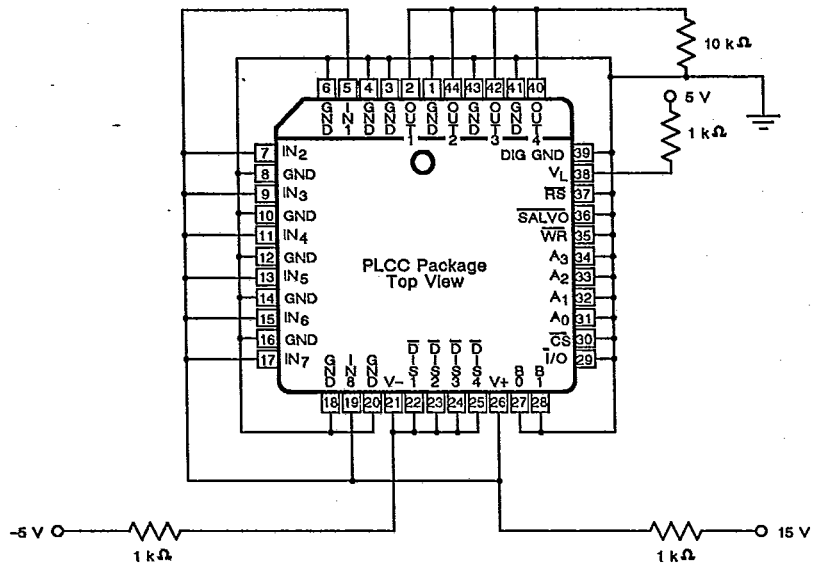


Note:
1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10µF tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V. Readback function for V- ≤ -3 V only.
3. At V_L = 5 V ± 10%, 0.8/2.0 V TTL compatibility is maintained over the entire operating voltage range.

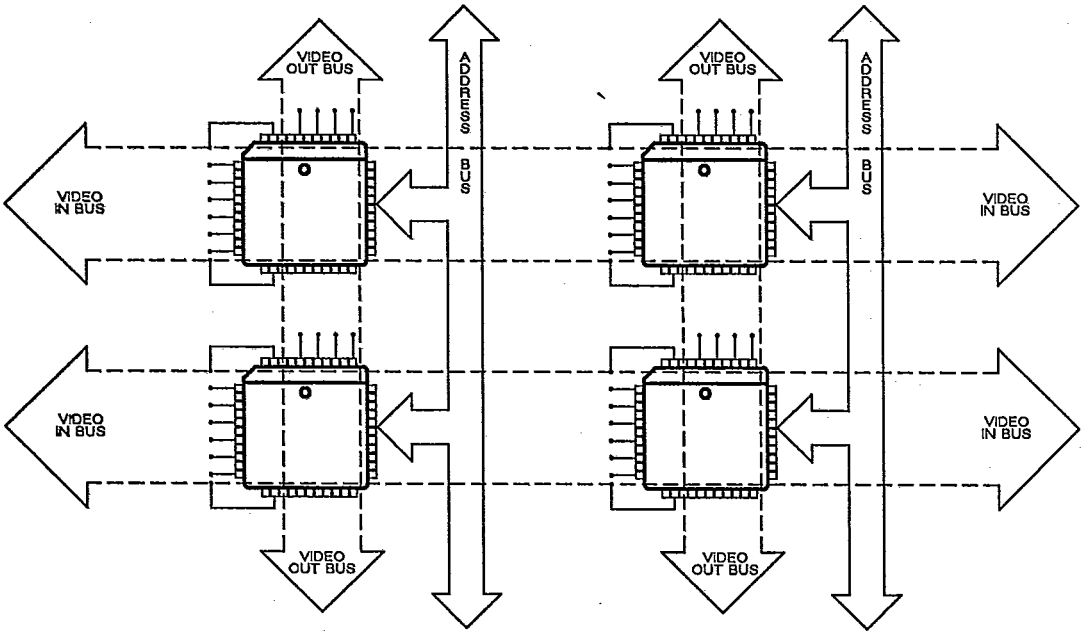
Figure 13

2

BURN-IN CIRCUIT – 44-LEAD PLCC



APPLICATIONS



16 x 8 EXPANDABLE CROSSPOINT MATRIX USING DG884

Preliminary

PIN DESCRIPTION (PLCC-44)

T-51-11

SYMBOL	PIN NUMBER PLCC 44	PIN NUMBER DIP PACKAGE	DESCRIPTION
GND	1,3,4,6,8,10,12, 14,16,18,20,41,43	16,18,20,22,23 25,27,29,31,33 35,37,39	Analog Signal Ground
DIG GND	39	14	Digital Ground
V+	26	1	Positive Supply Voltage
V–	21	40	Negative Supply Voltage
V_L	38	13	Logic Supply Voltage
IN_1 to IN_8	5,7,9,11, 13,15,17,19	24,26,28,30 32,34,36,38	Analog Input Channels
OUT_1 to OUT_4	2,40,42,44	21,19,17,15	Analog Output Channels
I/O	29	4	Pin that determines whether data is being written into the next event latches or read from the current event latches
$\overline{CS}$	30	5	Chip Select
A_0,A_1,A_2,A_3	31,32,33,34	6,7,8,9	Input Address Bus
B_0,B_1	27,28	2,3	Output Address Bus
$\overline{WR}$	35	10	Write command that latches A_0, A_1, A_2, A_3 into the next event latches
$\overline{SALVO}$	36	11	Master write command that in one action transfers all the data from next event latches into current event latches
$\overline{RS}$	$\overline{DIS}_1$ thru $\overline{DIS}_4$ 37	12	Reset
$\overline{DIS}_1$ thru $\overline{DIS}_4$	22,23,24,25	Not Available	Disable outputs to power down external video buffers

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