

DN74LS01 *DN74LS41*

Quad 2-input Positive NAND Gates (with Open Collector Outputs)

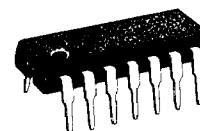
■ Description

DN74LS01 contains four 2-input positive isolation NAND gate circuits with open collector outputs.

■ Features

- "Wired" AND capability
- Low power consumption ($P_d = 8\text{mW}$ typical)
- High speed ($t_{pd} = 16\text{ns}$ typical)
- Wide operating temperature range ($T_a = -20$ to $+75^\circ\text{C}$)

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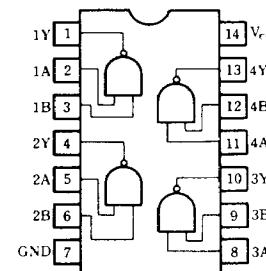


14-pin plastic DIL package

P-4



14-pin Panaflat package (SO-14D)

Pin configuration (top view)**■ Recommended operating conditions**

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.75	5.00	5.25	V
HIGH level output voltage	V _{OH}			5.5	V
LOW level output voltage	I _{OL}			8	mA
Operating temperature range	T _{opr}	-20	25	75	°C

4 R

■ DC characteristics ($T_a = -20 \sim +75^\circ\text{C}$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output voltage	V_{OL1}	$V_{CC} = 4.75\text{V}$	$I_{OL} = 4\text{mA}$		0.25	0.4	V
	V_{OL2}	$V_{IH} = 2\text{V}$	$I_{OL} = 8\text{mA}$		0.35	0.5	V
Input current	I_{IH}	$V_{CC} = 5.25\text{V}$	$V_I = 2.7\text{V}$			20	μA
	I_{IL}	$V_{CC} = 5.25\text{V}$	$V_I = 0.4\text{V}$			-0.4	mA
	I_J	$V_{CC} = 5.25\text{V}$	$V_I = 7\text{V}$			0.1	mA
Output current	I_{OH}	$V_{CC} = 4.75\text{V}, V_{IL} = 0.8\text{V}$				100	μA
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}$	$I_I = -18\text{mA}$			-1.5	V
Supply current	I_{CCH}	$V_{CC} = 5.25\text{V}$			0.8	1.6	mA
	I_{CCL}	$V_{CC} = 5.25\text{V}$			2.4	4.4	mA

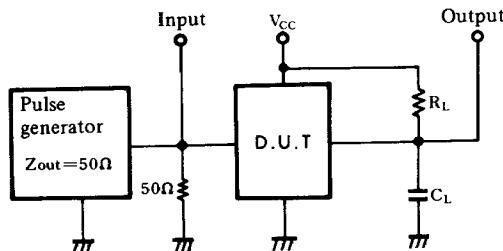
* When constant at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

■ Switching characteristics ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Parameter	Sym	Test conditions		Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$			17	32	ns
	t_{PHL}				15	28	ns

※ Switching parameter measurement information

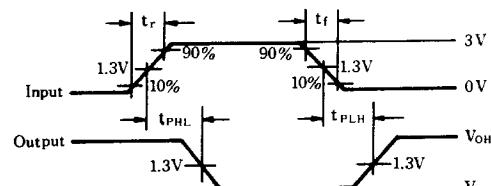
1. Measurement circuit



Notes

1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes

1. Input waveform: $t_r \leq 15\text{ns}$, $t_f \leq 6\text{ns}$, PRR = 1MHz, duty cycle = 50%.