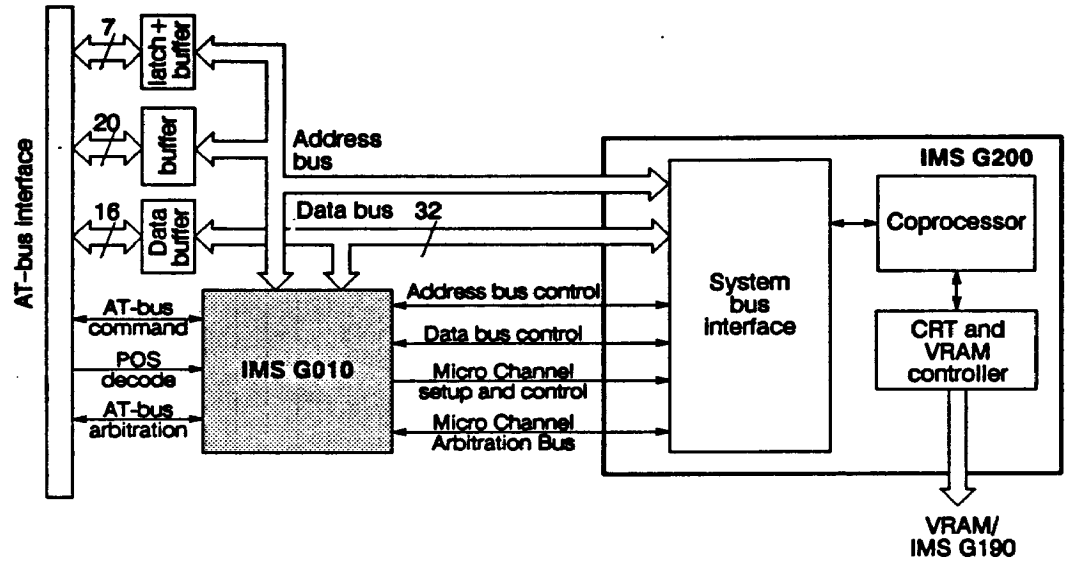
IMS G010
XGA AT-bus interface peripheral

inmos®

Product preview

The information in this document is subject to change



FEATURES

- Compatible with IMS G200 system interface
- Provides all logic to support AT-bus
- Supports multiple DMA channels
- Provides POS register emulation and selection
- Decodes Micro Channel access status for direct AT-bus implementation
- Single +5V ± 5% power supply
- Standard 84 pin PLCC package

GENERAL DESCRIPTION

The IMS G010 is an interface device that allows the INMOS XGA chipset, comprising the IMS G200 Display Controller and the IMS G190 Serializer Palette DAC, to operate in an AT-bus system. It implements many of the IMS G200 Micro Channel bus interface functions to allow the use of multiple DMA channels, card-local set-up and bus sizing with all the required AT-bus I/O, memory and system memory strobes.

SGS-THOMSON MICROELECTRONICS

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November 1991

Contents

1 XGA AT-bus interface using the IMS G010

The IMS G010 is an interface device that enables the INMOS XGA chipset, comprising the IMS G200 Display Controller and the IMS G190 Serializer Palette DAC, to operate in an AT-bus system. The IMS G200, designed to interface to the Micro Channel bus, is able to interface to AT-bus systems through the IMS G010 peripheral. This device implements many of the IMS G200 Micro Channel bus interface functions, allowing the use of multiple DMA channels, card-local setup and bus sizing with all the required AT-bus I/O, memory and system memory strobes.

The IMS G010 together with the IMS G200 provide all the control signals for external data buffers, data byte swapping, address latches and buffers, inherently simplifying system level design. The IMS G010 also allows direct board level configuration for local expansion ROM. Figure 1 illustrates how the IMS G010 is connected into the existing XGA chipset, allowing an AT-bus compatible system interface to and from the IMS G200 display controller.

2 Pin function reference guide

2.1 POS register emulation and selection

Pin name	I/O	Description
notSetup	O	A write to the POS Setup Register, decoded at #96, determines which board will be placed into setup mode. This is indicated by the assertion of the **notSetup** signal. Data bits **D0-2** describe the instance configuration which the IMS G010 uses to place the adaptor into setup mode.
A0-9, A15-19	I	Address signals **A0-9** and **A15-19** are generated by the microprocessor or DMA controller and are gated on the system bus when **BALE** is high. They are used by the AT-bus interface logic for register decoding.
AddrBufDir	I	This signal controls the direction of an external 3 state bidirectional buffer isolating the IMS G200 from the AT-bus address bus. A high signifies the AT-bus is driving the IMS G200 pins (G200 is the slave), a low signifies that the IMS G200 is driving the AT-bus (G200 is the master).
LA20-23	I -	Address signals **LA20-23** generate memory decodes for 16-bit, 1 wait-state, memory cycles and may be derived from the system microprocessor or other arbitrated devices or DMA controllers.
D0-4	I	Data bits **D0-2** describe the instance configuration which the IMS G010 uses to place the adaptor into setup mode. The logic level written on **D3** defines if the boards are in setup mode.
AEN	I	When active, the address enable signal **AEN** tri-states the microprocessor and other devices from the I/O channel to allow DMA transfers to take place.
RESET	I	Bus reset signal.
-ALE	I	This signal indicates a valid microprocessor or DMA address and is used for address latching.
-MEMCS16	O	This signal indicates to the system that the current data transfer is a 1 wait-state, 16-bit, memory cycle. It is derived from the decode of **LA20-23** and is driven with a tri-state driver capable of sinking 20mA.
-IOCS16	O	This signal indicates to the system that the current data transfer is a 16-bit 1 wait-state, I/O cycle. It is derived from the decode of **LA20-23** and is driven with a tri-state driver capable of sinking 20mA.
ARBLVL0-2	I	These signals indicate the POS select number (board number) of the XGA AT-bus board.

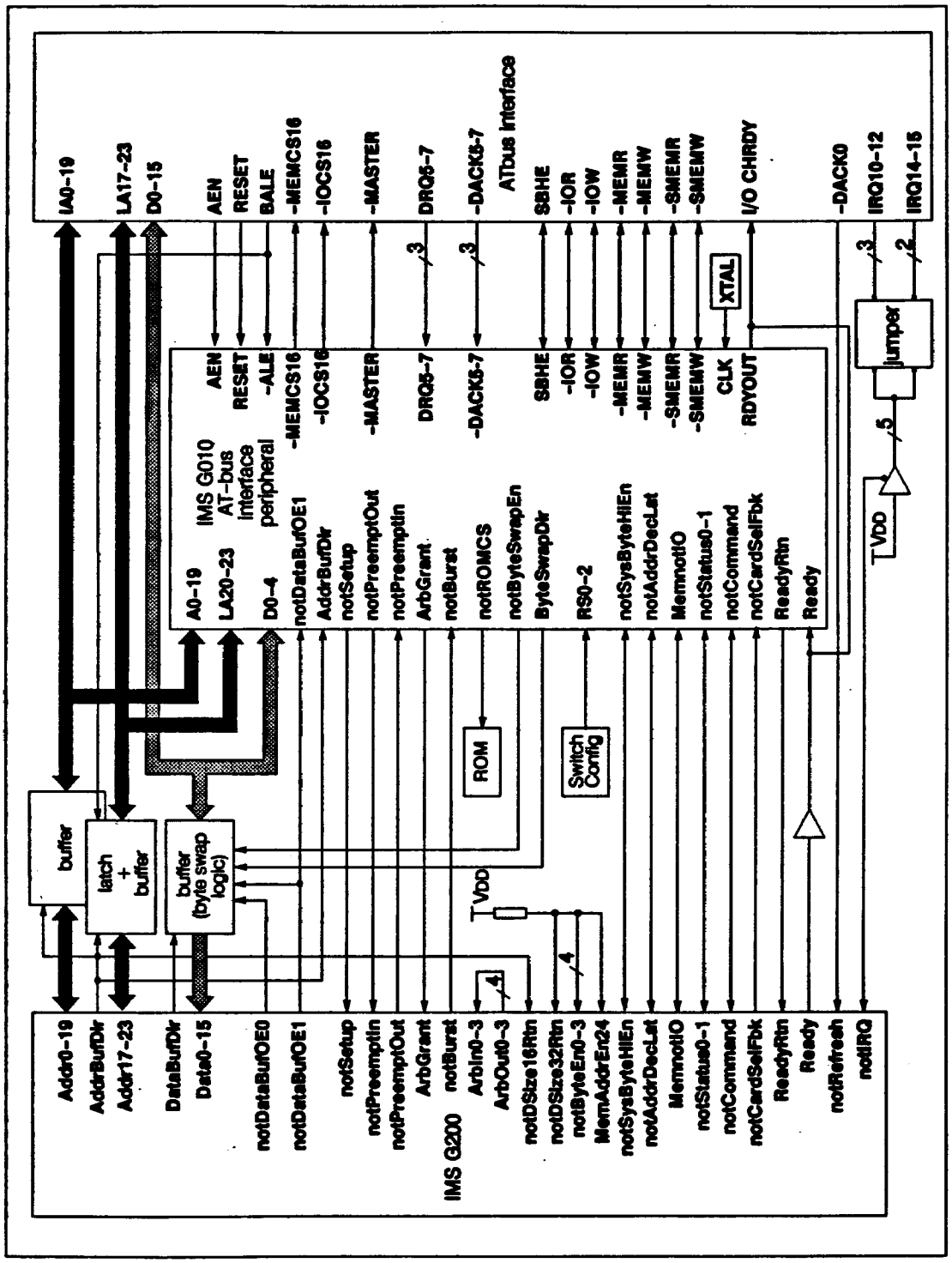


Figure 1 An XGA subsystem implementation for the AT-bus

2.2 DMA arbitration and request logic

Pin name	I/O	Description
notPreemptIn	I	This connects to the IMS G200 **notPreemptOut** signal, which is the output portion of the Micro Channel **-PREEMPT** signal. The IMS G010 uses this signal to generate DMA requests on the assigned channel and to assert **notPreemptIn** on the IMS G200.
notPreemptOut	O	Connected to the IMS G200 **notPreemptIn** signal, the status of this output controls the duration of the arbitration during burst cycles.
ArbGrant	O	This output defines the status of the arbitration cycle. A low on this pin indicates the IMS G010 has control of the assigned DMA channel.
notBurst	I	This signal is asserted by the IMS G200 when extended use of the channel is required for transferring a block of data, defining a burst cycle.
DRQ5-7	O	These signals asynchronously request a bus master service. They are prioritized with **DRQ5** having highest priority and **DRQ7** having lowest.
-DACK5-7	I	A DMA request is serviced after an arbitration acknowledge generated on **-DACK5-7**.
-MASTER	O	This signal is used with a DRQ line to gain control of the system. Typically, an arbitrating controller (the IMS G200) on the I/O channel may assert this signal to allow control of the system address, data and control lines. The IMS G010 asserts this signal and the IMS G200 **ArbGrant** signal when a DMA acknowledgement is received on the I/O channel.

2.3 Command protocol converter

Pin name	I/O	Description
notSysByteHiEn	I/O	System byte high enable. This signal indicates and enables transfer of data on the high byte of the data bus and is used with **Addr0** to distinguish between high byte transfers (**Data8-15**) and low byte transfers (**Data0-7**).
notAddrDecLat	I/O	Address Decode Latch
MemnotIO	I/O	**MemnotIO** distinguishes between memory and input/output (I/O) cycles. When high a memory cycle is in progress, when low an I/O cycle is in progress.
notStatus0-1	I/O	Status bits 0 and 1, asserted at the start of the cycle, indicate in conjunction with the **notMemIO** the type of cycle as outlined below:
notCommand	I/O	This signal indicates the presence of valid data on the data bus.
notCardSelFbk	I	Card select feedback. When the controlling master (eg. i386 processor) addresses the IMS G200, the display controller drives **notCardSelFbk** active to indicate its presence at the address specified.

MemnotIO	notStatus0	notStatus1	Function
0	0	1	I/O write
0	1	0	I/O read
1	0	1	memory write
1	1	0	memory write

Pin name	I/O	Description
Ready	I	This normally active signal is pulled inactive (not ready) by the IMS G200, via a non-inverting buffer, to allow additional time to complete an operation. **Ready** is tied to **RDYOUT** and the AT-bus I/O CHRDY signal.
ReadyRtn	O	The IMS G010 simulates a positive AND of all the channel ready signals. This signal is used by the IMS G010 to extend bus master cycles.
SBHE	I/O	The system byte high enable signal indicates a transfer of data on the upper byte of the data bus, **D8-15**. 16-bit devices use **SBHE** to condition the respective data buffers.
-IOR	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** to produce **-IOR** which instructs an I/O device to drive its data onto the data bus.
-IOW	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** to produce **-IOW** which instructs an I/O device to read the data off the data bus.
-SMEMR	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** with an address decode, to produce **-SMEMR** which instructs memory devices to drive data onto the data bus. **-SMEMR** is active only when the memory decode is within the low 1MByte of memory space.
-SMEMW	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** with an address decode, to produce **-SMEMW** which instructs memory devices to store the data present on the data bus. **-SMEMR** is active only when the memory decode is within the low 1MByte of memory space.
-MEMR	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** to produce **-MEMR** which instructs memory devices to drive data onto the data bus. **-MEMR** is active on all memory read cycles.
-MEMW	I/O	The IMS G010 decodes the Micro Channel signals **MemnotIO** and **notStatus0-1** to produce **-MEMW** which instructs memory devices to store data present on the data bus. **-MEMW** is active on all memory read cycles.
CLK	I	28.322MHz clock input
RDYOUT	O	See description for **Ready** (above).
notByteSwapEn	O	This signal ensures compatibility between Micro Channel and AT-bus assignments of single bytes. The AT-bus specification dictates that when writing byte0, byte1 will also contain byte0 information and when reading byte-wide data, must be resident in byte0. This is contradictory to the Micro Channel specification which requires that data written in byte1 will always be read in byte1. Byte swap logic is therefore required to correct this incompatibility.
ByteSwapDir	O	This signal controls the byte swap buffers direction.
notDataBufOE1	I	Indicates that a high byte (byte 1, bits 8:15) is being transferred on the data bus.

2.4 ROM decoder

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>notROMCS</td><td>O</td><td>The IMS G010 allows optional ROM address space selection defined by binary coded inputs RS0-2. The expansion ROM address space in the system memory map is decoded into 32 KByte sections.</td></tr>
<tr><td>RS0-2</td><td>I</td><td>These inputs define the address space in which the expansion ROM resides. They are binary coded as follows:
<table>
<tr><th>RS0</th><th>RS1</th><th>RS2</th><th>Address space</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>#0C0000</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>#0C8000</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>#0D0000</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>#0D8000</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ROM disabled</td></tr>
</table>
</td></tr>
</table>

3 IMS G010 functional description

The IMS G010 AT-bus interface peripheral comprises four functional blocks.

- POS register emulation and selection
- DMA arbitration and request logic
- Command protocol converter and I/O logic
- ROM address decoder logic

3.1 POS register emulation and selection

An internal 8-bit register is available for card-local POS definition of system parameters for the engineering software setup.

3.2 DMA arbitration control

DMA channel bits are assigned as shown below. These two bits are taken from the 4-bit arbitration level specified in POS register setup (bits 3-6 of the IMS G200 POS register 3). This implementation allows three DMA channels to be active at any one time although only a single DMA channel assigned XGA can be a bus master at any one time. In the maximum system of eight XGA instances, five XGAs must be slave configured (no DMA channel assigned).

Bits	DMA configuration
0 0	No DMA assigned
0 1	DMA channel 5
1 0	DMA channel 6
1 1	DMA channel 7

Table 2 DMA channel assignment

The bus master function on the AT-bus is centrally arbitrated by the DMA controller (on the system motherboard). The three DMA assigned XGA instances will be prioritized by this controller. The IMS G200 has a 4-bit arbitration level defined for the Micro Channel specification. The IMS G010 employs only two bits for the AT-bus implementation.

Writes to the POS Setup Register, decoded at #96, determines which board will be placed into setup mode. The engineering software setup procedure asserts one of eight instance configurations on data bits **D0-2** which are compared by the IMS G010 setup decode logic in all XGAs, to the board selection bits defined by board level switches. The logic level written on **D3** defines whether the boards are in setup mode or not.

The AT-bus signal **-MEMCS16** indicates to the system (or another bus master) that the present data is a one wait state, 16-bit, memory cycle. Its logic level specifies whether a 16-bit memory cycle can proceed or a double access must be performed. Since this signal must be presented *before* the falling edge of **BALE** it must derived from the decode of LA17 through LA23, since these are the earliest available addresses in the cycle.

-MEMCS16 is effectively disabled until the POS register 5 enables the 1MByte aperture.

3.3 DMA arbitration and request logic

The arbitration sequence begins with the IMS G200 asserting **notPreemptOut**. If DMA is enabled the IMS G010 asserts **DREQ5, DREQ6** or **DREQ7**, causing **notPreemptOut** from the IMS G010 to assert **notPreemptIn** on the IMS G200.

The system DMA controller (8237) prioritises requests and grants a channel by asserting **-DACK5-7**. The IMS G010 in response asserts both **-MASTER** to the system and **ArbGrant** to the IMS G200. Upon reception of the low level on **ArbGrant**, the IMS G200 drives **notBurst** (if required) and deasserts **notPreemptOut**. The IMS G010 uses the status of **notBurst** to maintain mastership over the defined DMA channel for the required number of accesses (**notPreemptOut** is also held low until **notBurst** returns high).

Holding **notPreemptOut** low in this fashion forces the IMS G200 to timeout the arbitration in order to accommodate another master. This method forces the IMS G200 to obey the fairness protocol defined for the Micro Channel in order to limit DMA access time to 7.8μs; thus maintaining the dynamic memory refresh requirements.

3.4 Command protocol converter

The Micro Channel protocol implements coded status bits to define the type of cycle. The IMS G010 bi-directionally decodes between **notStatus0-1** and **MemnotIO** from the IMS G200 and the AT-bus compatible signals **-IOR, -IOW, -MEMR, -MEMW, -SMEMR** and **-SMEMW**.

When the system processor performs an AT-bus access to the XGA subsystem, a wait state must be introduced since the AT-bus protocol will not define the type of cycle until **-IOR, -IOW, -MEMR, -MEMW, -SMEMR** or **-SMEMW** is asserted. Typically, **-IOR, -IOW, -MEMR, -MEMW, -SMEMR** or **-SMEMW** sets **notStatus0-1** to the relevant decode one clock cycle into the AT-bus cycle; two further cycles are then required to complete the Micro Channel cycle from the point of **notStatus0-1** being presented.

During AT-bus to Micro Channel protocol conversions, byte swap operations are controlled by the IMS G010. The AT-bus specification dictates that when writing a single byte0, byte1 will also contain byte0 information; a byte read operation requires the data to be presented in byte0. This is contradictory with the Micro Channel specification which states that data written in byte1 will always be read in byte1. Byte swap logic is inherently required to correct this incompatibility.

4 Package specifications

4.1 84 pin plastic leaded-chip-carrier package

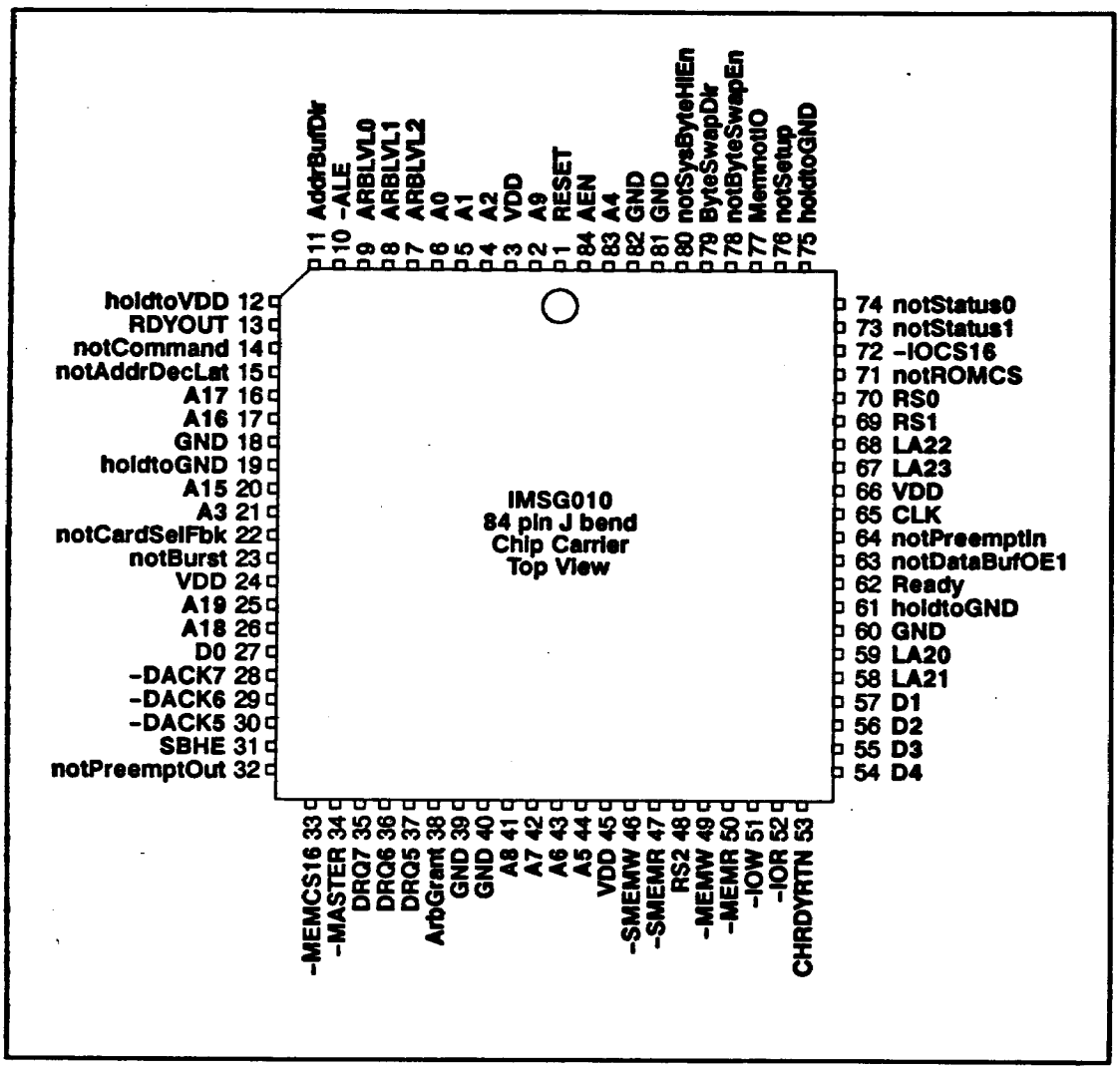
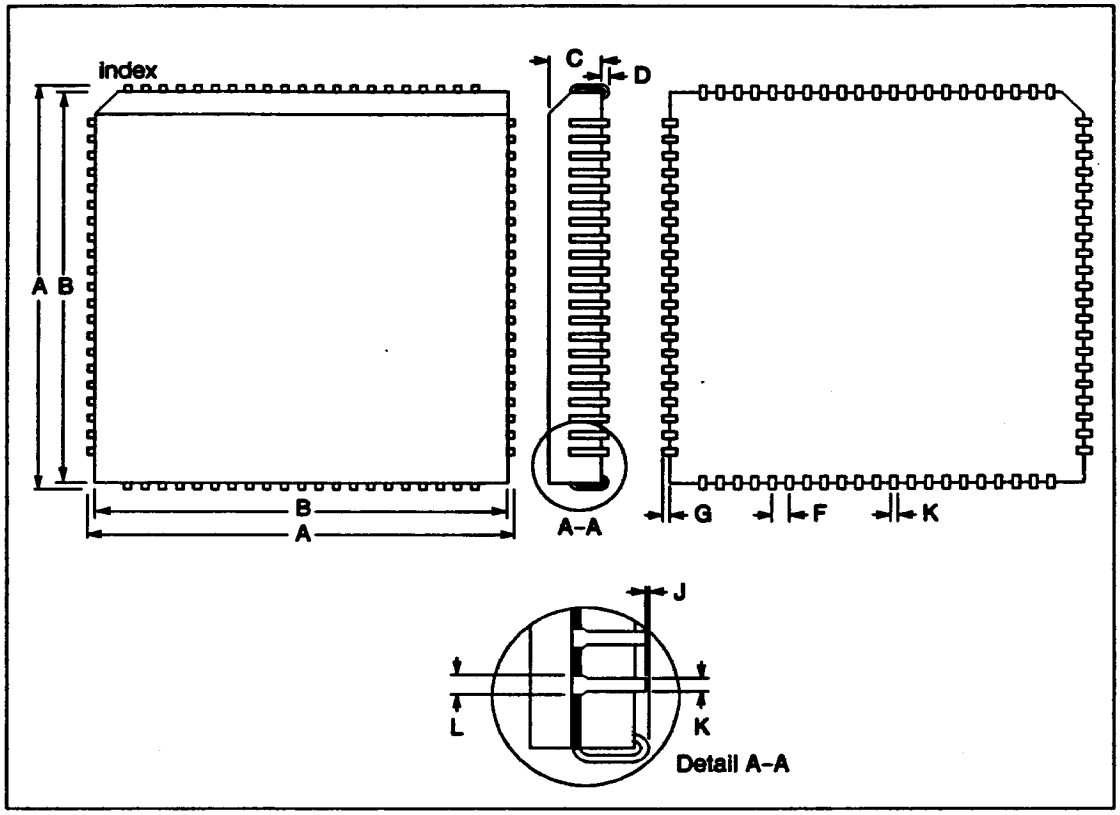


Figure 2 IMS G010 pin configuration



DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	30.226	±0.127	1.190	±0.005	
B	29.312	±0.127	1.154	±0.005	
C	3.810	±0.127	0.150	±0.005	
D	0.508	±0.127	0.020	±0.005	
F	1.270	±0.127	0.050	±0.005	
G	0.457	±0.127	0.018	±0.005	
J	0.000	±0.051	0.000	±0.002	
K	0.457	±0.127	0.018	±0.005	
L	0.762	±0.127	0.030	±0.005	
Package weight is approximately 7.0 grams					

Table 3 84 pin PLCC J-bend package dimensions

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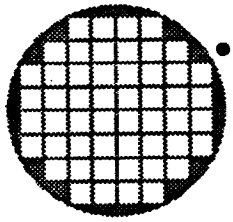
November 1991



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November 1991