L6260

2.7 – 5.5V DISK DRIVER SPINDLE & VCM, POWER & CONTROL COMBO'S

PRODUCT PREVIEW

GENERAL

- 5V AND 3V OPERATION. *REGISTER BASED ARCHITECTURE
- MINIMUM EXTERNAL COMPONENTS
- SLEEP AND IDLE MODES FOR LOW POWER CONSUMPTION.
- SELECTABLE GAINS FOR BOTH V.C.M. AND SPINDLE.
- 10 BIT (+ SIGN + GAIN) VCM & 8 BIT SPINDLE DACs
- HIGH BANDWIDTH SPEED REGULATION LOOP (ONCE PER MECH\ELEC CYCLE ACCURACY)

VCM DRIVER

- CURRENT SENSE CONTROL (VOLTAGE PROPORTIONAL TO CURRENT).
- 300mA DRIVE CAPABILITY
- TWO CURRENT RANGES FOR SEEKING AND TRACKING
- INTERNAL REGISTER FOR POWER AMP CONTROL LINES

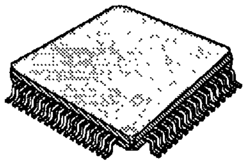
SPINDLE DRIVER

- BEMF PROCESSING FOR SENSOR-LESS MOTOR COMMUTATION
- PROGRAMMABLE COMMUTATION PHASE DELAY
- PROGRAMMABLE SLEW-RATE FOR REDUCED E.M.I.
- 0.8Ω FOR ANY HALF BRIDGE WORST CASE
- SYNCHRONOUS RECTIFICATION OF THE B.E.M.F. DURING RETRACT OPERATION
- UNIPOLAR \ BIPOLAR \ TRIPOLAR OPERATION
- SYNTHESIZED HALL OUTPUTS
- 1.0 AMP DRIVE CAPABILITY

OTHER FUNCTIONS

- POWER UP SEQUENCING
- POWER DOWN SEQUENCING
- LOW VOLTAGE SENSE
- ACTUATOR RETRACTION
- DYNAMIC BRAKE

HF3CMOS TECHNOLOGY



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ORDERING NUMBER: L6260

- THERMAL SHUTDOWN
- THERMAL & CURRENT PROTECTION

DESCRIPTION

The L6260 is single chip sensorless (DC) spindle motor and voice coil controllers that including power stages suitable for use in small disk drives.

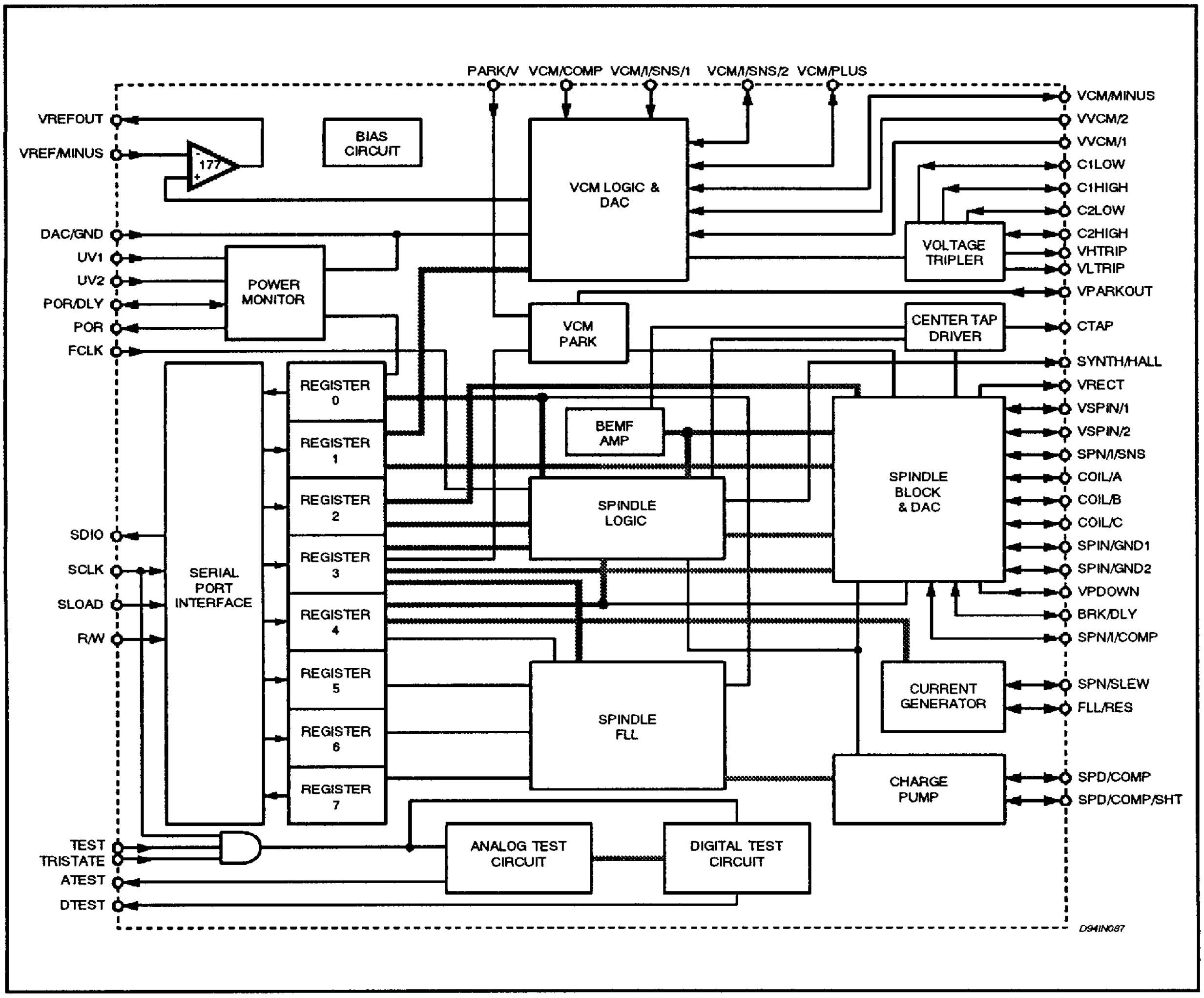
These devices have a serial interface for a microprocessor running up to 10 Mega bits per second. There are registers on chip to allow the setting of the desired spindle speed via the on chip Frequency Locked Loop (F.L.L.). No external components are required in the sensor-less operation as the control functions are integrated on chip (e.g. B.E.M.F. processing, digital masking, digital delay and sequencing).

The V.C.M. drivers uses a transconductance amplifier, able to provide 2 different current ranges, suitable for seeking and tracking.

When a low voltage is detected, a Power On Reset (P.O.R.) is issued and the internal registers are reset, the spindle power circuitry is tri-stated, B.E.M.F. synchronous rectification is enabled, the actuator retracts and then dynamic braking of the spindle is applied. The L6261 includes an extra pin carrying an accurate programmable voltage.

These devices are built in HF3CMOS technology allowing dense digital circuitry to be combined with MOS\Bipolar power devices.

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)

Power

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
8	VDC	Digital power. Positive nominally 5V or 3V	AI	No	No
41	VCC	Analog power. Positive nominally 5V or 3V	AI	No	No
54	VVCM_1	VCM power supply. Positive nominally 5V or 3V	AI	No	No
58	VVCM_2	Same as above	AI	No	No
23	VSPIN_1	Spindle power pin. Positive nominally 5V or 3V	AI	No	No
31	VSPIN_2	Same as above	AI	No	No
1	GND	Ground	AI	No	No
15-17	GND	Ground	AI	No	No
32-34	GND	Ground	AI	No	No
47-49	GND	Ground	AI	No	No
18	SPN_GND_1	Ground for spindle circuit	AI	No	No
27	SPN_GND_2	As above	AI	No	No
44	DAC_GND	Ground for all DACs	AI	No	No
45	AGND	Analog ground	AI	No	No
7	DIG_GND	Digital ground	AI	No	No
63	TRIPGND	Voltage tripler ground	AI	No	No

Serial Interface & Test Pins

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
12	FCLCK	System clock. 4-12MHz selectable via the CLK_PRESCALE bit in the System Control Register B (Reg 4 Bit 4).	DI	Yes	No
11	SDIO	Serial port data I/O running up to 10MHz. For full details of all serial port signals see the Circuit Description section.	DI/O	Yes	Yes
10	SCLK	Serial port clock (max 10Mbits/s)	DI	Yes	No
19	R/W	Read / Write signal for serial interface	DI	Yes	No
9	SLOAD	Chip select input.	DI	Yes	No
21	TEST	Used to enable one of the test modes. The mode is selcted in conjunction with the TRISTATE pin (see below for more details).	DI	No	No
24	TRISTATE	Used to enable one of the test modes. The mode is selcted in conjunction with the TEST pin (see below for more details). This pin has no effect on the spindle or VCM drivers, this is a test pin only.	DI	No	No
60	ATEST	Analog test pin. This pin carries the required analog signal to allow external testing.	AO	No	No
26	DTEST	Digital Test Output Pin. This pin also doubles as the Clock input if an external FLL is used.	DI/O	No	No

Test Mode	TEST pin	TRISTATE pin
IOMAPPING Test	1	0
DIGITAL Test*	1	1
ANALOG Test*	1	1
TRISTATE Test	0	1
Normal Operation (non test mode)	0	0

For a detailed description please refer to the Test Circuit section of the CIRCUIT OPERATION portion of this datasheet

*These two test modes operate simultaneously through separate testpins (ATEST and DTEST).

PIN DESCRIPTION (continued)

Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)

VCM Driver and DAC

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
53	VCM_I_SNS1	To ISENSE resistor network. This voltage is proportional to the current through the VCM load as sensed by the sense resistor and is used for the fine adjustment. The resistor is always five times higher than that in VCM_I_SNS2 (e.g .3.333Ω smallest resistance).	A	No	No
56	VCM_I_SNS2	As above but this is the coarse adjustment. As such the current is 300mA maximum and the voltage 0.25V (one fifth of VCM_I_SNS1). e.g 0.833Ω smallest resistance.	A	No	No
6	VCM_COMP	VCM RC compensation network. An RC network from this pin to ground allows for compensation of the VCM driver. Example typical values are 10KΩ and 2.7nF.	A	No	No
57	VCM_PLUS	One end of the VCM load is attached to this pin (positive)	A	No	No
55	VCM_MINUS	The other end of the VCM load is attached to this pin (negative)	A	No	No
46	PARK_V	The PARK voltage is defined by a resistor from this pin to GND. 10μA is supplied to this pin. VRequired = 10μA x R.	A	No	No
35	VPARKOUT	Output from the retract circuit. This is usually connected directly to the VCM_MINUS pin.	AO	No	No

Spindle Driver and DAC

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
40	SPN_SLEW	A resistor from this pin to ground defines the slew rate along with the setting of Register 4 bits 7-10.I0=0.5V/R. I0 should be in the range of 2μA - 16μA. 250KΩ nominal. I0 is multiplied by the value in Reg 4. e.g. I0 x Reg = Desired ISlew. There is an internal 20pf cap.	A	A	No
36	SPN_I_COMP	An RC network from this pin to ground sets the spin driver compensation. Typical values are 20KΩ and 4nf.	A	No	No
13	SPN_I_SNS	The current sensing resistor is connected from this pin to ground (sense FET output). This is described fully in the CIRCUIT OPERATION section.(Typical 2.5KΩ).	AO	No	No
20	COIL_A	Motor coil driving pins. These pins are also used for sensing the BEMF. Phase A.	A	No	No
25	COIL_B	Phase B version of above.	A	No	No
29	COIL_C	Phase C version of above.	A	No	No
59	CTAP	The center tap of the motor must be connected to this pin.	A	No	No
22	SYNTH_HALL	A CMOS level signal that emulates one of the Hall signals (see the description on page 16 for a complete description).	DO	Yes	Yes
37	SPD_COMP	An RC network on this pin defines the compensation network for the spindle while at speed.	A	No	No
38	SPD_COMP_SHT	This shorts out the resistor from this network if required (when bit 9 of Reg 3 is set to 1, SPEED bit of the System Control Register A).	A	No	No
39	FLL_RES	Frequency Locked Loop charge pump gain resistor. The gain is also trimmed (multiplied) upwards with the setting of Register 4 bits 0-2 (FLLGAIN bits in the System Control Register B). I0=0.5V/R. I0 is multiplied by the contents of the above register. I0 should be in the range of 40μA - 320μA. 12.5KΩ nominal.	A	A	No

PIN DESCRIPTION (continued)

Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)

Power down sequencing, POR, other voltage pins

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
14	VRECT	Under normal conditions, power is supplied to various blocks via this pin. When the external power is removed , energy stored in the rotating spindle is converted into a voltage which supplies the retract circuitry.	AO	No	No
28	BRK_DLY	An external parallel RC network from this point to ground delays the activation	A	No	No
30	VPDOWN	Voltage tripler reservoir capacitor. This is used for the brake operation when power is removed from the chip. No DC load allowed. 1μF minimum, 10μF prefered.	A	No	No
61	C1HIGH	Voltage tripler charge pump capacitor (C1) for step up conversion. This maybe removed if higher RDSONs are required. 10nF nominal (5nF - 20nF okay).	A	No	No
62	C1LOW	The other polarity of the voltage tripler charge pump capacitor (C1) for step up conversion. This maybe removed if higher RDSONs are required.	A	No	No
64	C2HIGH	Voltage tripler charge pump capacitor (C2) for step up conversion. This maybe removed if higher RDSONs are required. 10nF nominal (5nF - 20nF okay).	A	No	No
2	C2LOW	The other polarity of the voltage tripler charge pump capacitor (C2) for step up conversion. This maybe removed if higher RDSONs are required.	A	No	No
52	POR_DLY	An external capacitor from this pin to ground defines the amount of time that this signal stays active. See Circuit Operation section for further details.	A	No	No
5	$\overline{\text{POR}}$	Power On Reset. This pin goes low when the supply voltage goes below the VOLTAGE GOOD threshold defined by UV1 and UV2. Supplies 1mA minimum.	DO	Yes	No
50	UV1	Under voltage detector 1. This defines the VOLTAGE GOOD threshold by comparing the voltage on this pin to the internal 1.25V reference. An external resistor divider network and capacitor filter provides the selection of threshold and supply noise rejection. There is an internal pull-up (2μA max).	AI	Yes	No
51	UV2	Under voltage detector 2. This defines the VOLTAGE GOOD threshold by comparing the voltage on this pin to the internal 1.25V reference. An external resistor divider network and capacitor filter provides the selection of threshold and supply noise rejection. There is an internal pull-up (2μA max).	AI	Yes	No
4	VHTRIP	High tripler output. 100nF-1μF cap required. 11V max.	AO	No	No
3	VLTRIP	Low tripler output. 10nF recommended for stabilization only.	AO	No	No

PIN DESCRIPTION (continued)

Pin Types: I = Input, O = Output, P = Power, A = Analog (passive)

Auxiliary Functions

PIN #	PIN NAME	DESCRIPTION	PIN TYPE	I\O MAPPED?	TRI-STATE @SLEEP/@POR
42	REFOUT	Output from auxiliary OPAMP.	A	No	No
43*	VREF_MINUS (L6260 only)	Negative input to auxiliary OPAMP. This is prsent ONLY on the L6260.	A	No	No
43*	VDAC_OUT (L6261 only)	This is the programmable voltage output pin. In the L6261, this replaces the VREF_MINUS pin of the L6260. This pin is not present on the L6260.	A	No	No
26	EXTFLL/ DTEST	See previous description of this pin (Serial Interface & Test Pin section).	DI/O	No	No

* This pin is used for different purposes between the L6260 & L6261

FEATURES

General

- 2.7 - 5.5 volts single voltage operation.
- Sleep mode
  - Less than 1.0 milliamperes of supply current 200 microamperes typical.
  - The VCM drivers are in high impedance state.
  - The spindle drivers are in high impedance state.
- Idle mode
  - All circuitry related to the VCM section is turned off.
  - The driver goes to a high impedance state.
- Dual supply power monitor.
  - Divider center brought to pin for possible external adjustment of threshold or disabling by connecting to Vdd.
  - Tolerance 2%.
- Power up Microprocessor reset sequencing.
  - Power up reset and delay.
  - Internal register initialization.
- Over temperature protection.
- Internal reference 1.25 volts available at external pin via buffer amplifier.
- The L6260 includes an extra Op-Amp for general useage (associated with the VCM DAC).
- The L6261 replaces the extra Op-Amp with a highly accurate programmable voltage source.

Interface

- Serial Synchronous
  - SCLK, SLOAD, SDIO, R/W.
  - 10 Megabit/sec data rate.

VCM Driver

- Internal power devices.
- Transconductance loop for H bridge.
- Intrinsic clamping of outputs to prevent substrate current
- 10 bit plus sign +GAIN resolution DAC.
  - Two ranges, ratio set by external resistors.
  - 10 bits resistive divider & 1 bit sign.
  - Chopper stabilized OTA.
  - Crossover distortion less than 1 bit.
- 20Khertz current loop bandwidth achievable.
- Voltage controlled retract.

Spindle Driver

- Internal power devices.
- Three phase bridge plus bipolar driver (and logic for unipolar operation).
- Tripolar drive option via microprocessor (for stuck rotor startup).
- Unipolar operation with center tap driver (guaranteed operation at 3V, not at 5V).
- Microprocessor spin-up and internal FLL speed control.
  - Microprocessor initiated startup with auto BEMF sensed spin-up.
  - Programmable commutation delay.
  - Speed compensation by external RC network.
  - Speed sensing by internal BEMF or external (servo bursts).
  - No snubbers required for current loop compensation or EMI control.
  - Microprocessor acceleration control via DAC (for smooth transition to at speed control) or FLL control.
- Non-linear control loop for faster speed settling time.
- Automatic clamping of output to prevent substrate current.
- Programmable slew rate control.
- Series current sense resistor and internal sense FET.

FEATURES (continued)

- 8 bit resolution spindle DAC for microprocessor acceleration control.
- Retract followed by brake if "command brake" asserted.

Retract

- Two quadrant retract.
- 2 operating modes:
  - Commanded (without an automatic brake). and
  - Undervoltage (park followed by automatic brake).
- Voltage controlled
- No blocking diode required
- Internal synchronous rectification of spindle BEMF.
- Retract then brake after delay

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{dd}, $V_{p\,max}$	Maximum Supply voltage	7	V
$V_{in\,max}$	Maximum input voltage	Vdd + 0.3 V	V
$V_{in\,min}$	Minimum input voltage	GND - 0.5 V	V
I_{peak}	Peak sink/source output current	1.5	A
I_{dc}	DC sink source output current	1.0	A
P_{tot}	Maximum Total Power Dissipation	1.0	W
T_{stg}, T_j	Maximum storage/junction temperature	-40 to 150	°C
$R_{th\,j\text{-}amb}$	Thermal resistance Junction to ambient. Standard PCB mounted	Package dependent	°C/W

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{dd}, V_p	Supply voltage range		2.7		5.5	V
READY	QUIESCENT CURRENT	VCM ENABLED SPINDLE ENABLED			10	mA
IDLE	QUIESCENT CURRENT	VCM DISABLEDSPINDLE ENABLED			5	mA
SLEEP	QUIESCENT CURRENT	VCM DISABLEDSPINDLE DISABLED		200	1000	µA

THERMAL DATA

To be determined

RECOMMENDED OPERATING CONDITIONS

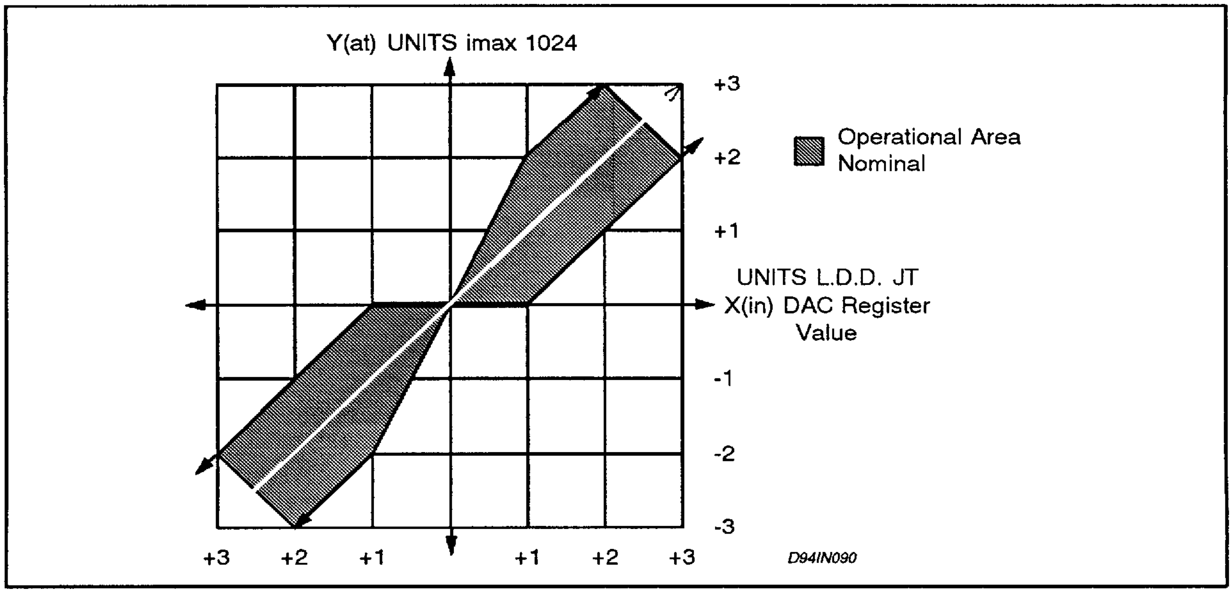
Symbol	Parameter	Value	Unit
V_{ddn}	Supply Voltage	2.7 to 5.5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_j	Junction Temperature	0 to 125	°C

ELECTRICAL CHARACTERISTICS

VCM Driver

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{ocr}	Max Current Coarse Range				300	mA
I_{ofr}	Max Current Fine Range				75	mA
R_{dson} ABEF	Source & Sink On Resistance Coarse	T_j =125 °C , I_{load} = 300 mA		1.0	2.5	Ohms
R_{dson} CD	Sink On Resistance Fine Range	C, D VCM drive transistors		5.0	10.0	Ohms
V_{jump}	Current Sense Jump Discontinuity				1	LSB
$V_{deadband}$	Current Sense Deadband				200	µV
I_{csbias}	Current Sense Bias Current				1	µA
PSRR	DC Power Supply Rejection Ratio	V_{dd} 2.7 to 5.5 V	50			dB
BW	Current Loop Bandwidth	La = 1mH Ra=40ohms I_{max} =75mA	20			KHz

Figure 1: Vjump vs. Deadband



VCM DAC

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
R_{es}	Resolution 10 Bits Resistive Ladder Plus Sign (1 Bit)	Unipolar			10	bits
N.L.	Differential Non-Linearity				1	LSB
I.N.L.	Integral Non - Linearity				3.0	LSB
C_T	Conversion Time 0 - 90 %	From Input Of Last Bit (for any change of code)			1.0	µs
FSTC	Full Scale Temperature Coefficient	0 to 125 °C			250	ppm/C
Voh	High Output Voltage	25 °C, No Load	0.240	0.250	0.260	V
Vol	Low output Voltage	25 °C, No Load			100	µV
PSRR	Power Supply Rejection		50			dB

ELECTRICAL CHARACTERISTICS (continued)

Spindle Motor

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_o	Maximum Output Current		1			A
R_{dson} Sink	Sink On Resistance	T_j =125 °C , I_{load} = 1A			0.4	Ohms
R_{dson} Total	Total drive resistance R_{dson} sink + R_{dson} source	T_j =125 °C, I_{load} = 1A			0.8	Ohms
dv/dt	Voltage Slew Rate		1		1	V/µs
R_{dson} unipolar	Unipolar Drive Resistance				1	Ohm

Spindle Current Sense FET

linearity Large signal	Current sense circuit linearity (spin-up). 2000:1 current sense.	1% to full scale current			5	%FS
Linearity small signal	Current sense circuit linearity(at speed). 500:1 current sense.	1% to 10% full scale			5	%
BW	Current loop bandwidth small signal (at speed)	Lmotor 100µH to 1 µH	20			KHz
FS	Full scale current error				5	%FS
matching	Current sense matching	25 to 250 mA			5	%

DAC Acceleration Control

res	Resolution	Full scale			8	bits
NL	Differential Non-linearity				0.5	LSB
INL	Integral Non-linearity				1	LSB
FS	Full scale accuracy				5	%
CT	Conversion time				10	ms
FSTC	Full Scale Temp Coefficient				250	ppm/°C
V_{oh}			1.2375	1.25	1.2625	V
V_{ol}			0	0.2	0.3	V
Gain1X	Current Sense Gain at 500:1		TBD	500	TBD	
Gain5X	Current Sense Gain at 2500:1		TBD	2500:1	TBD	

Step-up Converter

V_{su3}	Step-up converter voltage (using Tripler as a doubler) above 5V.	V_{dd} = 4.5 to 5.5 volts, Maximum load	3.5	4.5		V
V_{su5}	Step-up converter voltage (using Tripler as a quadrupler) above 3V.	V_{dd} = 2.7 to 3.3 volts, Maximum load		4.5		V

Digital Inputs (All digital inputs are CMOS compatible)

V_{ih}	High level input voltage	I_{in} = TBD	30% V_{dd}			V
V_{il}	Low level input voltage	I_{in} = TBD			70% V_{dd}	V
V_{oh}	High level output voltage	I_{out} = TBD	V_{dd}-0.6			V
V_{ol}	Low level output voltage	I_{out} = TBD			0.4	V
I_{in}	Input leakage current	T_j =125°C	+1		-1	µA

Power On Reset (Either low voltage detector can be disabled by trying the divider to a high voltage)

T_{delay}	Minimum delay power OK to RESET high	C_{POR_DELAY} = 0.22*H	110	137.5	165	ms
V_{ref}	Voltage reference		1.225	1.25	1.275	V

ELECTRICAL CHARACTERISTICS

Retract

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Units
$T_{retract}$	Retract time before brake	power low detected $T_{retract} = 0.4 \times RC$	TBD		TBD	ms
R_{dson}	Total switch circuit resistance				10	Ohms
T_{brake}	Minimum brake time		3			s
$V_{retract}$	2 quadrant retract voltage	V_{BEMF} > PARK_V. ($V_{retract} = 10\mu A \times R_{RETRACT}$)	0.1		2	V

INTERNAL REGISTER DEFINITION

System Status Register (Reg 0)

Reg: 0

Name: System Status Register

Type: Readonly.

BIT	LABEL	DESCRIPTION	@POR
0	THERMAL	Thermal shutdown = 1, normal = 0. One signifies that the chip temperature has exceeded the 180°C. The bit will reset when the temperature falls from 180°C to 140°C (the hysteresis prevents rapid changing of this bit). When this bit is activated, the spindle logic will tristate both high and low side drivers to allow the disk to coast and cool down the chip.	0
1	UV	Under Voltage=0, good voltage =1. This signals whether the under voltage circuit has been activated or not. NOTE: When UV=0, the POR is activated and all serial port control logic is reset. This means that writes are impossible, however, the user can still poll the status of this register provided the logic voltage is sufficient for the logic to function.	0
2	FLL_UP	Providing mainly for testing. When the FLL is sourcing current into the charge pump capacitor this is set to 1. A 0 means that the sourcing current is disabled.	0
3	FLL_DOWN	Providing mainly for testing. When the FLL is sinking current from the charge pump capacitor this is set to 1. A 0 means that the sourcing current is disabled.	0
4	BEMF_SENSE	Toggles with BEMF.	0
5	MASK_TIME	Mask time currently in use = 1. When 1 this means the BEMF comparator will not sense the zero crossing at this time. A 0 means zero crossing sensing will occur.	0
6	DELAY	Delay time currently in use = 1. e.g. A commutation delay is active and at the end of this delay the next commutation is executed.	0
7	AT_SPEED	1=spindle is at speed (set by the first "down pulse" of the FLL. It is reset at POR.	0
8		UNUSED	0
9		UNUSED	0
10		UNUSED	0
11		UNUSED	0

VCM DAC Register (Reg 1)

The VCM DAC register is used to control the current in the voice coil motor. All 10 bits are part of a resistor divider network. Bit 10 is the sign bit and logically controls the current direction through the VCM. Bit 11 selects the current sense resistor to use for current control. A 0 selects coarse and therefore only the lower sense resistor, a 1 selects the top of both resistors so that the sense resistor is the sum of the coarse and fine resistance's.

To clarify the manner in which the 2's complement is used here are some examples:

Value entered to register (0x means hex)	DAC value	Sign	Gain
0x000	0x000	+	0
0x800	0x000	+	1
0x3FF	0x3FF	+	0
0x400	0x3FF	-	0
0x401	0x3FF	-	0
0x7FF	0x001	-	0

Reg: 1
Name: VCM DAC Register
Type: Write only.

BIT	LABEL	DESCRIPTION	@POR
0	VDAC BIT 0	LSB resistor ladder of the 10 bit VCM DAC. This is a true unsigned representation of the DAC input. The value entered here is a 2s-complement of the required DAC value encoded across eleven bits (10 bit data and 1 sign bit encoded into 11 bits in 2s-complement)	0
1	VDAC BIT 1		0
2	VDAC BIT 2		0
3	VDAC BIT 3		0
4	VDAC BIT 4		0
5	VDAC BIT 5		0
6	VDAC BIT 6		0
7	VDAC BIT 7		0
8	VDAC BIT 8		0
9	VDAC BIT 9	MSB resistor ladder.	0
10	VCMSIGN	Sign bit of the above 2s-complement number.	0
11	VCMGAIN	This changes the gain of the VCM DAC	0

Spin Control Register (Reg 2)

The spin control register has two functions:

(1) The first (bits 0-7) is to program the current to the spindle motor to allow motor control and to preset the "at speed" voltage for the charge pump.

(2) The second (bits 8-11) is to set the phase lag from when a BEMF zero crossing occurs to the next commutation. Nominally the delay would be 30 electrical degrees but it often is better to advanced the commutation, due to the presence of other sources of delay, related to switching. The range is from 1.875 through to 28.125 electrical degree delay at 1.875 degree increments.

Reg: 2
Name: Spin Control Register
Type: Write only.

BIT	LABEL	DESCRIPTION	@POR
0	SPIN DAC BIT 0	Spindle current limit LSB (LSB of 8 bits written to the spindle DAC)	0
1	SPIN DAC BIT 1		0
2	SPIN DAC BIT 2		0
3	SPIN DAC BIT 3		0
4	SPIN DAC BIT 4		0
5	SPIN DAC BIT 5		0
6	SPIN DAC BIT 6		0
7	SPIN DAC BIT 7	Spindle current limit MSB	0
8	SPINDLY BIT 0	Spindle commutation delay LSB	0
9	SPINDLY BIT 1		0
10	SPINDLY BIT 2		0
11	SPINDLY BIT 3	Spindle commutation delay MSB	0

System Control Register A (Reg 3)

Reg: 3

Name: System Control Register A

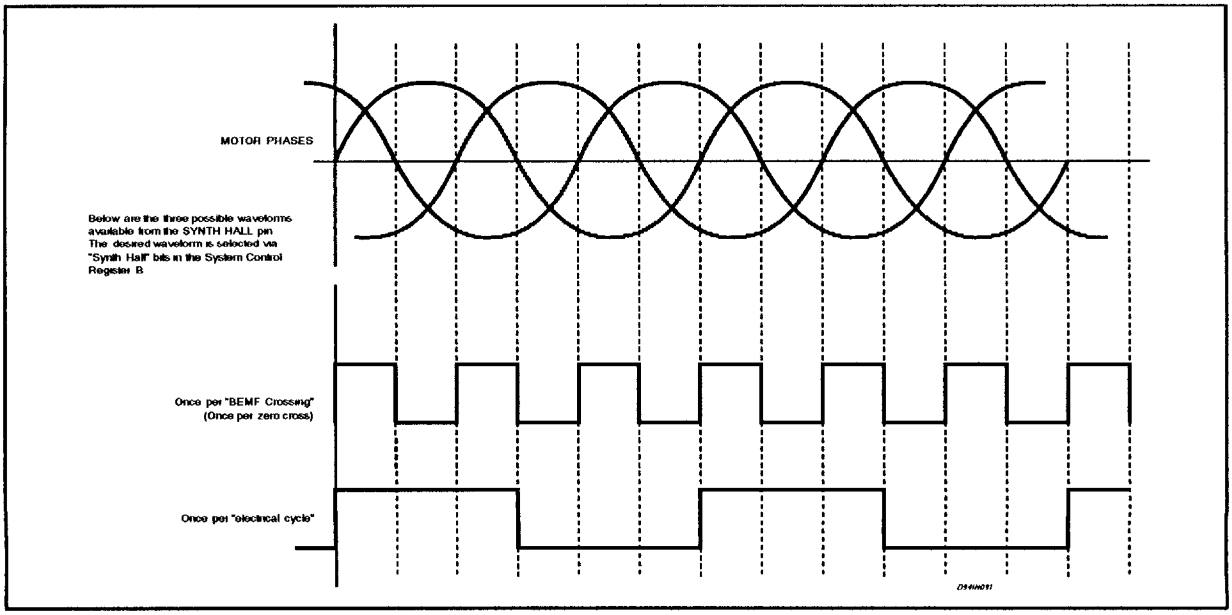
Type: Write only.

BIT	LABEL	DESCRIPTION	@POR
0	SPIN_ENABLE	Enable spindle functions (1 = Enabled, 0 = Idle or Sleep). If both SPIN ENABLE and VCM ENABLE are set to 0 (VCM & SPIN), the chip will go into Sleep mode. VCM & SPIN will cause the part to go into Idle mode. SPIN & VCM is invalid and must never occur. SPIN & VCM is Ready mode for normal operation of the spindle and VCM.	0
1	VCM_ENABLE	Enable VCM functions (1 = Enabled, 0 = Idle or Sleep = 0): See bit 0 for more details.	0
2	SRESET	Reset spindle state machine (the sequencer) (0 = Reset). All spindle and FLL registers are reset.	0
3	INCRE	Increment spindle state machine (1 to toggle sequencer) or in other words advance the commutation. This is normally for use in SEARCH mode.	0
4	RUN_SRCH	1 = Auto-increment (RUN), 0 = Use Increment state (SEARCH) and hence the INCRE bit. In RUN mode the sequencer in automatically toggled by the zero crossing. SEARCH mode implies that the microprocessor is controlling the sequencing.	0
5	8_12P	Selects 8/12 pole motor: 0 = 8 pole, 1 = 12 pole	0
6	BIP_TRIP	Used in conjunction with the following bit to define the mode of operation of the spindle. (0,0) = Tristate, (1,0) = Bipolar where the bit positions are (0,1) = Unipolar, (1,1) = Tripolar (Bit 6, Bit 7)	0,0
7	UNI_TRIP		
8	VCMRET	Puts VCM driver into retract: 1 = retract.	0
9	SPEED	Open or closed loop speed control. This basically controls whether the FLL or the DAC is used to control the Speed Regulation Loop. 1 = open loop (DAC control), 0 = closed loop (FLL control).The SPD_COMP_SHT pin is used to short one of the external resistors when this bit is set to one.	0
10	EL_MECH	Specifies electrical or mechanical cycle for the FLL control. 1 = Electrical, 0 = Mechanical	0
11	TEST_COUNT_RESET	Resets (0) the TEST_MODE counter	0

System Control Reg B (Reg 4)
Reg: 4
Name: System Control Register B
Type: Write only

BIT	LABEL	DESCRIPTION	@POR
0	FLLGAIN BIT 0	FLL Gain bit LSB. These three bits define 1-8 times gain factor for the FLL.	0
1	FLLGAIN BIT 1	charge pump.	0
2	FLLGAIN BIT 2	← FLL Gain MSB	0
3	EXT_INT	External or internal spindle loop feedback (BEMF = 0, Ext = 1) External feedback is connected via the DTEST pin which is configured as an output in this mode.	0
4	CLK_PRESCALE	This selects if the system FCLK will be divided by 1 or 2. The selection here allows the same performance of the FLL and logic counters.1 = 4-6MHz system clock, 0 = 8-12MHz system clock	0
5	SYNHALL	This selects the type of signal to be presented at the SYNTH_HALL pin.0 = Synth Hall pin will produce a once per BEMF crossing signal (from BEMF comparitor) 1 = Synth Hall pin will give a once per electrical cycle signal (from zero crossing detector).	0
6	SFETGAIN	Selects the gain of the sense FET circuit of the spindle driver. 0 = Spindle is high transconductance loop gain, 1 = low gain	0
7	SLEW BIT 0	Slew LSB. Slew rate tuning. Bits 0-2 select control of the slew and bit 3	0
8	SLEW BIT 1	selects External Slew or Internal Slew.	0
9	SLEW BIT 2	← Slew MSB	0
10	SLEW BIT 3	← Ext Slew/Int Slew bit (1 = Internal Slew). If this bit (bit 10) is set then the internal slew resistor of 250K is used. This internal resistor is subject to the normal heat variations of the chip while in operation.	0
11	MASK_PHASE	Selects between 7.5° and 15° mask time (0=15°, 1=7.5°)	

Figure 2: The following diagram explains bits 5 "SYNTH HALL" and the effect it has on the pin named SYNTH_HALL



Frequency Locked Loop Coarse Counter (Reg 5)
This register contains the "coarse" FLL counter value for the FLL. This register gives a worst case resolution of 16µs with the worst case (i.e. slowest) 4MHz clock and has a valid range of 001 to FFF hex.

Reg: 5
Name: FLL Coarse Counter Register
Type: Write Only

BIT	LABEL	DESCRIPTION	@POR
0	CLATCH BIT 0	FLL Coarse counter LSB	0
1	CLATCH BIT 1		0
2	CLATCH BIT 2		0
3	CLATCH BIT 3		0
4	CLATCH BIT 4		0
5	CLATCH BIT 5		0
6	CLATCH BIT 6		0
7	CLATCH BIT 7		0
8	CLATCH BIT 8		0
9	CLATCH BIT 9		0
10	CLATCH BIT 10		0
11	CLATCH BIT 11	FLL Coarse counter MSB	0

Frequency Locked Loop Fine Counter (Reg 6)
This register contains the "fine" counter value of the FLL. The worst case resolution (i.e. with a 4MHz clock) is 1µs. **It is important that the most significant bit of this register must be a zero when a write is made.** Valid writes to this register must be between 001 and 7FF hex.

Reg: 6
Name: FLL Fine Counter Register
Type: Write only.

BIT	LABEL	DESCRIPTION	@POR
0	FLATCH BIT 0	FLL Fine counter LSB	0
1	FLATCH BIT 1		0
2	FLATCH BIT 2		0
3	FLATCH BIT 3		0
4	FLATCH BIT 4		0
5	FLATCH BIT 5		0
6	FLATCH BIT 6		0
7	FLATCH BIT 7		0
8	FLATCH BIT 8		0
9	FLATCH BIT 9		0
10	FLATCH BIT 10		0
11	FLATCH BIT 11	FLL Fine counter MSB -NOTE: On a write to this register, this bit must be zero.	0

Frequency Locked Loop Fine Error Counter (Reg 7)

This register contains the error detected between the "fine" counter value of the FLL and the actual spindle rotation time (in either mechanical or electrical mode).

Reg: 7
Name: FLL Fine Error Counter Register
Type: Read Only

BIT	LABEL	DESCRIPTION	@POR
0	FINEC BIT 0	FLL Fine error count LSB	0
1	FINEC BIT 1		0
2	FINEC BIT 2		0
3	FINEC BIT 3		0
4	FINEC BIT 4		0
5	FINEC BIT 5		0
6	FINEC BIT 6		0
7	FINEC BIT 7		0
8	FINEC BIT 8		0
9	FINEC BIT 9		0
10	FINEC BIT 10		0
11	FINEC BIT 11	FLL Fine error count MSB	0

CIRCUIT OPERATION

General

This device includes a sensorless spin driver, VCM driver, power sequencing, actuator retraction with dynamic braking, serial interface for a microprocessor and frequency locked loop for speed control. The device is register based and designed to operate via either 3V or 5V power supply.

POR & Under Voltage

The L6260 has an on chip power monitoring system that controls all aspects of powering up, Power On Reset of the Logic (POR), low voltage detection and power down sequencing. The circuitry consists of a Bandgap reference generator, hysteresis comparitor (for low voltage detection) and a POR timer circuit (which controls the duration of the reset).

Four external pins determine the behavior of this circuit.

- UV1 & UV2: These two pins are provided to the user to connect to the supply voltages for low voltage detection. The voltage on these pins is compared to the internal Bandgap voltage to determine if a low voltage on one of the supply pins has been detected. The comparitor has built in hysteresis to reduce the effects of noise on the supply lines triggering a false POR. In other words, if either one of these inputs falls below 1.25V then the supply is regarded as being "under voltage". Normally one of these pins will be connected to allow a sensing of a 3V supply and the other to the 5V supply but this is arbitrary
- POR_DLY: This is a pin from which a capacitor can be connected to ground. This sets the duration of the reset state of the this chip. On power up, an internal current source charges the capacitor with a current of approximately 2mA. When the voltage on this pin reaches the bandgap voltage, the chip comes out of its reset state. The duration of this reset is determined by the size of an external capacitor to ground.
- POR: The POR pin is an output from the chip for resetting other devices.

APPLICATION DIAGRAM

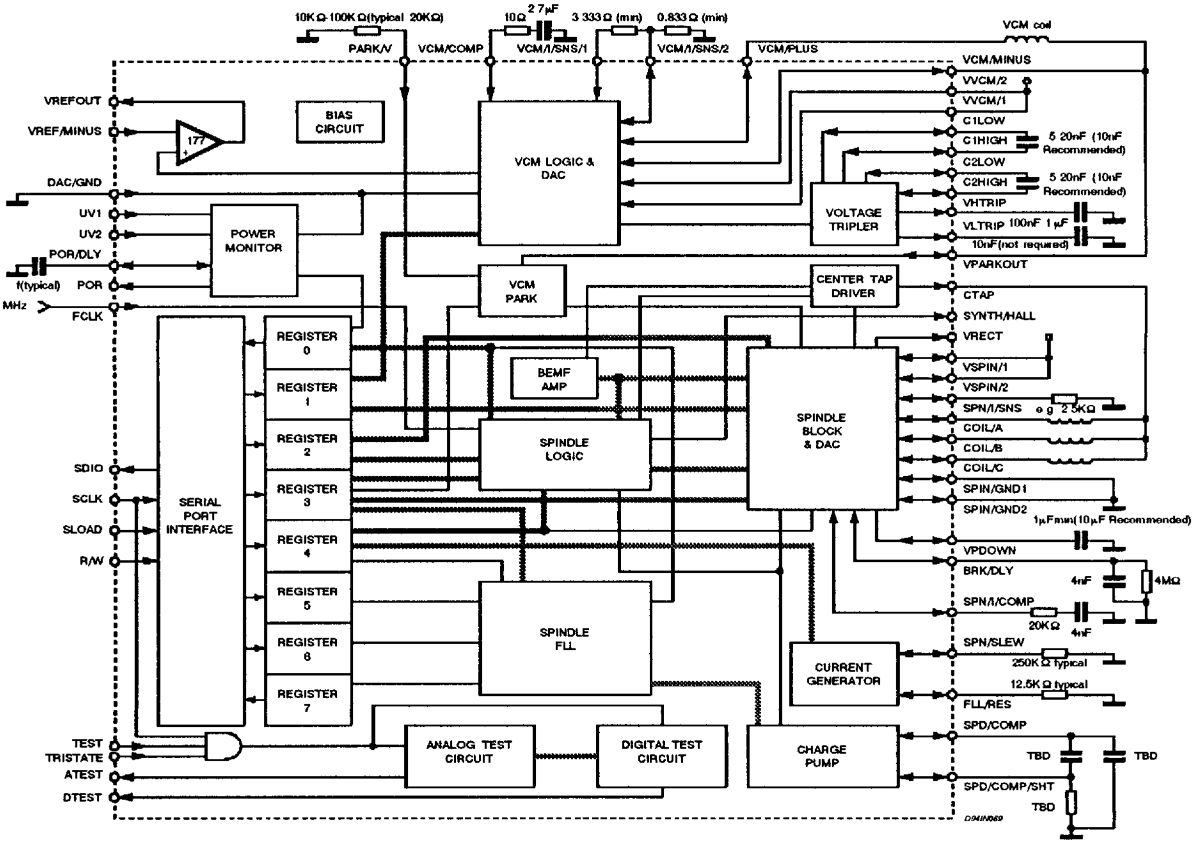
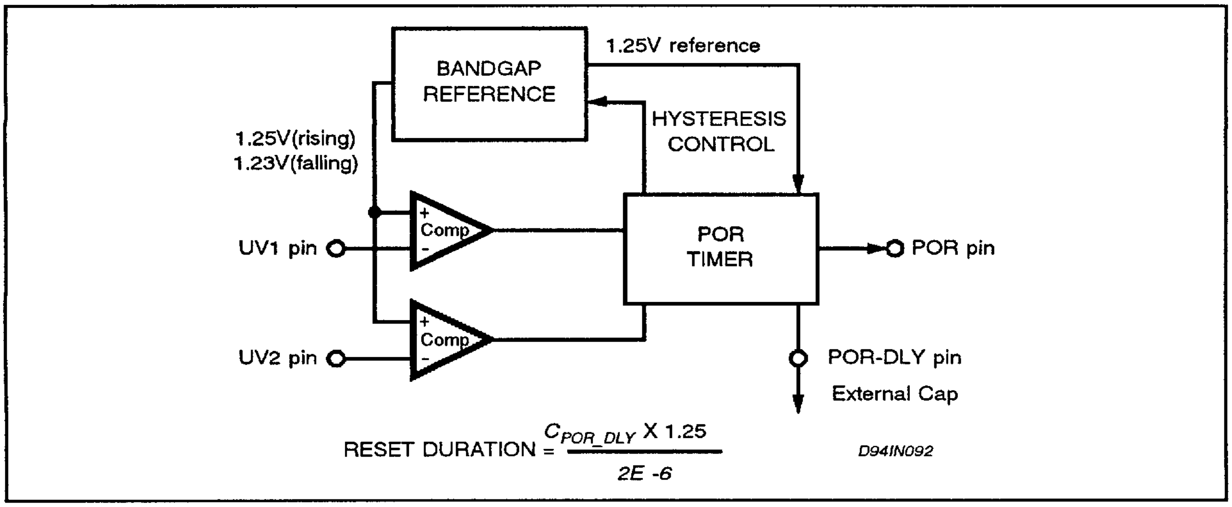


Figure 3.



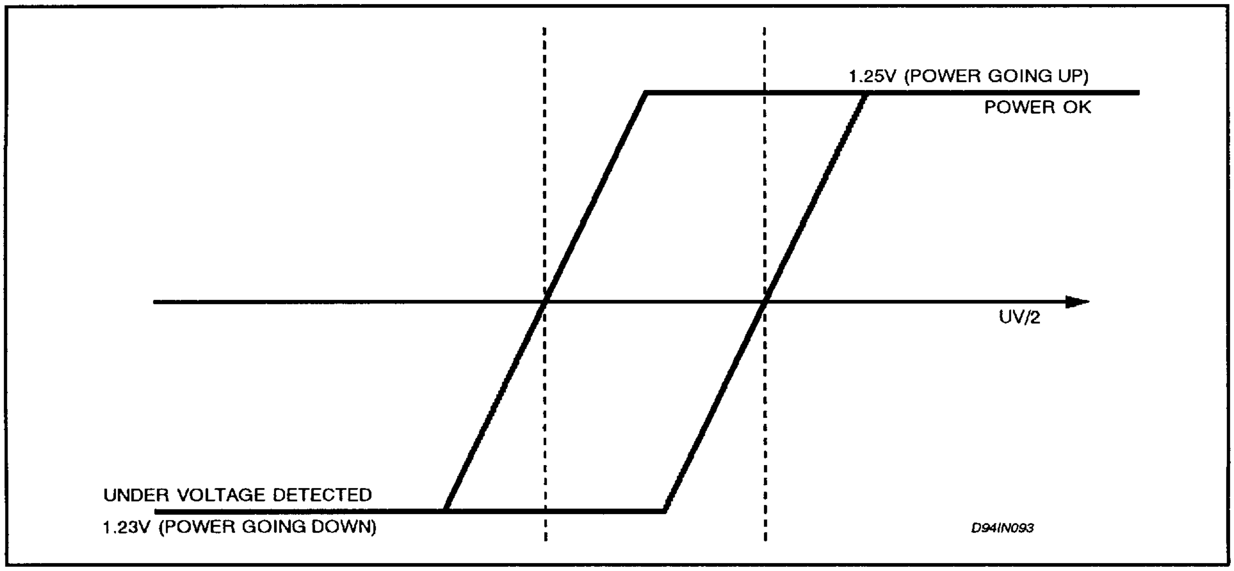
$$\text{RESET DURATION} = \frac{C_{POR\_DLY} \times 1.25}{2E\text{-}6}$$

POR Parameters

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
C_{PORDLY}	POR delay capacitor	220	2200	4700	pF
T_{delay}	Delay time	(*)	(*)	(*)	
UV_{rise}	Rising edge reference		1.25		V (**)
UV_{fall}	Falling edge reference		1.23		V (**)
T_{UVD}	Under voltage detect to POR low			250	ns

(*) See previous equation
(**) See hysteresis transfer function below

Figure 4: Hysteresis Comparitor Transfer Characteristic for Under Voltage Detection.



The duration of the brake delay is defined by an external resistor and capacitor connected to the brake delay pin (BRK_DLY). Charge stored in an external capacitor connected to the Voltage Tripler (VPDOWN) is used to supply the brake delay *circuit after the loss* of power.

During the application of power to the IC, the power on reset signal (POR) is asserted, forcing all registers to their default state (see @POR column of the register definitions) and disabling the VCM and spindle drivers. Once the supply voltage has exceeded the Voltage Good (VGT) threshold, the POR delay begins. When this delay has expired, POR is de-asserted. It is this delay whose duration is determined by an external capacitor connected to the POR_DLY pin.

When a low voltage condition is detected (the supply voltage falls below the VGT) the following happens (in order):

1) Internal registers are reset and POR is asserted.
2) The automatic parking of the actuator is enabled and the brake delay starts.
3) After the brake delay expires, all low side drivers are enabled to brake the spindle.

Serial Interface

The serial interface is designed to be compatible with the Intel 80196 (and other similar micros) serial interface but is capable of faster data rates, up to 10 MHz. All read and write operations must consist of 16 bits, with the 80196 this would be two 8 bit accesses. The first four bits are address and the next 12 are data. If the address is a read register then the L6260 will use the SCLK from the system to shift out 12 bits of data from the addressed register. The system must provide 16 SCLK pulses to insure that the read operation completes.

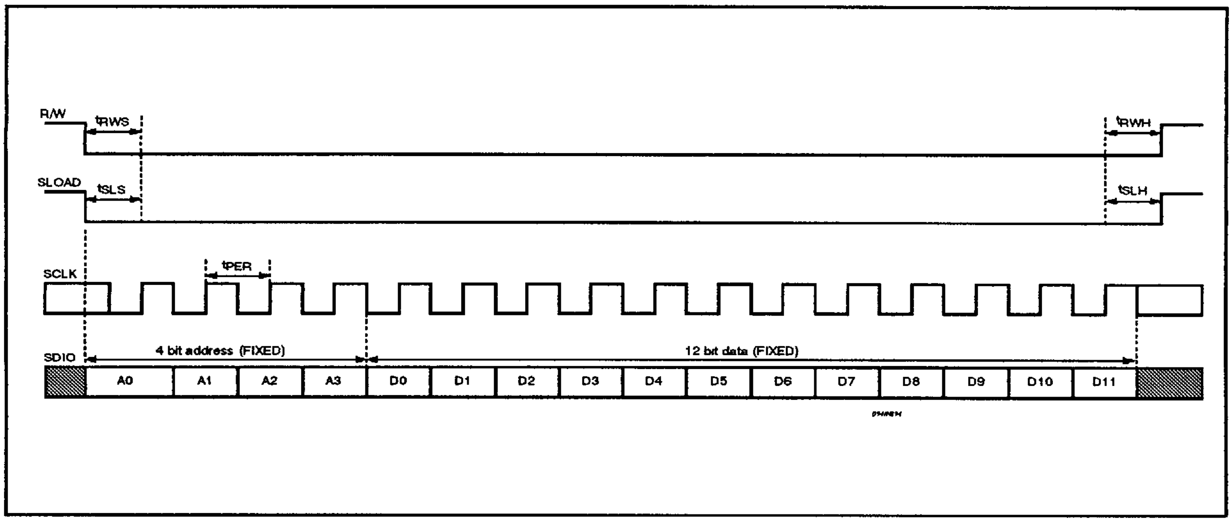
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{RWS}	R/$\overline{W}$ setup time to SCLK going high	100			ns
t_{SLS}	SLOAD setup time to SCLK going high	100			ns
t_{RWH}	R/$\overline{W}$ hold time after SCLK going high	100			ns
t_{SLH}	SLOAD hold time after SCLK going high	100			ns
t_{SCKD}	SCLK high to Data Valid		30	50	ns
t_{RWD}	R/$\overline{W}$ High to Data Valid Data bit D[0] valid from HiZ		30	50	ns
t_{AS}	Address setup time to SCLK going high	30			ns
t_{DS}	Data setup time to SCLK going High	30			ns
t_{AH}	Address Hold after SCLK going high	10			ns
t_{DH}	Data Hold time after SCLK going High	10			ns
t_{SDZ}	SDIO tri-state after SLOAD going High	30			ns
t_{RWZ}	SDIO tri-state after R/$\overline{W}$ going low	30			ns
t_{PER}	Minimum SCLK period	100			ns
t_{REC} (*)	Recycle - Time between successive accesses	100			ns

(*) For 10MHz system clock operation (in other words. 1 or more clock cycles of SCLK).

Serial Interface Truth Table

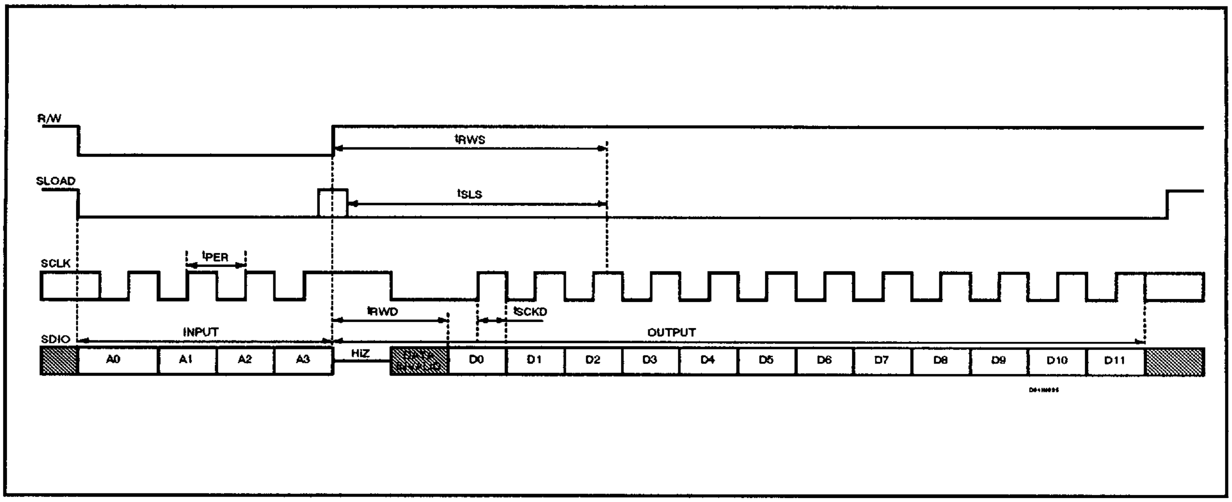
R/$\overline{W}$	SLOAD	SDIO	DIRECTION
1	1	Tri-state (Port unselected)	Tri-state
0	1	Tri-state (Port unselected)	Tri-state
0	0	Address/Data input	Input
1	0	Data output	Output

Figure 5: Serial Write Timing Diagram



The write cycle has a fixed address and data length. Four bits of address and 12 bits of data must be clocked in to allow the data to be loaded into the desired register. The write cycle is initiated by setting SLOAD and R/W low. Setting R/W low causes the SDIO line to be tri-stated for data input. SLOAD low enables the internal counter to increment on the rising edge of SCLK. The address and data are clocked into the chip serially on each rising edge of SCLK as shown above. When both the 4 bits of address and the 12 bits of the data have been clocked in, then the addressed register will be written to with the provided data. Setting SLOAD high will clear the internal logic and tri-state the SDIO line. This also provides a way of safely aborting a write by simply forcing SLOAD high. NOTE: SLOAD must be kept low during the entire duration of the 16 write clocks.

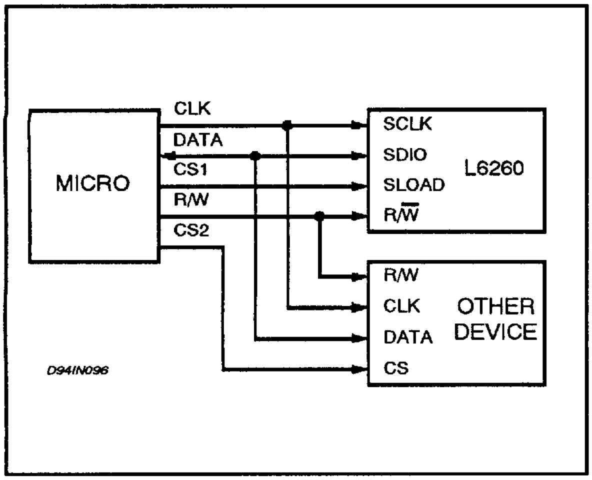
Figure 6: Serial Read Timing Diagram



The read cycle is initiated by setting SLOAD low and clocking in a valid read address. Only four bits of address are necessary, if more than four bits are clocked in, the four MSBs will be ignored (i.e. only the first four bits will be used). If a valid address is detected, the rising edge of R/W will load the desired register into the internal serial/parallel register ready for clocking out. The data in the serial/parallel register is then serially clocked out on every rising edge of SCLK (LSB is clocked out first). Additional padded bits clocked out will be zero.

Note: If SLOAD is set low with R/W high, the current contents of the internal shift register can be clocked out. This is useful for a "read back" of the data last written into the required register.

Figure 7: System Level Interface



System clock (FCLK input) and its Pre Scale

System clock (FCLK input) and its Pre Scale The chip must be clocked via the FCLK pin at one of two possible input frequency ranges, 4-6MHz or 8-12MHz. The required range is set up via register bit 4.3 (System Control Register B, Sys Clock Prescale bit) where 0 selects the lower frequency of 4-6MHz and a 1 selects the higher input range of 8-12MHz.

VCM System

The following functions are provided: Voltage controlled retract including sourcing and sinking current, two quadrant retract, with "Spindle Powered" or "Commanded" Retract. The VCM DAC register is accessed via the serial port and allows the DAC value to be changed. This drives the VCM DAC and in turn the VCM driver.

VCM Compensation and Loop Equations

This information will be included in the next version of this datasheet.

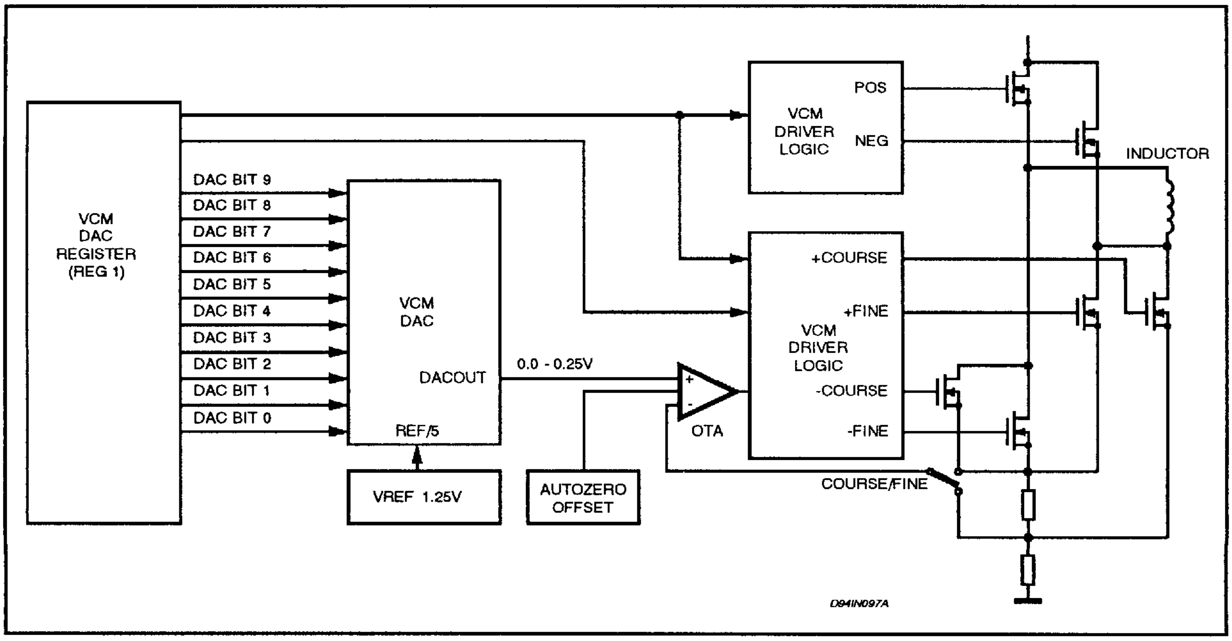
VCM Driver

The VCM driver is capable of supplying +/- 300 mA of current although higher peak currents are acceptable for short periods of time. Closed loop control of the load current is provided by the power amplifier which consists of an error amplifier followed by an H bridge output section. The loop is compensated by an external RC network connected to the VCM_Comp pin.

The direction of the current flowing in the bridge is determined by the sign bit. The H bridge has two pairs of lower drivers, only one of which is selected at a given time. Such a configuration makes it possible to choose between two values of transconductance by selecting the appropriate pair of drivers. This gain selection is accomplished using the VCM DAC Register.

The VCM current sense amplifier produces a voltage which is proportional to the current flow in the voice coil. When the system is operating in a linear fashion, the steady state voltage at the VCM_I_SNS pins is approximately equal to the voltage commanded by the DAC. However, under

Figure 8.



certain transient conditions, the control loop which regulates the load current can recirculate, causing the VCM_I_SNS voltage to be different from the commanded voltage. This information is useful in optimizing the command profile during a seek.

The retract voltage is set by external components.

The current loop bandwidth is greater than 20Khertz.

VCM DAC

The VCM DAC consists of 10 bits via the DAC, 1 bit sign and 1 gain bit. However, externally this can be viewed as being a single 11 bit signed value with a gain bit in the MSB position. The sign bit controls the direction of the current. Positive values of the DAC are regarded as moving the actuator towards the inside diameter (this is required for parking/braking). The magnitude is converted to a voltage which is used for closed loop regulation of the magnitude of the load current. The gain bit

Retract

Automatic actuator retraction is initiated when any of the following conditions occur: disabling the spin system while the VCM system is still enabled, excessive junction temperature (thermal shutdown), loss of power or microprocessor issued retract. In all cases except the loss of power, the voltage applied to the voice coil is limited by an active clamp. When power is lost, the BEMF generated by the spinning motor is rectified and applied across the voice coil to perform the parking operation.

Command retract is activated via the System Control Register.

VCM Gain Considerations

$$I_{OUT} = \pm 0.25 \cdot \frac{\text{DAC\_VALUE}}{1024} \cdot \frac{1}{R_{S1}}$$ (High current setting)

or

$$I_{OUT} = \pm 0.25 \cdot \frac{\text{DAC\_VALUE}}{1024} \cdot \frac{1}{R_{S1} + R_{S2}}$$ (Low current setting)

Modes of Operation

The L6260 provides for four different modes of operation, namely, Unipolar, Bipolar, Tripolar and Tristate. The Tripolar mode is included for achieving reliable start-ups in a stuck rotor condition (lengthening drive life-time). These modes are initiated via the System Control Register A, bits 7 & 8 as follows:

	Bit 6	Bit 7	# of drivers on
Tristate	0	0	None
Unipolar	0	1	1 low side, no high side
Bipolar	1	0	1 low side and 1 high side
Tripolar	1	1	1 high side and 2 low side OR 2 high side and 1 low side

Spindle compensation and Loop Equations

This material will be available in the next version of this datasheet.

Spindle State Machine

The spindle state machine provides the logic and timing signals to the spindle driver in support of the various modes of operation.

When the spindle driver is disabled (via the System Control Register), the state machine puts the spindle driver into a high impedance mode and places all spindle related circuit into a reduced power mode.

After a POR, at boot up or after RESET (via System Control Register) the state machine is in the known state as defined by the System Control Registers (A & B) initial condition after POR (see the @POR column of these registers).

When in Unipolar mode the commutation sequence is CTR/IA, CTR/IB CTR/IC where IA = lower A driver (NOTE: Unipolar mode is only guaranteed at 3V operation). In Bipolar the commutation sequence is uA/IB (upper A and lower B), uA/IC, IC/uB, uB/IA, IA/uC and uC/IB. In Tripolar mode the state machine does not auto commutate, the microprocessor must increment the state. The sequence is uA/IBC (upper A and lower B & C), uAB/IC, uB/IAC, uCB/IA, uC/IAB and uAC/IB. The Uni/Bi/Tri-polar operation is set by two bits in the System Control Register A (3.7-3.8) described above (Modes of Operation).

If the RUN/SEARCH bit (System Control Register A, bit 4) is false or 0 (SEARCH mode), the commutation state only increments when the INC STATE bit is strobed (also in the same register, bit 3). If the RUN/SEARCH bit is true or 1 (RUN mode) the state will increment either on a INC STATE strobe or if a qualified BEMF CROSSING occurs the state will increment after the commutation delay times out.

If either THERMAL=1 (register.bit 0.0) or the POR=0, all the drivers are turned off. Tristate is the default mode of operation at power up.

Period counters and delay and masking functions

The period counter is an internal 11 bit register that is used to time the interval between successive zero crossings. Whenever a zero crossing is encountered, the period counter is loaded into both a mask counter (9 bits) and a delay counter (11 bits). The period counter is automatically reset to count the next zero crossing period.

The clock used for the period and mask counters is a function of the system clock. If the FCLK (the system clock) is set to the 8-12MHz range then *the period* and mask counters are clocked at 1/64 of the system clock, other wise the registers are clocked at 1/32 of the system clock. The delay counter clock is programmable via the SPIN COM DLY bits in the Spin Control Register (2.8-2.11). This value is used to divide down the system clock. Since there is 60 electrical degrees between zero-crossings, the delay counter can provide 1.875 through to 28.125 electrical degree delay at 1.875 degree increments.

When the period counter reaches zero, the masking of the zero-crossing starts (to avoid seeing current recirculation spikes). The delay counter then starts to count down and when it reaches zero the masking of the BEMF is released so that zero crossings can once again be detected. The masking hides the commutation of the motor which takes place during the mask.

The clocking frequency of the mask and delay counters is identical. However, the delay is 11 bits and the mask only 9 bits. This means that the mask can provide 15 electrical degrees of masking time. In the System Control Register B, bit MAKE_PHASE (4.11) a bit value of zero gives this 15 electrical degrees mask time but a one gives 7.5 electrical degrees of mask.

Speed Control & F.L.L.

The rotational position of the motor is inferred from the BEMF wave form generated by the floating coil. The chip uses the instant of a particular zero-crossing and the period between successive zero crossings to dictate the commutation timings. The complete control loop is on chip and the speed is controlled by a reference clock FCLK.

The speed control loop uses a frequency locked loop which in conjunction with an external compensation network brings the frequency of the tachometer signal to be equal to the internally generated reference frequency. The tachometer signal can either be the BEMF signal divided down to a once per mechanical revolution signal or an externally generated tachometer signal, sector burst. The output of the speed control is a current demand signal that goes to the Spindle Driver.

The spindle current and the commutation delay is programmed via the Spin Control Register. There is a "fine" and a "coarse" counter that defines the speed of the motor.

In more detail, the two registers are used in conjunction with two down counters which form a frequency detector that in turn creates feedback through to a charge pump to maintain the motors speed regulation.

The course counter is 12 bits and is clocked at $1/64^{th}$ the rate of the frequency clock (FCLK). The fine counter is clocked at 1/4th FCLK. The on chip Frequency Locked Loop (FLL) uses the electrical cycle pulses ("ec pulse") to time the motors rotation. Upon the first ec pulse, the course register's contents (loaded via the serial port) is loaded into the internal course counter is then loaded from its corresponding register. The fine counter then also immediately starts to count down. In theory (but not normally in run mode, possibly at start up) the fine counter could count down through zero an continue counting down the 2's complement of the original fine counter value.

The period between the start of the course counter and the zero crossing during the fine counter operation is the programmed period. Any differences between the desired period and the ec pulse (zero crossing) is the error in the transconductance loop and corrective action is take by the charge pump. This error is a number given from a counter starting when the fine counter reaches zero and resetting when the BEMF pulse occurs. The vice versa happens if the BEMF anticipate the ending of the fine counter. The error number is loaded in REG. 7.

The course and fine counter arrangement is guarateed to work in all possible circumstances (providing there is enough BEMF). For example if the zero crossing is within or outside the fine window or even if the zero crossing is in the course register range. This system will even work if the zero crossing occurs across multiple course/fine cycles.

The FLL has a prescaler (defined by the System Control Register bits EL_MECH and 8_12P (3.10 & 3.5) that changes the cycle counting mechanism between electrical, 8 pole or 12 pole (i.e. dividing the ec clock by 1,4 or 6) respectively.

The procedure for setting the motor speed is as follows:

let's call T0 this quantity. $T0 = \frac{60}{SPEED}$

Doing $\frac{T0 \cdot 0.9 \cdot FCLK}{64}$ we obtain Ncourse e. g.

the number to load in the course register. If this number exceed 4096 the desired speed is not achievable. Let's call ErrNc the decimal part of Ncourse doing

$\frac{T0 \cdot 0.1 \cdot Fclk}{4} + ErrNc \cdot 16$ we obtain Nfine e.g.

the number to load in the fine register. If this number exceed 2048 all the procedure must be repeated changing 0.9 with 0.91 and 0.1 with 0.09 and so on.

The spindle is enabled via the System Control Registers.

The slew rate is defined by attaching a resistor to ground from the SPN_SLW pin. The current loop has a compensation RC network on the SPN_I_COMP pin and the sense resistor is attached to the SPN_I_SNS pin (to ground).

Figure 9.

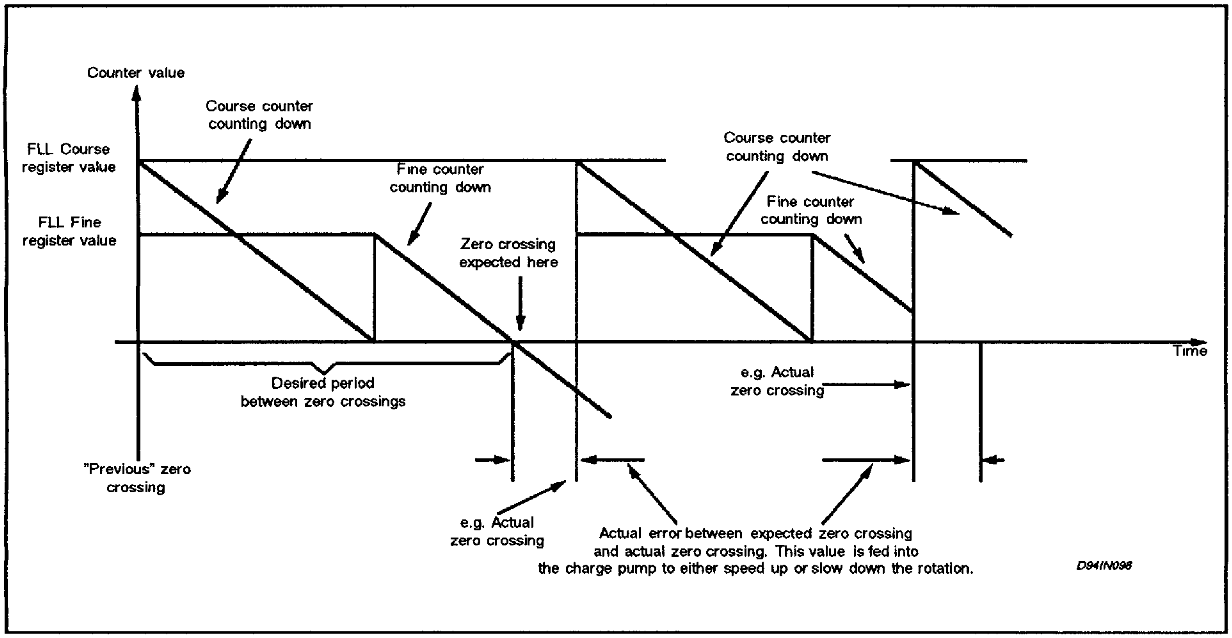
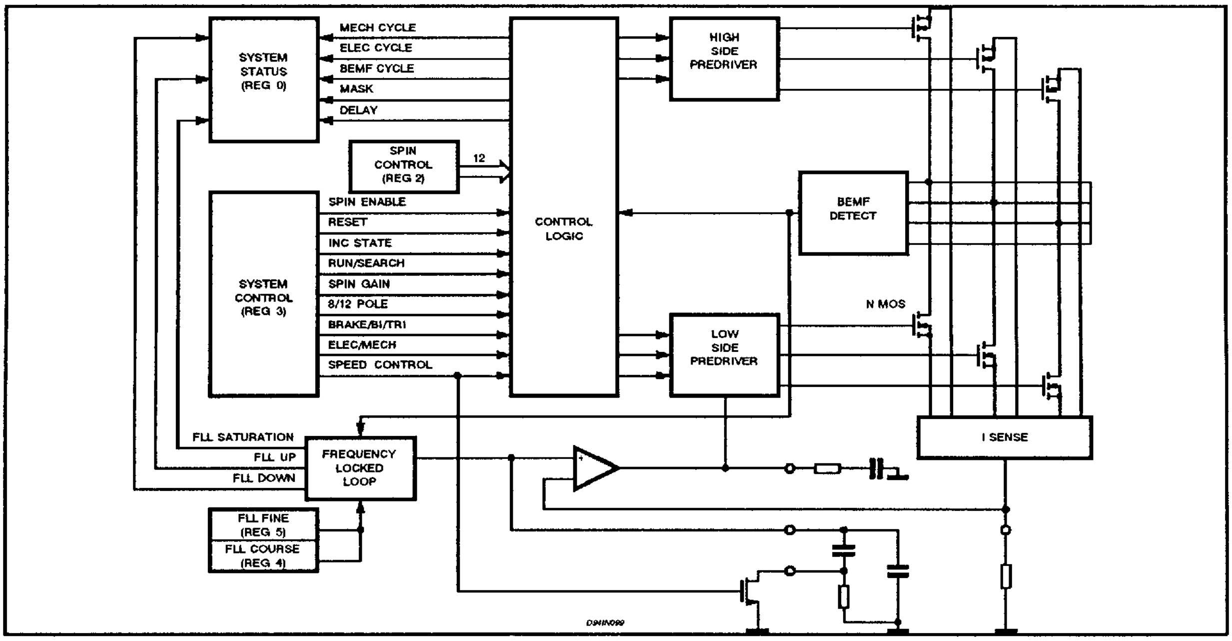


Figure 10.



A Synthetic Hall output is also provided from this chip once per electrical or BEMF crossing.

Using the remote current sensing of the Spindle current

The remote current sensing allows the connection of the power drivers directly to ground. The benefit here is the elimination of the external sense resistor.

Under normal operation there is a 500:1 difference between the current seen on the sense pin and the current in the spindle power drivers. At start up this ratio is changed to 2500:1 (five time the normal operation). The recommended voltage at the sense pin is approximately one volt.

Example

Assuming that your motor requires 200mA run current then the sense current would be 200/500 = 400μA. Therefore for 1 volt at the sense pin a 2500 Ohm resistor is required (R = 1/400μA). Also assuming you require 1 Amp start-up current. You need to change the sense range to 5X. This also gives 1A/2500 = 400μA or 1V on a 2500 Ohm resistor.

In the normal "at-speed" running the voltage at this pin will vary between 0 and 2 volts approximately (e.g. when using the FLL). When using the spindle DAC the voltage swing is from 0 to 1.25 Volts

Using the Spindle DAC for Start-Up

When the SPEED bit in the System Control Register A (Register 3.9) is set (to 1), the speed control is given to the DAC (i.e. control is removed from the FLL). The normal method of start-up is achieved using the DAC rather than the FLL. However the FLL can be used from zero speed with an align-and-go algorithm but start-up will be slower. The 8-bit DAC gives 4.88mV per step with a maximum voltage of 1.25V.

Example

If 1 amp start-up current is required and a sense resistor of 2.5K Ohms is to be used then the high gain mode would be required and the DAC voltage set to 1 Volt.

When the CPU has determined that the spindle is near or at-speed the DAC voltage should be reprogrammed to the nominal voltage that the charge pump requires for steady-state operation. For example if the motor requires 100mA for steady-state operation, a 2.5K Ohm sense resistor then the sense FET gain needs changing down to the 500:1 setting (low gain) and the DAC needs to be set to 0.5V.

Since the DAC output is shorted to the charge pump capacitors during "DAC control" this leaves the correct voltage on these capacitors when the switch is made to the FLL control. This is advantageous as it reduces the settling time of the motor.

Power Devices

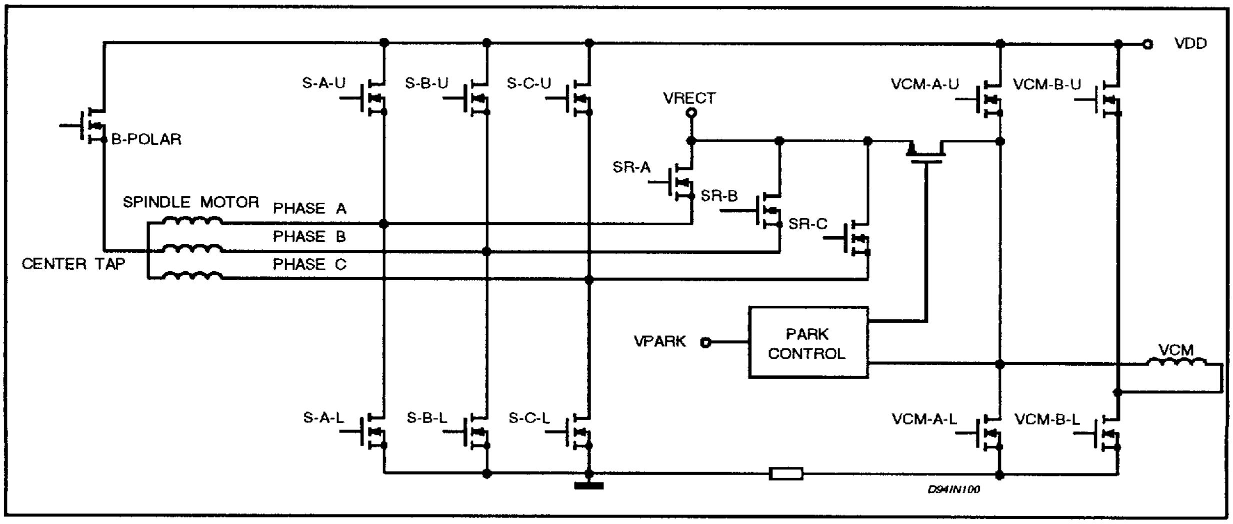
When S_BIPLOAR (internal) is turned on and saturated when the spindle driver is placed in unipolar mode and has an Rdson of 1 Ohm (worst case over temperature). To support retract without requiring an isolation diode the transistor is designed so as not to conduct current from source to drain even if the supplies Vp and Vdd are at ground and the source is at a positive voltage.

S_A_U, S_B_U and S_C_U are the upper spindle drive transistors. They are active whenever the drive is in bipolar mode and can be turned on in pairs in tripolar mode. To support retract without requiring an isolation diode these transistors are designed so as to not conduct current from source to drain even if the supplies Vdd and Vp are at ground and the source is at a positive voltage.

S_A_L, S_B_L and S_C_L are the lower spindle drive transistors. They are active in unipolar, bipolar and tripolar drive. In linear mode the active transistor's gate drive is controlled so as to bring the current in the motor to the level set by the speed control compensation circuit or the current limit DAC.

The power circuits will be as shown in the following figure 11.

Figure 11.



Synth Hall

The Synth Hall pin can be programmed to provide one of two possible output wave forms (see register definitions). By setting the SYNTH_HALL bit in register System Control Register B (4.5) to zero, the signal is a once per BEMF crossing signal which has the same phase as the BEMF amplifier on chip with all the noise and false transitions removed. With this bit set to one, a once per electrical cycle signal with 50% duty cycle is produced.

Brake

The BRAKE mode commands a retract & then turns on the lower three drivers, S_A_L, S_B_L and S_C_L, to cause immediate braking of the spindle.

Retract

The retract voltage is defined by a resistor to ground from the RETRACT_V pin.

Test Circuits

1) I/O Mapping Test Mode. This mode is activated by taking the TEST pin high and holding the TRISTATE pin low. This puts the device into a test mode that allows certain pins to be directly internally connected to other pins for the purpose of testing continuity of solder joints on a board. The following table defines which pins are I/O mapped and which is an input and which is an output. Notice that I/O mapped pins in one group are not physically adjacent in the package allowing more thorough testability.

INPUT PIN #	INPUT PIN NAME	OUTPUT PIN #	OUTPUT PIN NAME
20	R/$\overline{W}$	11	SDIO
9	SLOAD	11	SDIO
10	SCLK	22	SYNTH_HALL
12	FCLK	22	SYNTH_HALL
50	UV1	5	$\overline{POR}$
51	UV2	5	$\overline{POR}$

2) Digital and Analog Test Mode. This mode is activated by taking both the TEST pin and TRISTATE pin high. Once this has been done the SCLK pin of the serial interface is used to clock out digital data through the DTEST pin. Simultanously, the ATEST pin cycles through carrying different analog signals from around the chip.

SCLK	ATEST pin carries...	DTEST pin carries...
1	Nominal Bandgap Voltgage (normally 1.25V)	Postive/Negative incrementing of the FLL
2	Low Bandgap Voltage (normally 1.23V)	Spindle mask
3	Bias Voltage (normally 0.5V)	Spindle delay
4	Spindle DAC Output	FCLK/16 or FCLK/32 depending on CLK_PRESCALE bit in System Control Reg B (4.4)
5	VCM DAC Output	BEMF Comparitor output (raw)
6	Temperature Shutdown Voltage (input - used to alter the point at which thermal shutdown starts operation)	VCM predriver (A)
7	Connected to the A gate of the spindles Low Side Driver. Allows Rds(on) testing.	VCM predriver (F).

3) Tristate Test Mode. This mode is activated by keeping the TEST pin low and taking the TRISTATE pin high. This disables the digital outputs, specifically SYNTH_HALL, POR & SDIO.

4) No Test Modes. All test modes are disabled by keeping the TEST pin & TRISTATE pin low

Sleep & Idle Functions

The chip has the following modes of operation

MODE	STATE	POWER LEVEL	POWER DISS.
Ready	Spin & VCM enabled	Full	10mA
Idle	Spin enabled, VCM disabled	Reduced	5mA
Sleep	Both spin and VCM disabled	Minimum	200μA (typical) 1000 μA (max)
INVALID	Spin disabled, VCM enabled		

If the spindle is disabled while the VCM is enabled the automatic parking function is invoked.

TQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.50	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)