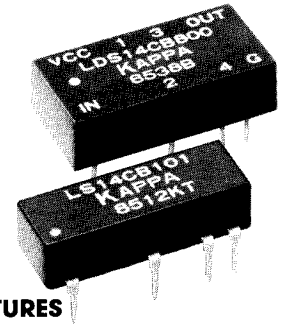
SERIES LS14/LDS14 LSTTL (14-PIN) 5-TAP

LOW POWER SCHOTTKY DELAY LINE



FEATURES

- Available in Auto-Insertable (LS14) and Standard (LDS14) 14-Pin Package
- TTL Low Power Schottky interfaced
- 5 equally-spaced taps
- Risetime: 8 ns Max(5)(6)
- Drives up to 20 Low Power TTL loads
- Total delays from 50-500 ns

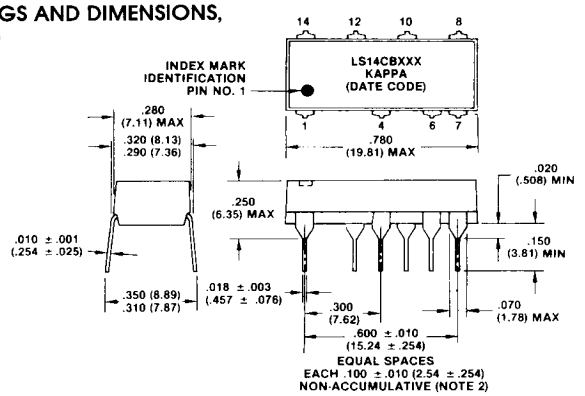
RECOMMENDED OPERATING CONDITIONS

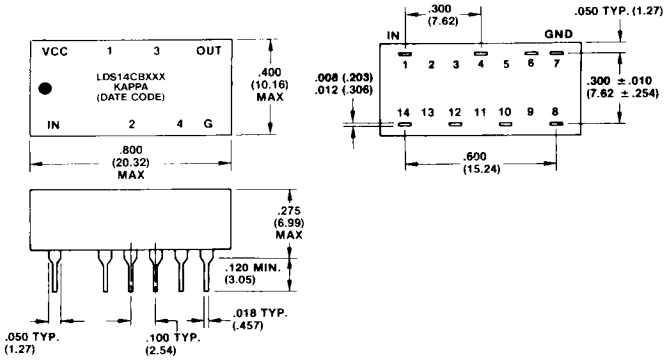
		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.00	5.25	V
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{IK}	Input Clamp Current			−18	mA
I_{OH}	High-Level Output Current			−0.4	mA
I_{OL}	Low-Level Output Current			8	mA
T_A	Operating Free-Air Temperature	0	+25	+70	°C

DC ELECTRICAL CHARACTERISTICS **TEST CONDITIONS**

V_{OH}	High-Level Output Voltage	V_{CC} = min, V_{IH} =min, I_{OH} = max	2.7	3.4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = min, V_{IL} = max, I_{OL} =max			0.4	V
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_I = I_{IK}			−1.5	V
I_{IH}	High-Level Input Current	V_{CC} = max, V_{IN} = 2.7V			20	μA
		V_{CC} = max, V_{IN} = 7.0V			0.1	mA
I_{IL}	Low-Level Input Current	V_{CC} = max, V_{IN} = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = max, V_{OUT} = 0, one output at a time	−20		−100	mA
I_{CCH}	High-Level Supply Current	V_{CC} = max, V_{IN} = OPEN			24	mA
I_{CCL}	Low-Level Supply Current	V_{CC} = max, V_{IN} = 0			24	mA
N_H	Fanout High-Level Output	V_{CC} = max, V_{OH} = 2.7V			20	LSTTL load
N_L	Fanout Low-Level Output	V_{CC} = max, V_{OL} = 0.5V			10	LSTTL load

MARKINGS AND DIMENSIONS, in (mm)





Marking and dimensions notes:

1. A notch may be substituted for PIN #1 Dot Index.
2. Each terminal is located within ±.010 of its nominal multiple of .100 along this longitudinal dimension relative to terminals 7 and 8.
3. Units may exclude terminals not shown in schematic.

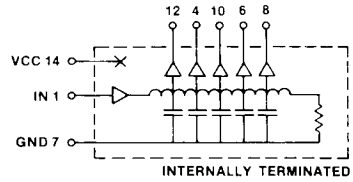
INPUT PULSE TEST CONDITIONS

E_{IN}	Pulse Voltage	3.1	3.2	3.3	V
T_{RI}	Pulse Rise-Time			2.0	ns
T_W	Pulse Width, of Total Delay	40	100		%
d	Duty Cycle		33.3	50	%

PART NUMBER	Total Delay (ns)(1) (2)	Tap Delay (ns)(1) (2)
LS14/LDS14CB500	**50**	**10**
LS14/LDS14CB750	75	15
LS14/LDS14CB101	**100**	**20**
LS14/LDS14CB251	250	50
LS14/LDS14CB501	**500**	**100**

Notes:

1. Delays measured at 1.5V level on leading edge only.
2. Delay tolerances: ±5% or ±2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: V_{CC} = Typ, T_A = Typ, E_{IN} = Typ, T_{RI} = max, T_W = Typ, P_{RR} = 1MHz (or d/tw, whichever is less), R_L 1 megohm and C_L 2pf.
3. Temperature coefficient of delay will vary, depending upon total delay, according to the formula: T_{PTA} = (100 + (25,000/T_{PLH})).
4. Delay will vary approximately 4% for every 5% change in supply voltage.
5. Risetime measured from 0.75V to 2.4V level.
6. Measured with no loads on taps.
7. **Other delays also available upon request.**



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