FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13701-8E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90570 Series

## MB90573/574/574C/F574/F574A/V570/V570A



## ■ DESCRIPTION

The MB90570 series is a general-purpose 16-bit microcontroller developed and designed by Fujitsu for process control applications in consumer products that require high-speed real time processing. It contains an I²C*2 bus interface that allows inter-equipment communication to be implemented readily. This product is well adapted to car audio equipment, VTR systems, and other equipment and systems.

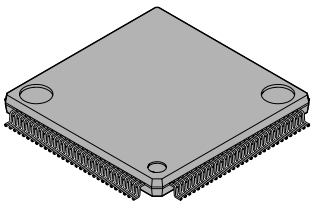
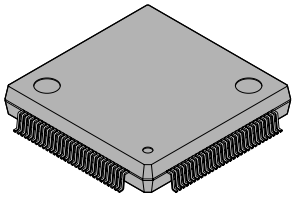
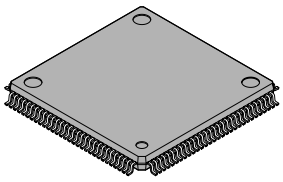
The instruction set of F²MC-16LX CPU core inherits AT architecture of F²MC*1 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90570 series has peripheral resources of an 8/10-bit A/D converter, an 8-bit D/A converter, UART (SCI), an extended I/O serial interface, an 8/16-bit up/down counter/timer, an 8/16-bit PPG timer, I/O timer (a 16-bit free run timer, an input capture (ICU), an output compare (OCU)).

*1: F²MC stands for FUJITSU Flexible Microcontroller.

*2: Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

## ■ PACKAGE

| 120-pin plastic LQFP | 120-pin plastic QFP | 120-pin plastic LQFP |
|---|---|---|
|  |  |  |
| (FPT-120P-M05) | (FPT-120P-M13) | (FPT-120P-M21) |

## ■ FEATURES

- Clock
  Embedded PLL clock multiplication circuit
  Operating clock (PLL clock) can be selected from 1/2 to 4× oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
  Minimum instruction execution time: 62.5 ns (at oscillation of 4 MHz, 4× PLL clock, operation at $V_{CC}$ of 5.0 V)
- Maximum memory space
  16 Mbytes
- Instruction set optimized for controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed
  4-byte instruction queue
- Enhanced interrupt function
  8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI²OS): Up to 16 channels
- Embedded ROM size and types
  Mask ROM: 128 kbytes/256 kbytes
  Flash ROM: 256 kbytes
  Embedded RAM size:6 kbytes/10 kbytes (mask ROM)
  10 kbytes (flash memory)
  10 kbytes (evaluation device)
- Low-power consumption (standby) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Hardware standby mode
- Process
  CMOS technology
- I/O port
  General-purpose I/O ports (CMOS): 63 ports
  General-purpose I/O ports (with pull-up resistors): 24 ports
  General-purpose I/O ports (open-drain): 10 ports
  Total: 97 ports
- Timer
  Timebase timer/watchdog timer: 1 channel
  8/16-bit PPG timer: 8-bit × 2 channels or 16-bit × 1 channel
- 8/16-bit up/down counter/timer: 1 channel (8-bit × 2 channels)

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- 16-bit I/O timer
  16-bit free run timer: 1 channel
  Input capture (ICU): Generates an interrupt request by latching a 16-bit free run timer counter value upon detection of an edge input to the pin.
  Output compare (OCU): Generates an interrupt request and reverse the output level upon detection of a match between the 16-bit free run timer counter value and the compare setting value.
- Extended I/O serial interface: 3 channels
- $I^2C$ interface (1 channel)
  Serial I/O port for supporting Inter IC BUS
- UART0 (SCI), UART1 (SCI)
  With full-duplex double buffer
  Clock asynchronized or clock synchronized transmission can be selectively used.
- DTP/external interrupt circuit (8 channels)
  A module for starting extended intelligent I/O service ($EI^2OS$) and generating an external interrupt triggered by an external input.
- Delayed interrupt generation module
  Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution
  Starting by an external trigger input.
  Conversion time: 26.3 µs
- 8-bit D/A converter (based on the R-2R system)
  8-bit resolution: 2 channels (independent)
  Setup time: 12.5 µs
- Clock timer: 1 channel
- Chip select output (8 channels)
  An active level can be set.
- Clock output function

## ■ PRODUCT LINEUP

| Item \ Part number | | MB90573 | MB90574/C | MB90F574/A | MB90V570/A |
|---|---|---|---|---|---|
| Classification | | Mask ROM products | | Flash ROM products | Evaluation product |
| ROM size | | 128 kbytes | 256 kbytes | | None |
| RAM size | | 6 kbytes | 10 kbytes | | |
| CPU functions | | The number of instructions: 340<br>Instruction bit length: 8 bits, 16 bits<br>Instruction length: 1 byte to 7 bytes<br>Data bit length: 1 bit, 8 bits, 16 bits<br>Minimum execution time: 62.5 ns (at machine clock of 16 MHz)<br>Interrupt processing time: 1.5 μs (at machine clock of 16 MHz, minimum value) | | | |
| Ports | | General-purpose I/O ports (CMOS output): 63<br>General-purpose I/O ports (with pull-up resistor): 24<br>General-purpose I/O ports (N-ch open-drain output): 10<br>Total: 97 | | | |
| UART0 (SCI), UART1 (SCI) | | Clock synchronized transmission (62.5 kbps to 1 Mbps)<br>Clock asynchronized transmission (1202 bps to 9615 bps)<br>Transmission can be performed by bi-directional serial transmission or by master/slave connection. | | | |
| 8/10-bit A/D converter | | Resolution: 8/10-bit<br>Number of inputs: 8<br>One-shot conversion mode (converts selected channel only once)<br>Scan conversion mode (converts two or more successive channels and can program up to 8 channels.)<br>Continuous conversion mode (converts selected channel continuously)<br>Stop conversion mode (converts selected channel and stop operation repeatedly) | | | |
| 8/16-bit PPG timer | | Number of channels: 1 (or 8-bit × 2 channels)<br>PPG operation of 8-bit or 16-bit<br>A pulse wave of given intervals and given duty ratios can be output.<br>Pulse interval: 62.5 ns to 1 μs (at oscillation of 4 MHz, machine clock of 16 MHz) | | | |
| 8/16-bit up/down counter/ timer | | Number of channels: 1 (or 8-bit × 2 channels)<br>Event input: 6 channels<br>8-bit up/down counter/timer used: 2 channels<br>8-bit re-load/compare function supported: 1 channel | | | |
| 16-bit I/O timer | 16-bit free run timer | Number of channel: 1<br>Overflow interrupts | | | |
| | Output compare (OCU) | Number of channels: 4<br>Pin input factor: A match signal of compare register | | | |
| | Input capture (ICU) | Number of channels: 2<br>Rewriting a register value upon a pin input (rising, falling, or both edges) | | | |

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| Item \ Part number | MB90573 | MB90574/C | MB90F574/A | MB90V570/A |
|---|---|---|---|---|
| DTP/external interrupt circuit | Number of inputs: 8<br>Started by a rising edge, a falling edge, an “H” level input, or an “L” level input.<br>External interrupt circuit or extended intelligent I/O service (EI$^2$OS) can be used. | | | |
| Delayed interrupt generation module | An interrupt generation module for switching tasks used in real time operating systems. | | | |
| Extended I/O serial interface | Clock synchronized transmission (3125 bps to 1 Mbps)<br>LSB first/MSB first | | | |
| I$^2$C interface | Serial I/O port for supporting Inter IC BUS | | | |
| Timebase timer | 18-bit counter<br>Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms<br>(at oscillation of 4 MHz) | | | |
| 8-bit D/A converter | 8-bit resolution<br>Number of channels: 2 channels<br>Based on the R-2R system | | | |
| Watchdog timer | Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms<br>(at oscillation of 4 MHz, minimum value) | | | |
| Low-power consumption (standby) mode | Sleep/stop/CPU intermittent operation/clock timer/hardware standby | | | |
| Process | CMOS | | | |
| Power supply voltage for operation* | 4.5 V to 5.5 V | | | |

* : Varies with conditions such as the operating frequency. (See section “■ ELECTRICAL CHARACTERISTICS.”)
Assurance for the MB90V570/A is given only for operation with a tool at a power voltage of 4.5 V to 5.5 V, an operating temperature of 0 °C to +25 °C, and an operating frequency of 1 MHz to 16 MHz.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB90573 | MB90574 | MB90F574/A | MB90574C |
|---|---|---|---|---|
| FPT-120P-M05 | ○ | ○ | ○ | × |
| FPT-120P-M13 | ○ | ○ | ○ | ○ |
| FPT-120P-M21 | × | × | ○ | ○ |

○ : Available ×: Not available

Note : For more information about each package, see section “■ PACKAGE DIMENSIONS.”

## ■ DIFFERENCES AMONG PRODUCTS

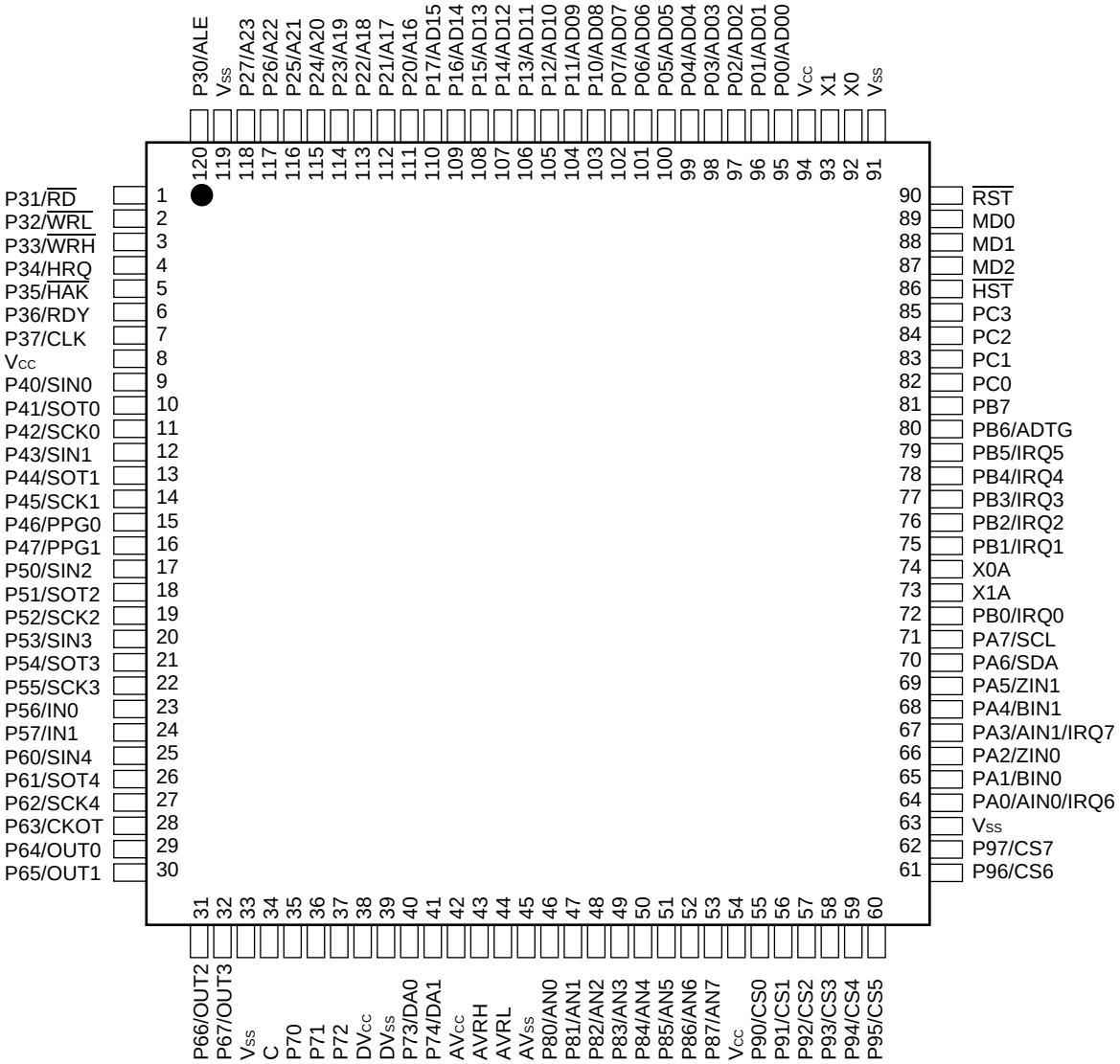
### Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V570/A does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V570/A, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FE0000_H$ to $FF3FFF_H$ to mapped to bank FE and FF only. (This setting can be changed by configuring the development tool.)
- In the MB90F574/574/573/F574A/574C, images from $FF4000_H$ to $FFFFFF_H$ are mapped to bank 00, and $FF0000_H$ to $FF3FFF_H$ to bank FF only.
- The products designated with /A or /C are different from those without /A or /C in that they are DTP/externally-interrupted types which return from standby mode at the ch.0 to ch.1 edge request.

## ■ PIN ASSIGNMENT

(Top view)




(FPT-120P-M05)
(FPT-120P-M13)
(FPT-120P-M21)

## ■ PIN DESCRIPTION

| Pin no. LQFP-120 *1 QFP-120 *2 | Pin name | Circuit type | Function |
|---|---|---|---|
| 92,93 | X0,X1 | A | High speed oscillator pins |
| 74,73 | X0A,X1A | B | Low speed oscillator pins |
| 89 to 87 | MD0 to MD2 | C | These are input pins used to designate the operating mode. They should be connected directly to Vcc or Vss. |
| 90 | $\overline{RST}$ | C | Reset input pin |
| 86 | $\overline{HST}$ | C | Hardware standby input pin |
| 95 to 102 | P00 to P07 | D | In single chip mode, these are general purpose I/O pins. When set for input, they can be set by the pull-up resistance setting register (RDR0). When set for output, this setting will be invalid. |
| | AD00 toAD07 | | In external bus mode, these pins function as address low output/data low I/O pins. |
| 103 to 110 | P10 to P17 | D | In single chip mode, these are general purpose I/O pins. When set for input, they can be set by the pull-up resistance setting register (RDR1). When set for output, the setting will be invalid. |
| | AD08 toAD15 | | In external bus mode, these pins function as address middle output/ data high I/O pins. |
| 111 to 118 | P20 to P27 | E | In single chip mode this is a general-purpose I/O port. |
| | A16 to A23 | | In external bus mode, these pins function as address high output pins. |
| 120 | P30 | E | In single chip mode this is a general-purpose I/O port. |
| | ALE | | In external bus mode, this pin functions as the address latch enable signal output pin. |
| 1 | P31 | E | In single chip mode this is a general-purpose I/O port. |
| | $\overline{RD}$ | | In external bus mode, this pin functions as the read strobe signal output pin. |
| 2 | P32 | E | In single chip mode this is a general-purpose I/O port. |
| | $\overline{WRL}$ | | In external bus mode, this pin functions as the data bus lower 8-bit write strobe signal output pin. |
| 3 | P33 | E | In single chip mode this is a general-purpose I/O port. |
| | $\overline{WRH}$ | | In external bus mode, this pin functions as the data bus upper 8-bit write strobe signal output pin. |
| 4 | P34 | E | In single chip mode this is a general-purpose I/O port. |
| | HRQ | | In external bus mode, this pin functions as the hold request signal input pin. |
| 5 | P35 | E | In single chip mode this is a general-purpose I/O port. |
| | $\overline{HAK}$ | | In external bus mode, this pin functions as the hold acknowledge signal output pin. |
| 6 | P36 | E | In single chip mode this is a general-purpose I/O port. |
| | RDY | | In external bus mode, this pin functions as the ready signal input pin. |

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*1 : FPT-120P-M05

*2 : FPT-120P-M13, FPT-120P-M21

| Pin no. LQFP-120 *1 QFP-120 *2 | Pin name | Circuit type | Function |
|---|---|---|---|
| 7 | P37 | E | In single chip mode this is a general-purpose I/O port. |
| | CLK | | In external bus mode, this pin functions as the clock (CLK) signal output pin. |
| 9 | P40 | F | In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register. |
| | SIN0 | | This is also the UART ch.0 serial data input pin. While UART ch.0 is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed. If shared by output from other functions, this pin should be output disabled during SIN operation. |
| 10 | P41 | F | In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register. |
| | SOT0 | | This is also the UART ch.0 serial data output pin. This function is valid when UART ch.0 is enabled for data output. |
| 11 | P42 | F | In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register. |
| | SCK0 | | This is also the UART ch.0 serial clock I/O pin. This function is valid when UART ch.0 is enabled for clock output. |
| 12 | P43 | F | In single chip mode this is a general-purpose I/O port. It can be set to open-drain by the ODR4 register. |
| | SIN1 | | This is also the UART ch.1 serial data input pin. While UART ch.1 is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed. If shared by output from other functions, this pin should be output disabled during SIN operation. |
| 13 | P44 | F | In single chip mode this is a general-purpose I/O port. It can be set to opendrain by the ODR4 register. |
| | SOT1 | | This is also the UART ch.1 serial data output pin. This function is valid when UART ch.1 is enabled for data output. |
| 14 | P45 | F | In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register. |
| | SCK1 | | This is also the UART ch.1 serial clock I/O pin. This function is valid when UART ch.1 is enabled for clock output. |
| 15,16 | P46,P47 | F | In single chip mode this is a general-purpose I/O port. It can be set to open drain by the ODR4 register. |
| | PPG0,PPG1 | | These are also the PPG0, 1 output pins. This function is valid when PPG0, 1 output is enabled. |
| 17 | P50 | E | In single chip mode this is a general-purpose I/O port. |
| | SIN2 | | This is also the I/O serial ch.0 data input pin. During serial data input, this input signal is in continuous use, and therefore the output function should only be used when needed. |

*(Continued)*

*1 : FPT-120P-M05

*2 : FPT-120P-M13, FPT-120P-M21

| Pin no. LQFP-120 *1 QFP-120 *2 | Pin name | Circuit type | Function |
|---|---|---|---|
| 18 | P51 | E | In single chip mode this is a general-purpose I/O port. |
| | SOT2 | | This is also the I/O serial ch.0 data output pin. This function is valid when serial ch.0 is enabled for serial data output. |
| 19 | P52 | E | In single chip mode this is a general-purpose I/O port. |
| | SCK2 | | This is also the I/O serial ch.0 clock I/O pin. This function is valid when serial ch.0 is enabled for serial data output. |
| 20 | P53 | E | In single chip mode this is a general-purpose I/O port. |
| | SIN3 | | This is also the I/O serial ch.1 data input pin. During serial data input, this input signal is in continuous use, and therefore the output function should only be used when needed. |
| 21 | P54 | E | In single chip mode this is a general-purpose I/O port. |
| | SOT3 | | This is also the I/O serial ch.1 data output pin. This function is valid when serial ch.1 is enabled for serial data output. |
| 22 | P55 | E | In single chip mode this is a general-purpose I/O port. |
| | SCK3 | | This is also the I/O serial ch.1 clock I/O pin. This function is valid when serial ch.1 is enabled for serial data output. |
| 23,24 | P56,P57 | E | In single chip mode this is a general-purpose I/O port. |
| | IN0,IN1 | | These are also the input capture ch.0/1 trigger input pins. During input capture signal input on ch.0/1 this function is in continuous use, and therefore the output function should only be used when needed. |
| 25 | P60 | F | In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid. |
| | SIN4 | | This is also the I/O serial ch.2 data input pin. During serial data input this function is in continuous use, and therefore the output function should only be used when needed. |
| 26 | P61 | F | In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid. |
| | SOT4 | | This is also the I/O serial ch.2 data output pin. This function is valid when serial ch.2 is enabled for serial data output. |
| 27 | P62 | F | In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid. |
| | SCK4 | | This is also the I/O serial ch.2 serial clock I/O pin. This function is valid when serial ch.2 is enabled for serial data output. |
| 28 | P63 | F | In single chip mode this is a general-purpose I/O port. When set for input it can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid. |
| | CKOT | | This is also the clock monitor output pin. This function is valid when clock monitor output is enabled. |

*(Continued)*

*1 : FPT-120P-M05

*2 : FPT-120P-M13, FPT-120P-M21

| Pin no. LQFP-120 *1 QFP-120 *2 | Pin name | Circuit type | Function |
|---|---|---|---|
| 29 to 32 | P64 to P67 | F | In single chip mode these are general-purpose I/O ports. When set for input they can be set by the pull-up resistance register (RDR6). When set for output this setting will be invalid. |
| | OUT0 to OUT3 | | These are also the output compare ch.0 to ch.3 event output pins. This function is valid when the respective channel(s) are enabled for output. |
| 35 to 37 | P70 to P72 | E | These are general purpose I/O ports. |
| 40,41 | P73,P74 | I | These are general purpose I/O ports. |
| | DA0,DA1 | | These are also the D/A converter ch.0,1 analog signal output pins. |
| 46 to 53 | P80 to P87 | K | These are general purpose I/O ports. |
| | AN0 to AN7 | | These are also A/D converter analog input pins. This function is valid when analog input is enabled. |
| 55 to 62 | P90 to P97 | E | These are general purpose I/O ports. |
| | CS0 to CS7 | | These are also chip select signal output pins. This function is valid when chip select signal output is enabled. |
| 34 | C | G | This is the power supply stabilization capacitor pin. It should be connected externally to an 0.1 µF ceramic capacitor. Note that this is not required on the FLASH model (MB90F574/A) and MB90574C. |
| 64 | PA0 | E | This is a general purpose I/O port. |
| | AIN0 | | This pin is also used as count clock A input for 8/16-bit up-down counter ch.0. |
| | IRQ6 | | This pin can also be used as interrupt request input ch. 6. |
| 65 | PA1 | E | This is a general purpose I/O port. |
| | BIN0 | | This pin is also used as count clock B input for 8/16-bit up-down counter ch.0. |
| 66 | PA2 | E | This is a general purpose I/O port. |
| | ZIN0 | | This pin is also used as count clock Z input for 8/16-bit up-down counter ch.0. |
| 67 | PA3 | E | This is a general purpose I/O port. |
| | AIN1 | | This pin is also used as count clock A input for 8/16-bit up-down counter ch.1. |
| | IRQ7 | | This pin can also be used as interrupt request input ch.7. |
| 68 | PA4 | E | This is a general purpose I/O port. |
| | BIN1 | | This pin is also used as count clock B input for 8/16-bit up-down counter ch.1. |
| 69 | PA5 | E | This is a general purpose I/O port. |
| | ZIN1 | | This pin is also used as count clock Z input for 8/16-bit up-down counter ch.1. |

*(Continued)*

*1 : FPT-120P-M05

*2 : FPT-120P-M13, FPT-120P-M21

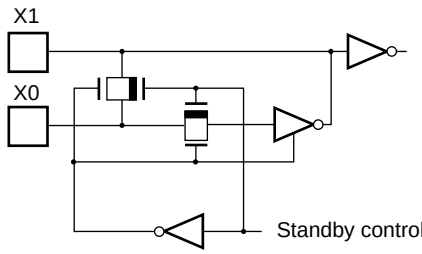
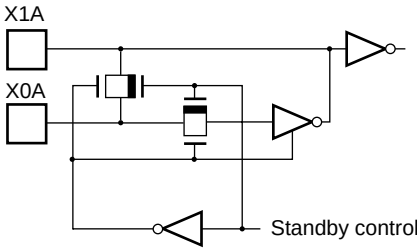
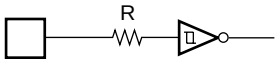
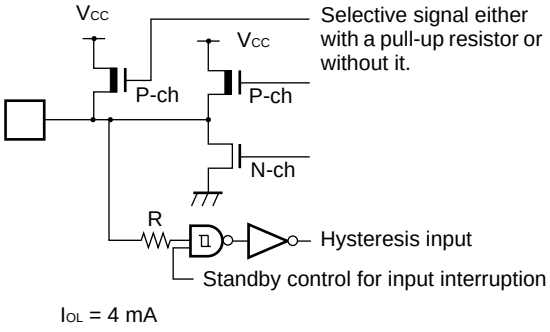
*(Continued)*

| Pin no. LQFP-120 *1 QFP-120 *2 | Pin name | Circuit type | Function |
|---|---|---|---|
| 70 | PA6 | L | This is a general purpose I/O port. |
| | SDA | | This pin is also used as the data I/O pin for the I²C interface. This function is valid when the I²C interface is enabled for operation. While the I²C interface is operating, this port should be set to the input level (DDRA: bit6 = 0). |
| 71 | PA7 | L | This is a general purpose I/O port. |
| | SCL | | This pin is also used as the clock I/O pin for the I²C interface. This function is valid when the I²C interface is enabled for operation. While the I²C interface is operating, this port should be set to the input level (DDRA: bit7 = 0). |
| 72, 75 to 79 | PB0, PB1 to PB5 | E | These are general-purpose I/O ports. |
| | IRQ0, IRQ1 to IRQ5 | | These pins are also the external interrupt input pins. IRQ0, 1 are enabled for both rising and falling edge detection, and therefore cannot be used for recovery from STOP status for MB90V570, MB90F574, MB90573 and MB90574. However, IRQ0, 1 can be used for recovery from STOP status for MB90V570A, MB90F574A and MB90574C. |
| 80 | PB6 | E | This is a general purpose I/O port. |
| | ADTG | | This is also the A/D converter external trigger input pin. While the A/D converter is in input operation, this input signal is in continuous use, and therefore the output function should only be used when needed. |
| 81 | PB7 | E | This is a general purpose I/O port. |
| 82 to 85 | PC0 to PC3 | E | These are general purpose I/O ports. |
| 8,54,94 | $V_{CC}$ | Power supply | These are power supply (5V) input pins. |
| 33,63, 91,119 | $V_{SS}$ | Power supply | These are power supply (0V) input pins. |
| 42 | $AV_{CC}$ | H | This is the analog macro (D/A, A/D etc.) Vcc power supply input pin. |
| 43 | AVRH | J | This is the A/D converter Vref+ input pin. The input voltage should not exceed Vcc. |
| 44 | AVRL | H | This is the A/D converter Vref- input pin. The input voltage should not less than Vss. |
| 45 | $AV_{SS}$ | H | This is the analog macro (D/A, A/D etc.) Vss power supply input pin. |
| 38 | $DV_{CC}$ | H | This is the D/A converter Vref input pin. The input voltage should not exceed Vcc. |
| 39 | $DV_{SS}$ | H | This is the D/A converter GND power supply pin. It should be set to Vss equivalent potential. |

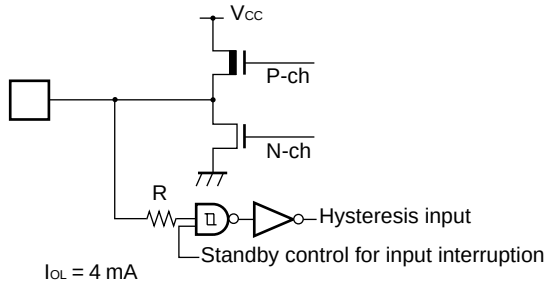
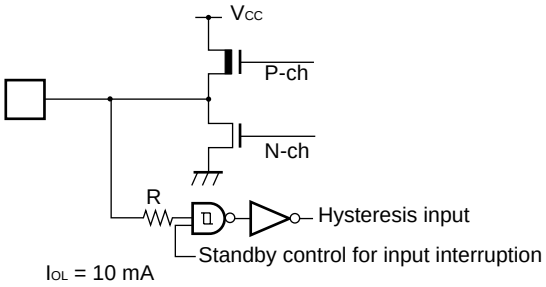
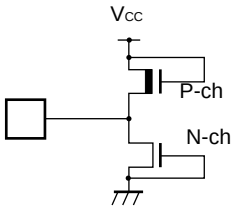
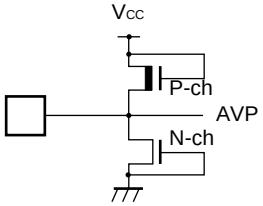
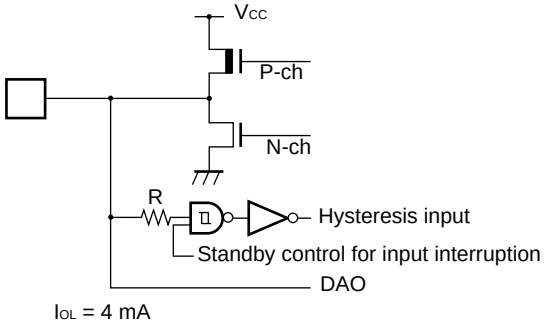
*1 : FPT-120P-M05

*2 : FPT-120P-M13, FPT-120P-M21

## ■ I/O CIRCUIT TYPE

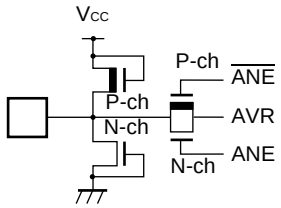
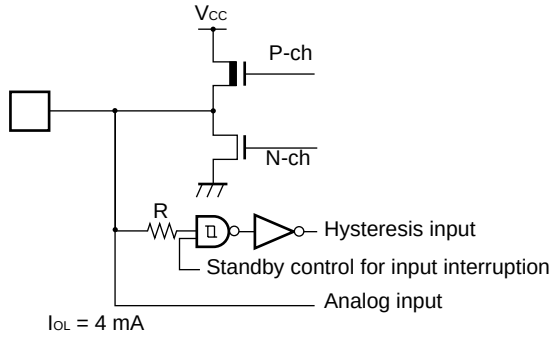
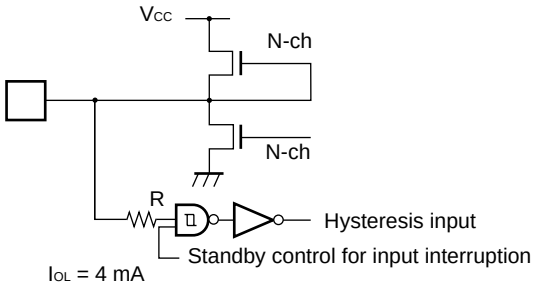
| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Oscillator circuit<br>Oscillator recovery resistance for high speed = approx. 1 MΩ |
| B |  | • Oscillator circuit<br>Oscillator recovery resistance for low speed = approx. 10 MΩ |
| C |  | • Hysteresis input pin<br>Resistance value = approx. 50 kΩ (typ.) |
| D |  | • CMOS hysteresis input pin with input pull-up control<br>• CMOS level output.<br>• CMOS hysteresis input<br>(Includes input shut down standby control function)<br>• Pull-up resistance value = approx. 50 kΩ(typ.)<br>$I_{OL}$ = 4mA |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| E |  | • CMOS hysteresis input/output pin.<br>• CMOS level output<br>• CMOS hysteresis input (Includes input shut down standby control function)<br>$I_{OL}$ = 4 mA |
| F |  | • CMOS hysteresis input/output pin.<br>• CMOS level output<br>• CMOS hysteresis input (Includes input shut down standby control function)<br>$I_{OL}$ = 10 mA (Large current port) |
| G |  | • C pin output (capacitance connector pin).<br><br>On the MB90F574 this pin is not connected (NC). |
| H |  | • Analog power supply protector circuit. |
| I |  | • CMOS hysteresis input/output<br>• Analog output/CMOS output dual-function pin (CMOS output is not available during analog output.) (Analog output priority: DAE = 1)<br>• Includes input shut down standby control function.<br>$I_{OL}$ = 4mA |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| J |  | • A/D converter ref+ power supply input pin(AVRH), with power supply protector circuit. |
| K |  | • CMOS hysteresis input /analog input dual-function pin.<br>• CMOS output<br>• Includes input shut down function at input shut down standby. |
| L |  | • Hysteresis input<br>• N-ch open-drain output<br>• Includes input shut down standby control function.<br>$I_{OL}$= 4mA |

## ■ HANDLING DEVICES

### 1. Preventing Latchup

CMOS ICs may cause latchup in the following situations:

- When a voltage higher than Vcc or lower than Vss is applied to input or output pins.
- When a voltage exceeding the rating is applied between Vcc and Vss.
- When AVcc power is supplied prior to the Vcc voltage.

In turning on/turning off the analog power supply, make sure the analog power voltage ($AV_{CC}$, AVRH, $DV_{CC}$)and analog input voltages not exceed the digital voltage ($V_{CC}$).

### 2. Treatment of unused pins



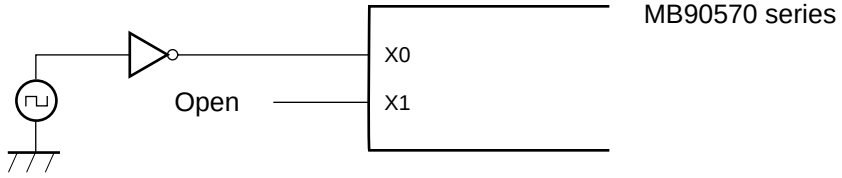
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefor they must be tied to $V_{CC}$ or Ground through resistors. In this case those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

**• Using external clock**




### 4. Unused Sub Clock Mode

If sub clock modes are not used, the oscillator should be connected to the X01A pin and X1A pin

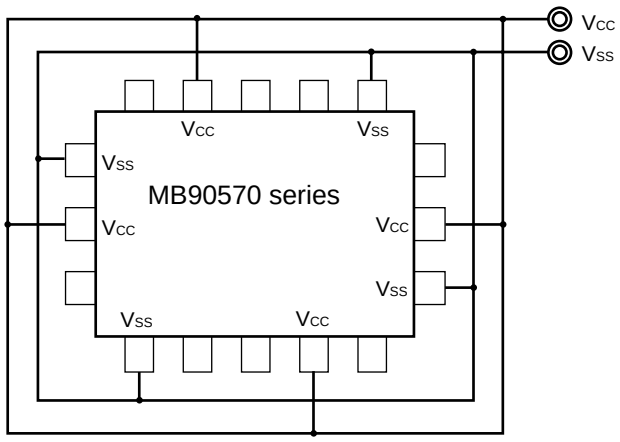
### 5. Power Supply Pins ($V_{CC}$/$V_{SS}$)

In products with multiple $V_{CC}$ or $V_{SS}$ pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect $V_{CC}$ and $V_{SS}$ pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 µF between $V_{CC}$ and $V_{SS}$ pin near the device.

- **Using power supply pins**






## 6. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

## 7. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply ($AV_{CC}$, AVRH, AVRL, $DV_{CC}$,$DV_{SS}$) and analog inputs (AN0 to AN7) after turning-on the digital power supply ($V_{CC}$).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 8. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

## 9. N.C. Pins

The N.C. (internally connected) pins must be opened for use.

## 10. Notes on Energization

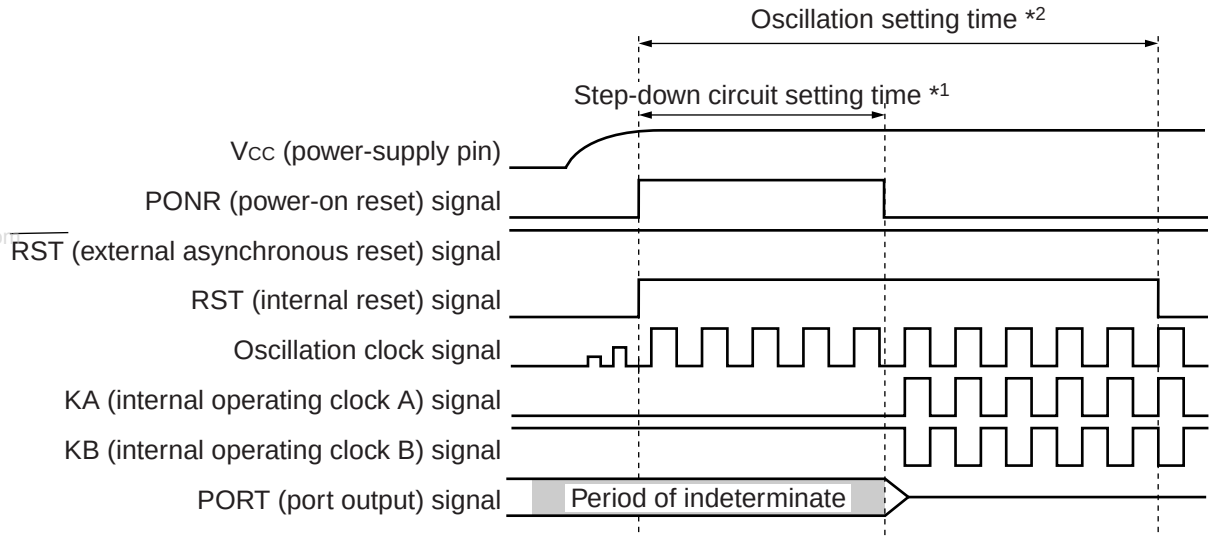
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more µs (0.2 V to 2.7 V).

## 11. Indeterminate outputs from ports 0 and 1

The outputs from ports 0 and 1 become indeterminate during oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on. (MB90573, MB90574, MB90V570, MB90V570A)

The series without built-in step-down circuit have no oscillation setting time of step-down circuit, so outputs should not become indeterminate. (MB90F574,MB90F574A,MB90574C)

Timing chart of indeterminate outputs from ports 0 and 1




*1: Step-down circuit setting time $2^{17}$/oscillation clock frequency (oscillation clock frequency of 16 MHz: 8.19 ms)

*2: Oscillation setting time $2^{18}$/oscillation clock frequency (oscillation clock frequency of 16 MHz: 16.38 ms)

## 12. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. Turn on the power again to initialize these registers.

## 13. Return from standby state

If the power-supply voltage goes below the standby RAM holding voltage in the standby state, the device may fail to return from the standby state. In this case, reset the device via the external reset pin to return to the normal state.

## 14. Precautions for Use of 'DIV A, Ri,' and 'DIVW A, Ri' Instructions

The signed multiplication-division instructions 'DIV A, Ri,' and 'DIVW A, RWi' should be used when the corresponding bank registers (DTB, ADB, USB, SSB) are set to value '00h.' If the corresponding bank registers (DTB, ADB, USB, SSB) are set to a value other than '00h,' then the remainder obtained after the execution of the instruction will not be placed in the instruction operand register.

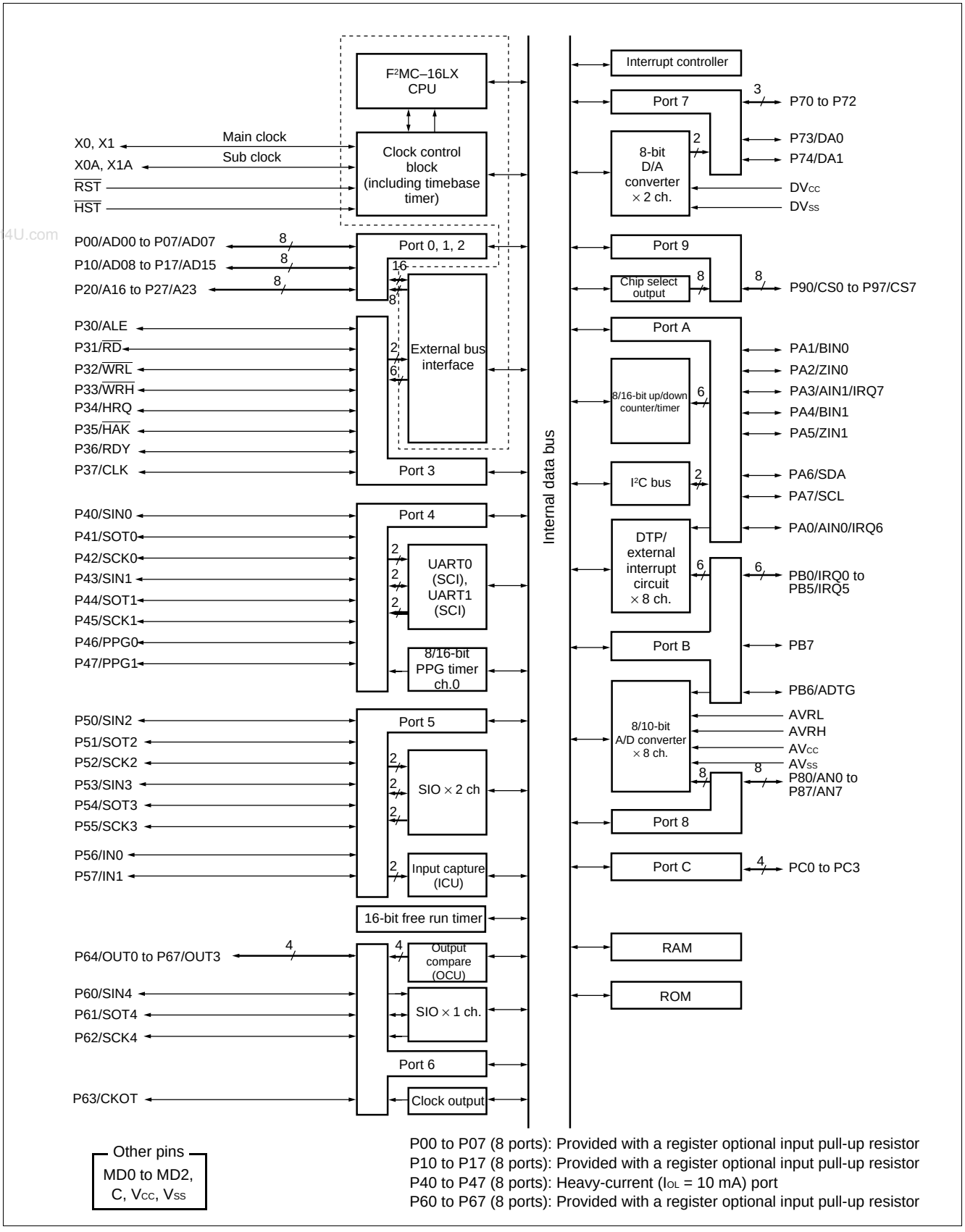
## 15. Precautions for Use of REALOS

Extended intelligent I/O service ($EI^2OS$) cannot be used, when REALOS is used.

## 16. Caution on PLL Clock Mode

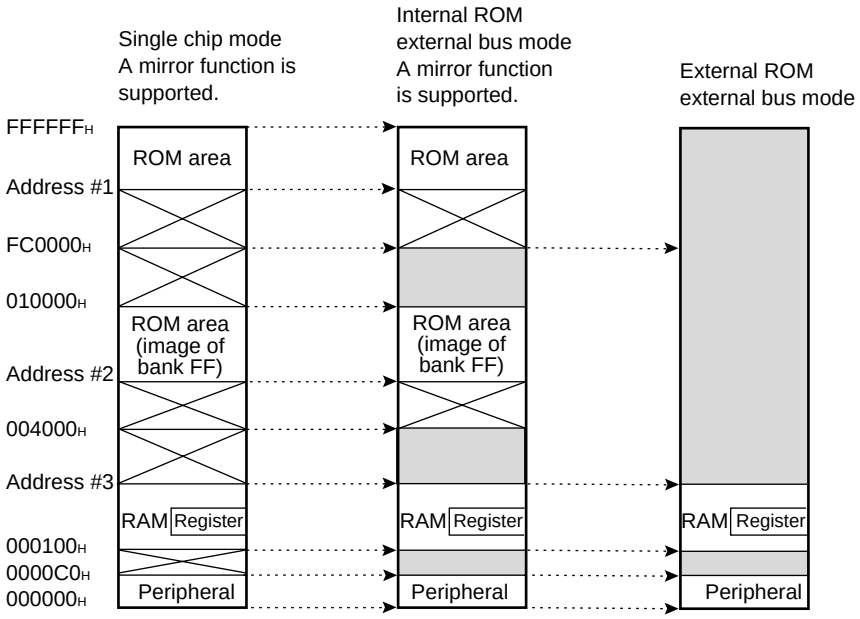
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## ■ BLOCK DIAGRAM




P00 to P07 (8 ports): Provided with a register optional input pull-up resistor
P10 to P17 (8 ports): Provided with a register optional input pull-up resistor
P40 to P47 (8 ports): Heavy-current ($I_{OL}$ = 10 mA) port
P60 to P67 (8 ports): Provided with a register optional input pull-up resistor

## ■ MEMORY MAP




| Part number | Address #1* | Address #2* | Address #3* |
|---|---|---|---|
| MB90573 | FE0000H | 004000H | 001800H |
| MB90574/C | FC0000H | 004000H | 002900H |
| MB90F574/A | FC0000H | 004000H | 002900H |

: Internal access memory
: External access memory
: Inhibited area

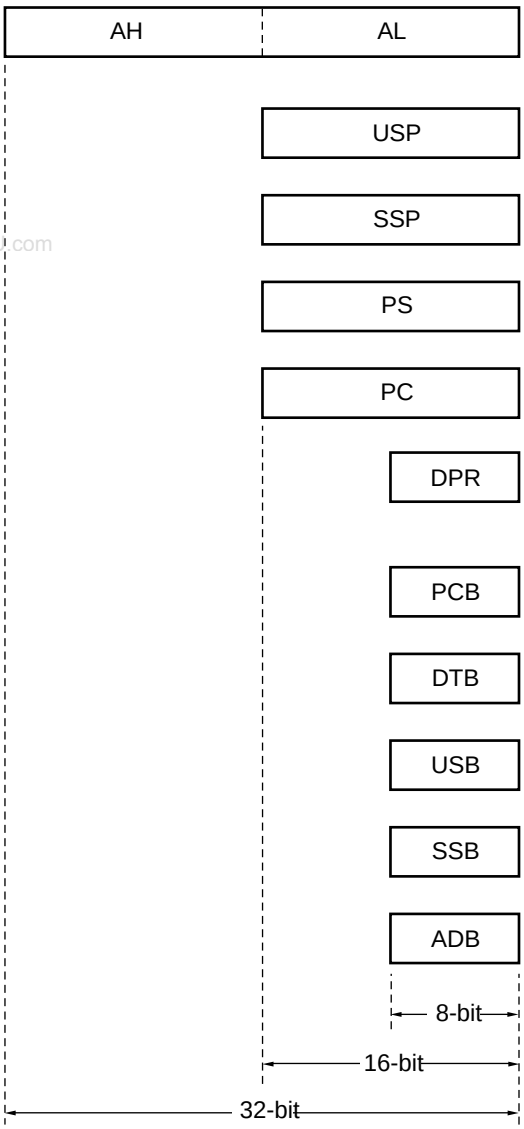
*: Addresses #1, #2 and #3 are unique to the product type.

Note : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 is assigned to the same address, enabling reference of the table on the ROM without stating “far”.

For example, if an attempt has been made to access 00C000H, the contents of the ROM at FFC000H are accessed actually. Since the ROM area of the FF bank exceeds 48 kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 00400H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

## ■ F²MC-16LX CPU PROGRAMMING MODEL

- **Dedicated registers**




:**Accumulator (A)**
Dual 16-bit register used for storing results of calculation etc. The two 16-bit registers can be combined to be used as a 32-bit register.

:**User stack pointer (USP)**
The 16-bit pointer indicating a user stack address.

:**System stack pointer (SSP)**
The 16-bit pointer indicating the status of the system stack address.

:**Processor status (PS)**
The 16-bit register indicating the system status.

:**Program counter (PC)**
The 16-bit register indicating storing location of the current instruction code.

:**Direct page register (DPR)**
The 8-bit register indicating bit 8 through 15 of the operand address in the short direct addressing mode.

:**Program bank register (PCB)**
The 8-bit register indicating the program space.

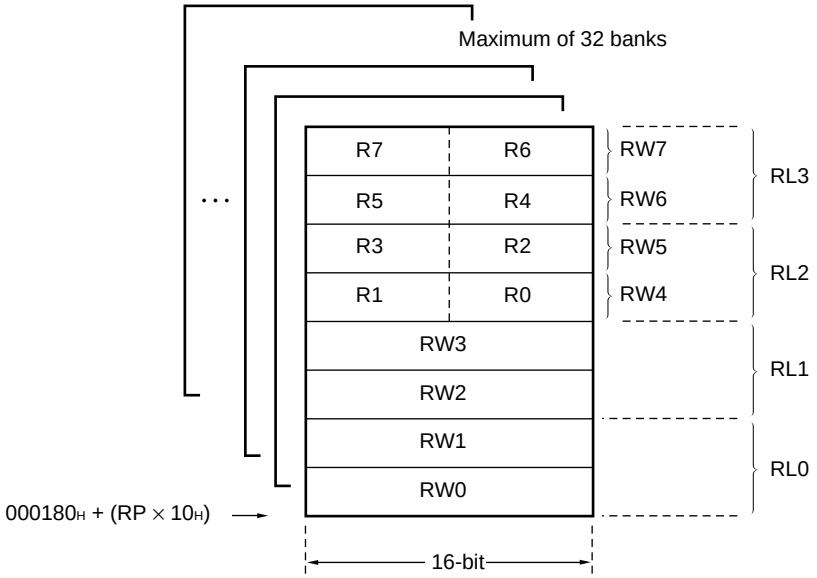
:**Data bank register (DTB)**
The 8-bit register indicating the data space.

:**User stack bank register (USB)**
The 8-bit register indicating the user stack space.

:**System stack bank register (SSB)**
The 8-bit register indicating the system stack space.

:**Additional data bank register (ADB)**
The 8-bit register indicating the additional data space.

- **General-purpose registers**






- **Processor status (PS)**

| | ILM | | | RP | | | | | CCR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| PS | ILM2 | ILM1 | ILM0 | B4 | B3 | B2 | B1 | B0 | — | I | S | T | N | Z | V | C |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | 0 | 1 | X | X | X | X | X |

—: Reserved
X: Undefined

## ■ I/O MAP

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000000H | PDR0 | Port 0 data register | R/W | Port 0 | XXXXXXXXB |
| 000001H | PDR1 | Port 1 data register | R/W | Port 1 | XXXXXXXXB |
| 000002H | PDR2 | Port 2 data register | R/W | Port 2 | XXXXXXXXB |
| 000003H | PDR3 | Port 3 data register | R/W | Port 3 | XXXXXXXXB |
| 000004H | PDR4 | Port 4 data register | R/W | Port 4 | XXXXXXXXB |
| 000005H | PDR5 | Port 5 data register | R/W | Port 5 | XXXXXXXXB |
| 000006H | PDR6 | Port 6 data register | R/W | Port 6 | XXXXXXXXB |
| 000007H | PDR7 | Port 7 data register | R/W | Port 7 | XXXXXXXXB |
| 000008H | PDR8 | Port 8 data register | R/W | Port 8 | XXXXXXXXB |
| 000009H | PDR9 | Port 9 data register | R/W | Port 9 | XXXXXXXXB |
| 00000AH | PDRA | Port A data register | R/W | Port A | XXXXXXXXB |
| 00000BH | PDRB | Port B data register | R/W | Port B | XXXXXXXXB |
| 00000CH | PDRC | Port C data register | R/W | Port C | XXXXXXXXB |
| 00000DH to 00000FH | (Disabled) | | | | |
| 000010H | DDR0 | Port 0 direction register | R/W | Port 0 | 00000000B |
| 000011H | DDR1 | Port 1 direction register | R/W | Port 1 | 00000000B |
| 000012H | DDR2 | Port 2 direction register | R/W | Port 2 | 00000000B |
| 000013H | DDR3 | Port 3 direction register | R/W | Port 3 | 00000000B |
| 000014H | DDR4 | Port 4 direction register | R/W | Port 4 | 00000000B |
| 000015H | DDR5 | Port 5 direction register | R/W | Port 5 | 00000000B |
| 000016H | DDR6 | Port 6 direction register | R/W | Port 6 | 00000000B |
| 000017H | DDR7 | Port 7 direction register | R/W | Port 7 | ---00000B |
| 000018H | DDR8 | Port 8 direction register | R/W | Port 8 | 00000000B |
| 000019H | DDR9 | Port 9 direction register | R/W | Port 9 | 00000000B |
| 00001AH | DDRA | Port A direction register | R/W | Port A | 00000000B |
| 00001BH | DDRB | Port B direction register | R/W | Port B | 00000000B |
| 00001CH | DDRC | Port C direction register | R/W | Port C | 00000000B |
| 00001DH | ODR4 | Port 4 output pin register | R/W | Port 4 | 00000000B |
| 00001EH | ADER | Analog input enable register | R/W | Port 8, 8/10-bit A/D converter | 11111111B |
| 00001FH | (Disabled) | | | | |
| 000020H | SMR0 | Serial mode register 0 | R/W | UART0 (SCI) | 00000000B |
| 000021H | SCR0 | Serial control register 0 | R/W | | 00000100B |

*(Continued)*

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000022H | SIDR0/ SODR0 | Serial input data register 0/ serial output data register 0 | R/W | UART0 (SCI) | XXXXXXXXB |
| 000023H | SSR0 | Serial status register 0 | R/W | | 00001–00B |
| 000024H | SMR1 | Serial mode register 1 | R/W | UART1 (SCI) | 00000000B |
| 000025H | SCR1 | Serial control register 1 | R/W | | 00000100B |
| 000026H | SIDR1/ SODR1 | Serial input data register 1/ serial output data register 1 | R/W | | XXXXXXXXB |
| 000027H | SSR1 | Serial status register 1 | R/W | | 00001–00B |
| 000028H | CDCR0 | Communications prescaler control register 0 | R/W | Communica-tions prescaler register 0 | 0–––1111B |
| 000029H | (Disabled) | | | | |
| 00002AH | CDCR1 | Communications prescaler control register 1 | R/W | Communica-tions prescaler register 0 | 0–––1111B |
| 00002BH to 00002FH | (Disabled) | | | | |
| 000030H | ENIR | DTP/interrupt enable register | R/W | DTP/external interrupt circuit | 00000000B |
| 000031H | EIRR | DTP/interrupt factor register | R/W | | XXXXXXXXB |
| 000032H | ELVR | Request level setting register | R/W | | 00000000B |
| 000033H | | | | | 00000000B |
| 000034H | (Disabled) | | | | |
| 000035H | | | | | |
| 000036H | ADCS1 | A/D control status register lower digits | R/W | 8/10-bit A/D converter | 00000000B |
| 000037H | ADCS2 | A/D control status register upper digits | R/W or W | | 00000000B |
| 000038H | ADCR1 | A/D data register lower digits | R | | XXXXXXXXB |
| 000039H | ADCR2 | A/D data register upper digits | W | | 0001–XXB |
| 00003AH | DADR0 | D/A converter data register ch.0 | R/W | 8-bit D/A converter | XXXXXXXXB |
| 00003BH | DADR1 | D/A converter data register ch.1 | R/W | | XXXXXXXXB |
| 00003CH | DACR0 | D/A control register 0 | R/W | | –––––––0B |
| 00003DH | DACR1 | D/A control register 1 | R/W | | –––––––0B |
| 00003EH | CLKR | Clock output enable register | R/W | Clock monitor function | ––––0000B |
| 00003FH | (Disabled) | | | | |
| 000040H | PRLL0 | PPG0 reload register L ch.0 | R/W | 8/16-bit PPG timer 0 | XXXXXXXXB |
| 000041H | PRLH0 | PPG0 reload register H ch.0 | R/W | | XXXXXXXXB |

*(Continued)*

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000042H | PRLL1 | PPG1 reload register L ch.1 | R/W | 8/16-bit PPG timer 1 | XXXXXXXXB |
| 000043H | PRLH1 | PPG1 reload register H ch.1 | R/W | | XXXXXXXXB |
| 000044H | PPGC0 | PPG0 operating mode control register ch.0 | R/W | 8/16-bit PPG timer 0 | 0X000XX1B |
| 000045H | PPGC1 | PPG1 operating mode control register ch.1 | R/W | 8/16-bit PPG timer 1 | 0X000001B |
| 000046H | PPGOE | PPG0 and 1 output control registers ch.0 and ch.1 | R/W | 8/16-bit PPG timer 0, 1 | 000000XXB |
| 000047H | (Disabled) | | | | |
| 000048H | SMCSL0 | Serial mode control lower status register 0 | R/W | Extended I/O serial interface 0 | ----0000B |
| 000049H | SMCSH0 | Serial mode control upper status register 0 | R/W | | 00000010B |
| 00004AH | SDR0 | Serial data register 0 | R/W | | XXXXXXXXB |
| 00004BH | (Disabled) | | | | |
| 00004CH | SMCSL1 | Serial mode control lower status register 1 | R/W | Extended I/O serial interface 1 | ----0000B |
| 00004DH | SMCSH1 | Serial mode control upper status register 1 | R/W | | 00000010B |
| 00004EH | SDR1 | Serial data register 1 | R/W | | XXXXXXXXB |
| 00004FH | (Disabled) | | | | |
| 000050H | IPCP0 | ICU data register ch.0 | R | 16-bit I/O timer (input capture (ICU) section) | XXXXXXXXB |
| 000051H | | | | | XXXXXXXXB |
| 000052H | IPCP1 | ICU data register ch.1 | R | | XXXXXXXXB |
| 000053H | | | | | XXXXXXXXB |
| 000054H | ICS01 | ICU control status register | R/W | | 00000000B |
| 000055H | (Disabled) | | | | |
| 000056H | TCDT | Free run timer data register | R/W | 16-bit I/O timer (16-bit free run timer section) | 00000000B |
| 000057H | | | | | 00000000B |
| 000058H | TCCS | Free run timer control status register | R/W | | 00000000B |
| 000059H | (Disabled) | | | | |
| 00005AH | OCCP0 | OCU compare register ch.0 | R/W | 16-bit I/O timer (output compare (OCU) section) | XXXXXXXXB |
| 00005BH | | | | | XXXXXXXXB |
| 00005CH | OCCP1 | OCU compare register ch.1 | R/W | | XXXXXXXXB |
| 00005DH | | | | | XXXXXXXXB |
| 00005EH | OCCP2 | OCU compare register ch.2 | R/W | | XXXXXXXXB |
| 00005FH | | | | | XXXXXXXXB |

*(Continued)*

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000060H | OCCP3 | OCU compare register ch.3 | R/W | 16-bit I/O timer (output compare (OCU) section) | XXXXXXXXB |
| 000061H | | | | | XXXXXXXXB |
| 000062H | OCS0 | OCU control status register ch.0 | R/W | | 0000––00B |
| 000063H | OCS1 | OCU control status register ch.1 | R/W | | –––00000B |
| 000064H | OCS2 | OCU control status register ch.2 | R/W | | 0000––00B |
| 000065H | OCS3 | OCU control status register ch.3 | R/W | | –––00000B |
| 000066H | (Disabled) | | | | |
| 000067H | | | | | |
| 000068H | IBSR | I²C bus status register | R | I²C interface | 00000000B |
| 000069H | IBCR | I²C bus control register | R/W | | 00000000B |
| 00006AH | ICCR | I²C bus clock control register | R/W | | ––0XXXXXB |
| 00006BH | IADR | I²C bus address register | R/W | | –XXXXXXXB |
| 00006CH | IDAR | I²C bus data register | R/W | | XXXXXXXXB |
| 00006DH | (Disabled) | | | | |
| 00006EH | | | | | |
| 00006FH | ROMM | ROM mirroring function selection register | W | ROM mirroring function selection module | –––––––1B |
| 000070H | UDCR0 | Up/down count register 0 | R | 8/16-bit up/down counter/timer | 00000000B |
| 000071H | UDCR1 | Up/down count register 1 | R | | 00000000B |
| 000072H | RCR0 | Reload compare register 0 | W | | 00000000B |
| 000073H | RCR1 | Reload compare register 1 | W | | 00000000B |
| 000074H | CSR0 | Counter status register 0 | R/W | | 00000000B |
| 000075H | (Reserved area)*3 | | | | |
| 000076H | CCRL0 | Counter control register 0 | R/W | 8/16-bit up/down counter/timer | –0000000B |
| 000077H | CCRH0 | | | | 00000000B |
| 000078H | CSR1 | Counter status register 1 | R/W | | 00000000B |
| 000079H | (Reserved area)*3 | | | | |
| 00007AH | CCRL1 | Counter control register 1 | R/W | 8/16-bit up/down counter/timer | –0000000B |
| 00007BH | CCRH1 | | | | –0000000B |
| 00007CH | SMCSL2 | Serial mode control lower status register 2 | R/W | Extended I/O serial interface 2 | ––––0000B |
| 00007DH | SMCSH2 | Serial mode control higher status register 2 | R/W | | 00000010B |
| 00007EH | SDR2 | Serial data register 2 | R/W | | XXXXXXXXB |
| 00007FH | (Disabled) | | | | |

*(Continued)*

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 000080H | CSCR0 | Chip selection control register 0 | R/W | Chip select output | – – – – 0 0 0 0B |
| 000081H | CSCR1 | Chip selection control register 1 | R/W | | – – – – 0 0 0 0B |
| 000082H | CSCR2 | Chip selection control register 2 | R/W | | – – – – 0 0 0 0B |
| 000083H | CSCR3 | Chip selection control register 3 | R/W | | – – – – 0 0 0 0B |
| 000084H | CSCR4 | Chip selection control register 4 | R/W | | – – – – 0 0 0 0B |
| 000085H | CSCR5 | Chip selection control register 5 | R/W | | – – – – 0 0 0 0B |
| 000086H | CSCR6 | Chip selection control register 6 | R/W | | – – – – 0 0 0 0B |
| 000087H to 00008BH | (Disabled) | | | | |
| 00008CH | RDR0 | Port 0 input pull-up resistor setup register | R/W | Port 0 | 0 0 0 0 0 0 0 0B |
| 00008DH | RDR1 | Port 1 input pull-up resistor setup register | R/W | Port 1 | 0 0 0 0 0 0 0 0B |
| 00008EH | RDR6 | Port 6 input pull-up resistor setup register | R/W | Port 6 | 0 0 0 0 0 0 0 0B |
| 00008FH to 00009DH | (Disabled) | | | | |
| 00009EH | PACSR | Program address detection control status register | R/W | Address match detection function | 0 0 0 0 0 0 0 0B |
| 00009FH | DIRR | Delayed interrupt factor generation/ cancellation register | R/W | Delayed interrupt generation module | – – – – – – – 0B |
| 0000A0H | LPMCR | Low-power consumption mode control register | R/W | Low-power consumption (standby) mode | 0 0 0 1 1 0 0 0B |
| 0000A1H | CKSCR | Clock select register | R/W | | 1 1 1 1 1 1 0 0B |
| 0000A2H to 0000A4H | (Disabled) | | | | |
| 0000A5H | ARSR | Automatic ready function select register | W | External bus pin | 0 0 1 1 – – 0 0B |
| 0000A6H | HACR | Upper address control register | W | | 0 0 0 0 0 0 0 0B |
| 0000A7H | ECSR | Bus control signal select register | W | | 0 0 0 0 0 0 0 0B |
| 0000A8H | WDTC | Watchdog timer control register | R/W | Watchdog timer | X X X X X X X XB |
| 0000A9H | TBTC | Timebase timer control register | R/W | Timebase timer | 1 – – 0 0 1 0 0B |
| 0000AAH | WTC | Clock timer control register | R/W | Clock timer | 1 X 0 0 0 0 0 0B |

*(Continued)*

*(Continued)*

| Address | Abbreviated register name | Register name | Read/ write | Resource name | Initial value |
|---|---|---|---|---|---|
| 0000AB$_H$ to 0000AD$_H$ | (Disabled) | | | | |
| 0000AE$_H$ | FMCS | Flash control register | R/W | Flash interface | 0 0 0 X 0 X X 0$_B$ |
| 0000AF$_H$ | (Disabled) | | | | |
| 0000B0$_H$ | ICR00 | Interrupt control register 00 | R/W | Interrupt controller | 0 0 0 0 0 1 1 1$_B$ |
| 0000B1$_H$ | ICR01 | Interrupt control register 01 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B2$_H$ | ICR02 | Interrupt control register 02 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B3$_H$ | ICR03 | Interrupt control register 03 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B4$_H$ | ICR04 | Interrupt control register 04 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B5$_H$ | ICR05 | Interrupt control register 05 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B6$_H$ | ICR06 | Interrupt control register 06 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B7$_H$ | ICR07 | Interrupt control register 07 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B8$_H$ | ICR08 | Interrupt control register 08 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B9$_H$ | ICR09 | Interrupt control register 09 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BA$_H$ | ICR10 | Interrupt control register 10 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BB$_H$ | ICR11 | Interrupt control register 11 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BC$_H$ | ICR12 | Interrupt control register 12 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BD$_H$ | ICR13 | Interrupt control register 13 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BE$_H$ | ICR14 | Interrupt control register 14 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BF$_H$ | ICR15 | Interrupt control register 15 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000C0$_H$ to 0000FF$_H$ | (External area)*1 | | | | |
| 000100$_H$ to 000###$_H$ | (RAM area)*2 | | | | |
| 000###$_H$ to 001FEF$_H$ | (Reserved area)*3 | | | | |
| 001FF0$_H$ | PADR0 | Program address detection register 0 | R/W | Address match detection function | X X X X X X X X$_B$ |
| 001FF1$_H$ | | Program address detection register 1 | R/W | | X X X X X X X X$_B$ |
| 001FF2$_H$ | | Program address detection register 2 | R/W | | X X X X X X X X$_B$ |
| 001FF3$_H$ | PADR1 | Program address detection register 3 | R/W | | X X X X X X X X$_B$ |
| 001FF4$_H$ | | Program address detection register 4 | R/W | | X X X X X X X X$_B$ |
| 001FF5$_H$ | | Program address detection register 5 | R/W | | X X X X X X X X$_B$ |
| 001FF6$_H$ to 001FFF$_H$ | (Reserved area) | | | | |

Descriptions for read/write

R/W : Readable and writable
R : Read only
W : Write only

Descriptions for initial value

0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.
– : This bit is unused. The initial value is undefined.



*1 : This area is the only external access area having an address of 0000FF$_H$ or lower. An access operation to this area is handled as that to external I/O area.

*2 : For details of the RAM area, see “■ MEMORY MAP”.

*3 : The reserved area is disabled because it is used in the system.

Notes : • For bits that is initialized by an reset operation, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.
For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.
• The addresses following 0000FF$_H$ are reserved. No external bus access signal is generated.
• Boundary ####$_H$ between the RAM area and the reserved area varies with the product model.

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

| Interrupt source | EI²OS support | Interrupt vector | | Interrupt control register | | Priority |
|---|---|---|---|---|---|---|
| | | Number | Address | ICR | Address | |
| Reset | × | # 08 | FFFFDC$_H$ | — | — | High |
| INT9 instruction | × | # 09 | FFFFD8$_H$ | — | — | |
| Exception | × | # 10 | FFFFD4$_H$ | — | — | |
| 8/10-bit A/D converter | ○ | # 11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ | |
| Input capture 0 (ICU) include | ○ | # 12 | FFFFCC$_H$ | | | |
| DTP0 (external interrupt 0) | ○ | # 13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ | |
| Input capture 1 (ICU) include | ○ | # 14 | FFFFC4$_H$ | | | |
| Output compare 0 (OCU) match | ○ | # 15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ | |
| Output compare 1 (OCU) match | ○ | # 16 | FFFFBC$_H$ | | | |
| Output compare 2 (OCU) match | ○ | # 17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ | |
| Output compare 3 (OCU) match | ○ | # 18 | FFFFB4$_H$ | | | |
| Extended I/O serial interface 0 | ○ | # 19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ | |
| 16-bit free run timer | × | # 20 | FFFFAC$_H$ | | | |
| Extended I/O serial interface 1 | ○ | # 21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ | |
| Clock timer | × | # 22 | FFFFA4$_H$ | | | |
| Extended I/O serial interface 2 | ○ | # 23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ | |
| DTP1 (external interrupt 1) | ○ | # 24 | FFFF9C$_H$ | | | |
| DTP2/DTP3 (external interrupt 2/ external interrupt 3) | ○ | # 25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ | |
| 8/16-bit PPG timer 0 counter borrow | × | # 26 | FFFF94$_H$ | | | |
| DTP4/DTP5 (external interrupt 4/ external interrupt 5) | ○ | # 27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ | |
| 8/16-bit PPG timer 1 counter borrow | × | # 28 | FFFF8C$_H$ | | | |
| 8/16-bit up/down counter/timer 0 borrow/overflow/inversion | ○ | # 29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ | |
| 8/16-bit up/down counter/timer 0 compare match | ○ | # 30 | FFFF84$_H$ | | | |
| 8/16-bit up/down counter/timer 1 borrow/overflow/inversion | ○ | # 31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ | |
| 8/16-bit up/down counter/timer 1 compare match | ○ | # 32 | FFFF7C$_H$ | | 0000BA$_H$ | |
| DTP6 (external interrupt 6) | ○ | # 33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ | |
| Timebase timer | × | # 34 | FFFF74$_H$ | | | Low |

*(Continued)*

*(Continued)*

| Interrupt source | EI²OS support | Interrupt vector | | Interrupt control register | | Priority |
|---|---|---|---|---|---|---|
| | | Number | Address | ICR | Address | |
| DTP7 (external interrupt 7) | ○ | # 35 | FFFF70H | ICR12 | 0000BCH | High |
| I²C interface | × | # 36 | FFFF6CH | | | |
| UART1 (SCI) reception complete | ◎ | # 37 | FFFF68H | ICR13 | 0000BDH | |
| UART1 (SCI) transmission complete | ○ | # 38 | FFFF64H | | | |
| UART0 (SCI) reception complete | ◎ | # 39 | FFFF60H | ICR14 | 0000BEH | |
| UART0 (SCI) transmission complete | ○ | # 40 | FFFF5CH | | | |
| Flash memory | × | # 41 | FFFF58H | ICR15 | 0000BFH | |
| Delayed interrupt generation module | × | # 42 | FFFF54H | | | Low |

○ :Can be used
× :Can not be used
◎ :Can be used. With EI²OS stop function.

## ■ PERIPHERALS

### 1. I/O Port

#### (1) Input/output Port

Port 0 through 4, 6, 8, A and B are general-purpose I/O ports having a combined function as an external bus pin and a resource input. Port 0 to Port 3 have a general-purpose I/O ports function only in the single-chip mode.

- Operation as output port

  The pin is configured as an output port by setting the corresponding bit of the DDR register to “1”.

  Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.



  The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

Note : When a read-modify-write instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output, however, values of bits configured by the DDR register as inputs are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when configuring the bit used as input as outputs.

- Operation as input port

  The pin is configured as an input by setting the corresponding bit of the DDR register to “0”.

  When the pin is configured as an input, the output buffer is turned-off and the pin is put into a high-impedance status.

  When a data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.

  Reading the PDR register reads out the pin level (“0” or “1”).

### (2) Register Configuration

- Port 0 data register (PDR0)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000000H | (PDR1) | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 1 data register (PDR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000001H | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | (PDR0) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |



- Port 2 data register (PDR2)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000002H | (PDR3) | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 3 data register (PDR3)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000003H | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 | (PDR2) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 4 data register (PDR4)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000004H | (PDR5) | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 5 data register (PDR5)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000005H | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 | (PDR4) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 6 data register (PDR6)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000006H | (PDR7) | P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 7 data register (PDR7)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000007H | — | — | — | P74 | P73 | P72 | P71 | P70 | (PDR6) | - - -XXXXXB |
| | — | — | — | R/W | R/W | R/W | R/W | R/W | | |

- Port 8 data register (PDR8)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000008H | (PDR9) | P87 | P86 | P85 | P84 | P83 | P82 | P81 | P80 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

*(Continued)*

- Port 9 data register (PDR9)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000009H | P97 | P96 | P95 | P94 | P93 | P92 | P91 | P90 | (PDR8) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port A data register (PDRA)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00000AH | (PDRB) | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



- Port B data register (PDRB)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00000BH | (PDRA) | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port C data register (PDRC)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00000CH | (Disabled) | — | — | — | — | PC3 | PC2 | PC1 | PC0 | XXXXXXXXB |
| | | — | — | — | — | R/W | R/W | R/W | R/W | |

- Port 0 direction register (DDR0)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000010H | (DDR1) | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 1 direction register (DDR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000011H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | (DDR0) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 2 direction register (DDR2)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000012H | (DDR3) | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 3 direction register (DDR3)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000013H | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | (DDR2) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 4 direction register (DDR4)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000014H | (DDR5) | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

*(Continued)*

- Port 5 direction register (DDR5)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000015H | D57 | D56 | D55 | D54 | D53 | D52 | D51 | D50 | (DDR4) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 6 direction register (DDR6)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000016H | (DDR7) | D67 | D66 | D65 | D64 | D63 | D62 | D61 | D60 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



- Port 7 direction register (DDR7)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000017H | — | — | — | D74 | D73 | D72 | D71 | D70 | (DDR6) | ---00000B |
| | — | — | — | R/W | R/W | R/W | R/W | R/W | | |

- Port 8 direction register (DDR8)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000018H | (DDR9) | D87 | D86 | D85 | D84 | D83 | D82 | D81 | D80 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 9 direction register (DDR9)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000019H | D97 | D96 | D95 | D94 | D93 | D92 | D91 | D90 | (DDR8) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port A direction register (DDRA)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00001AH | (DDRB) | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port B direction register (DDRB)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00001BH | (DDRA) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port C direction register (DDRC)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00001CH | (ODR4) | — | — | — | — | DC3 | DC2 | DC1 | DC0 | 00000000B |
| | | — | — | — | — | R/W | R/W | R/W | R/W | |

- Port 4 output pin register (ODR4)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00001DH | (DDRC) | OD47 | OD46 | OD45 | OD44 | OD43 | OD42 | OD41 | OD40 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Port 0 input pull-up resistor setup register (RDR0)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00008CH | (RDR1) | RD07 | RD06 | RD05 | RD04 | RD03 | RD02 | RD01 | RD00 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

*(Continued)*

*(Continued)*

- Port 1 input pull-up resistor setup register (RDR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00008D$_H$ | RD17 | RD16 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | (RDR0) | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Port 6 input pull-up resistor setup register (RDR6)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00008E$_H$ | (Disabled) | RD67 | RD66 | RD65 | RD64 | RD63 | RD62 | RD61 | RD60 | 00000000$_B$ |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



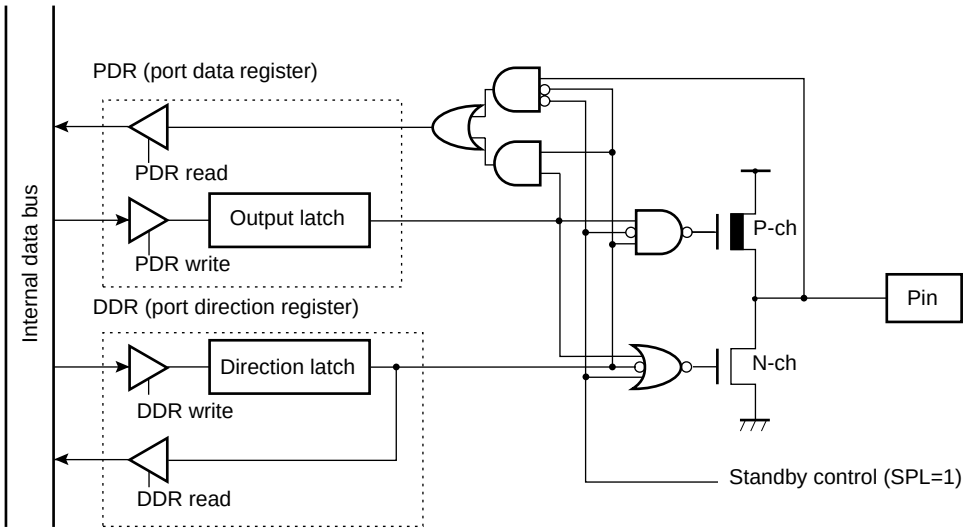
- Analog input enable register (ADER)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00001E$_H$ | (Disabled) | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 | 11111111$_B$ |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
—:Reserved
X:Undefined

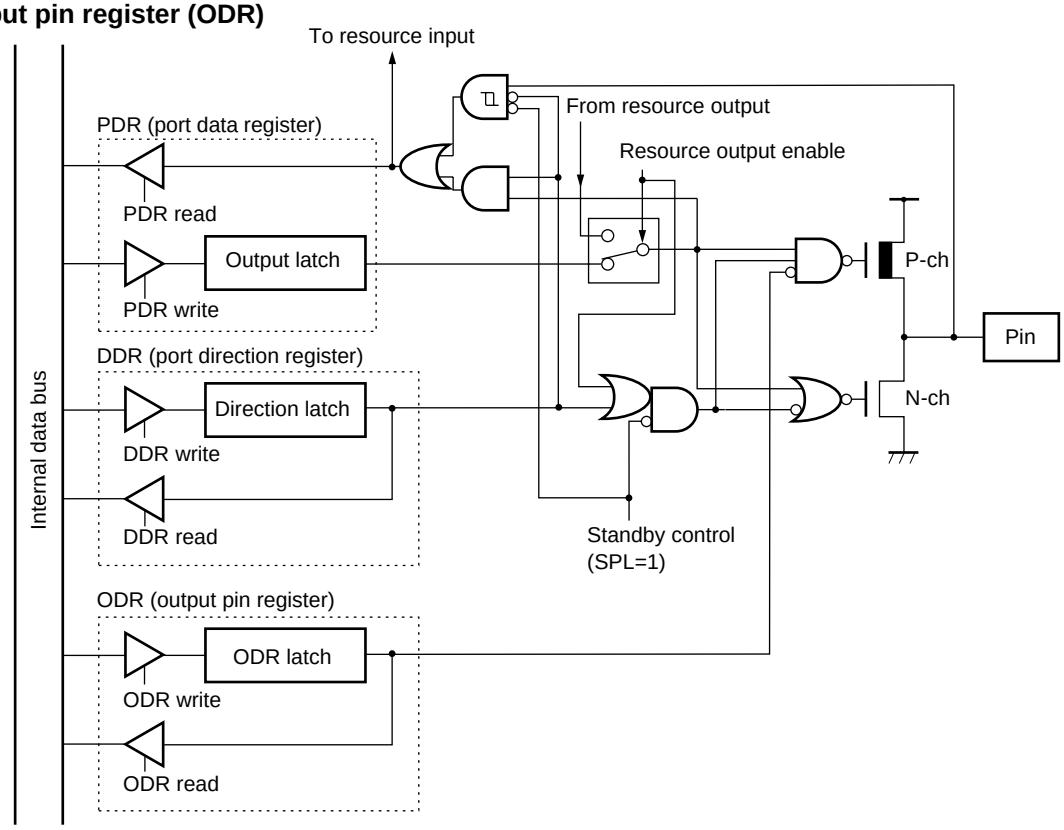
### (3) Block Diagram

- **Input/output port**



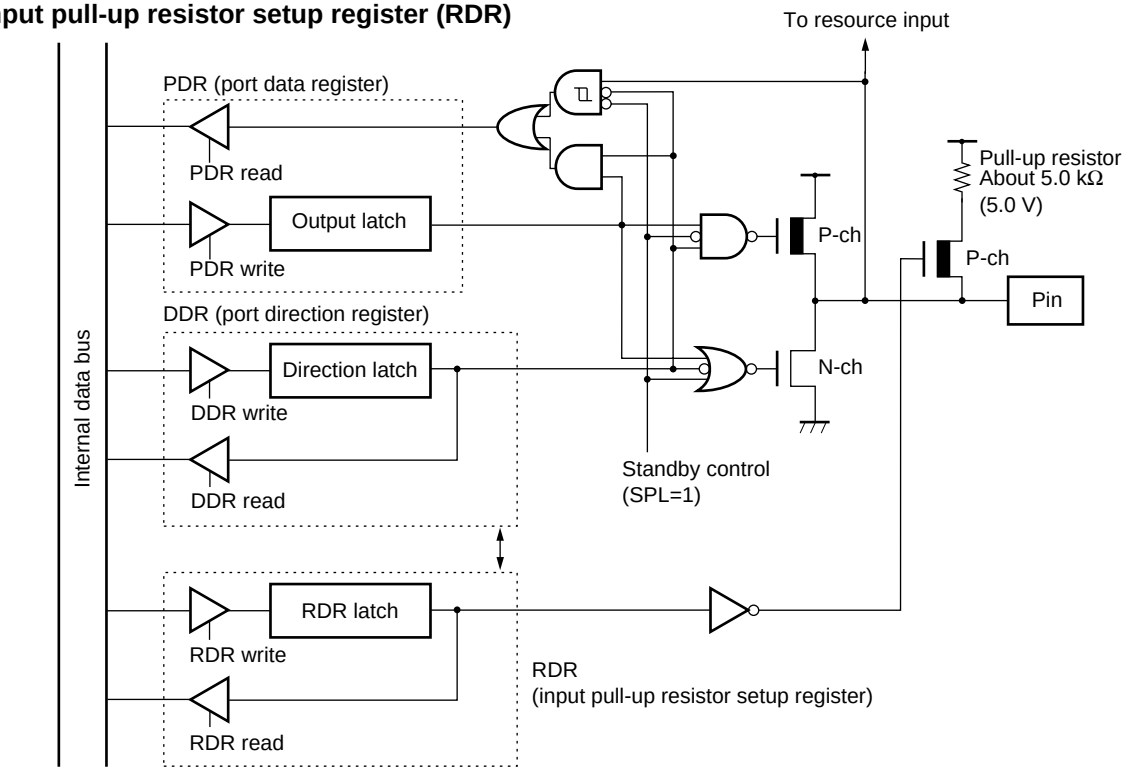

Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

- **Output pin register (ODR)**



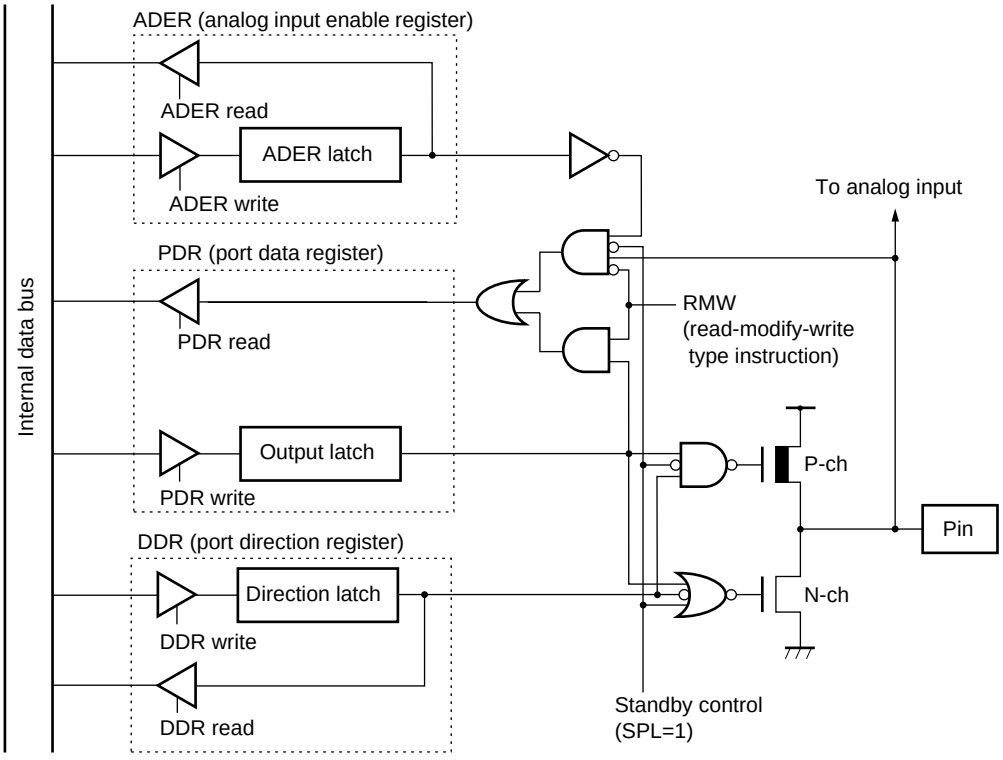

Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

- **Input pull-up resistor setup register (RDR)**




Standby control: Stop, timebase timer mode and SPL=1

- **Analog input enable register (ADER)**




Standby control: Stop, timebase timer mode and SPL=1

## 2. Timebase Timer

The timebase timer is a 18-bit free run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types of $2^{12}$/HCLK, $2^{14}$/HCLK, $2^{16}$/HCLK, and $2^{19}$/HCLK.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer etc.

### (1) Register Configuration

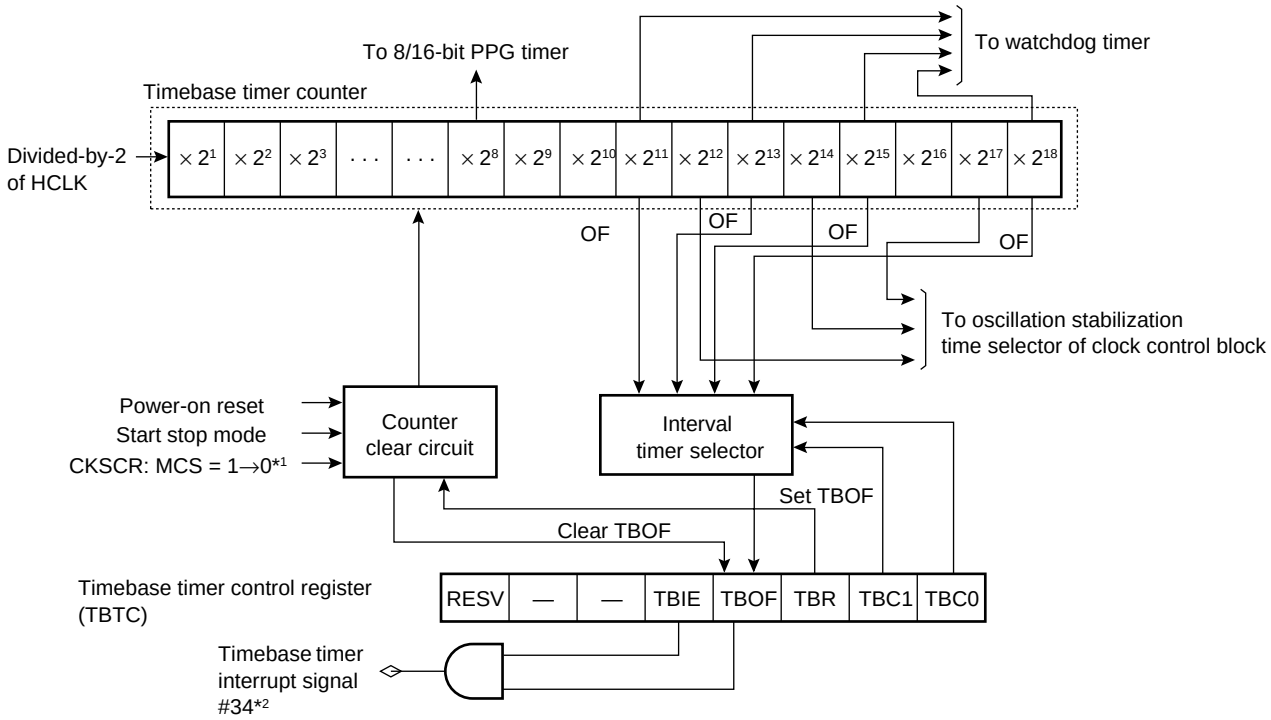
- Timebase timer control register (TBTC)



| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 0000A9H | RESV | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 | (WDTC) | 1--00100B |
| | — | — | — | R/W | R/W | W | R/W | R/W | | |

R/W:Readable and writable
W:Write only
—:Unused
RESV: Reserved bit

### (2) Block Diagram




OF: Overflow
HCLK: Oscillation clock
*1: Switch machine clock from oscillation clock to PLL clock
*2: Interrupt signal

## 3. Watchdog Timer

The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

### (1) Register Configuration

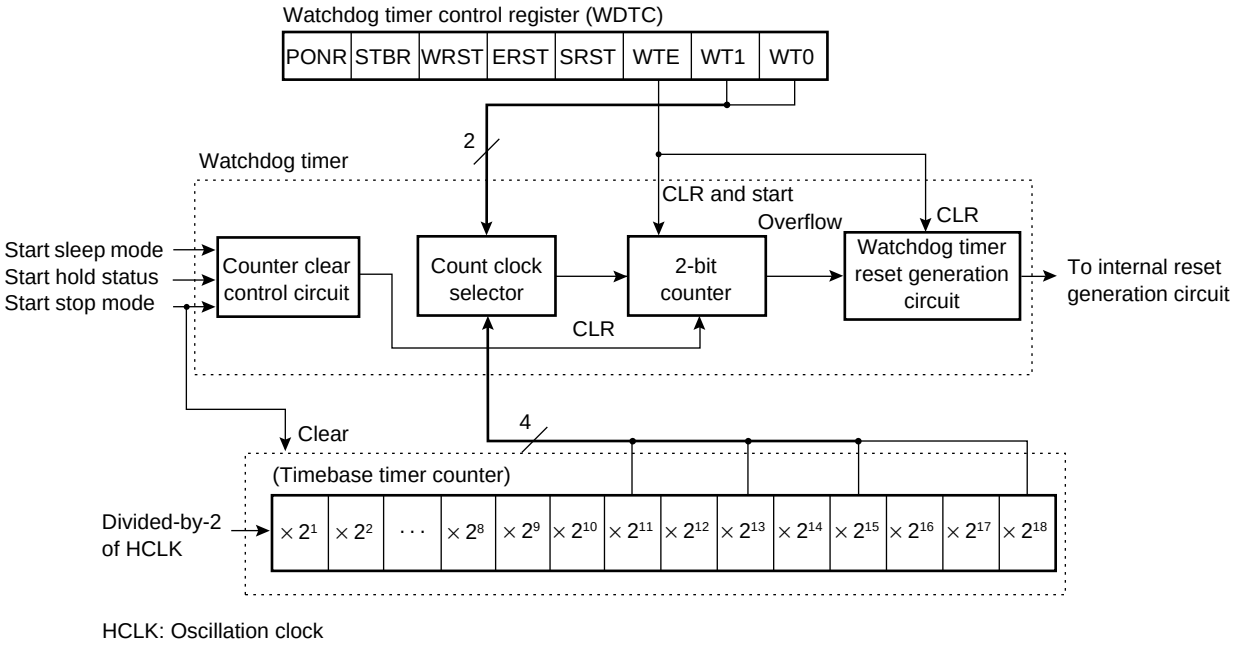
- Watchdog timer control register (WDTC)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 0000A8H | (TBTC) | PONR | STBR | WRST | ERST | SRST | WTE | WT1 | WT0 | XXXXXXXXB |
| | | R | R | R | R | R | W | W | W | |

R:Read only
W:Write only
X:Indeterminate



### (2) Block Diagram




HCLK: Oscillation clock

## 4. 8/16-bit PPG Timer

The 8/16-bit PPG timer is a 2-CH reload timer module for outputting pulse having given frequencies/duty ratios.

The two modules performs the following operation by combining functions.

- 8-bit PPG output 2-CH independent operation mode
  This is a mode for operating independent 2-CH 8-bit PPG timer, in which PPG0 and PPG1 pins correspond to outputs from PPG0 and PPG1 respectively.
- 16-bit PPG timer output operation mode
  In this mode, PPG0 and PPG1 are combined to be operated as a 1-CH 8/16-bit PPG timer operating as a 16-bit timer. Because PPG0 and PPG1 outputs are reversed by an underflow from PPG1 outputting the same output pulses from PPG0 and PPG1 pins.
- 8 + 8-bit PPG timer output operation mode
  In this mode, PPG0 is operated as an 8-bit communications prescaler, in which an underflow output of PPG0 is used as a clock source for PPG1. A toggle output of PPG0 and PPG output of PPG1 are output from PPG0 and PPG1 respectively.
- PPG output operation
  A pulse wave with any period/duty ratio is output. The module can also be used as a D/A converter with an external add-on circuit.

### (1) Register Configuration

- PPG0 operating mode control register ch.0 (PPGC0)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000044H | (PPGC1) | PEN0 | — | PE00 | PIE0 | PUF0 | — | — | RESV | 0X000XX1B |
| | | R/W | — | R/W | R/W | R/W | — | — | — | |

- PPG1 operating mode control register ch.1 (PPGC1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000045H | PEN1 | — | PEI0 | PIE1 | PUF1 | MD1 | MD0 | RESV | (PPGC0) | 0X000001B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |



- PPG0, 1 output control register ch.0, ch.1(PPGOE)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000046H | (Disabled) | PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | — | — | 000000XXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | — | — | |

- PPG0 reload register H ch.0 (PRLH0)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000041H | | | | | | | | | (PRLL0) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- PPG1 reload register H ch.1 (PRLH1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000043H | | | | | | | | | (PRLL1) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- PPG0 reload register L ch.0 (PRLL0)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000040H | (PRLH0) | | | | | | | | | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

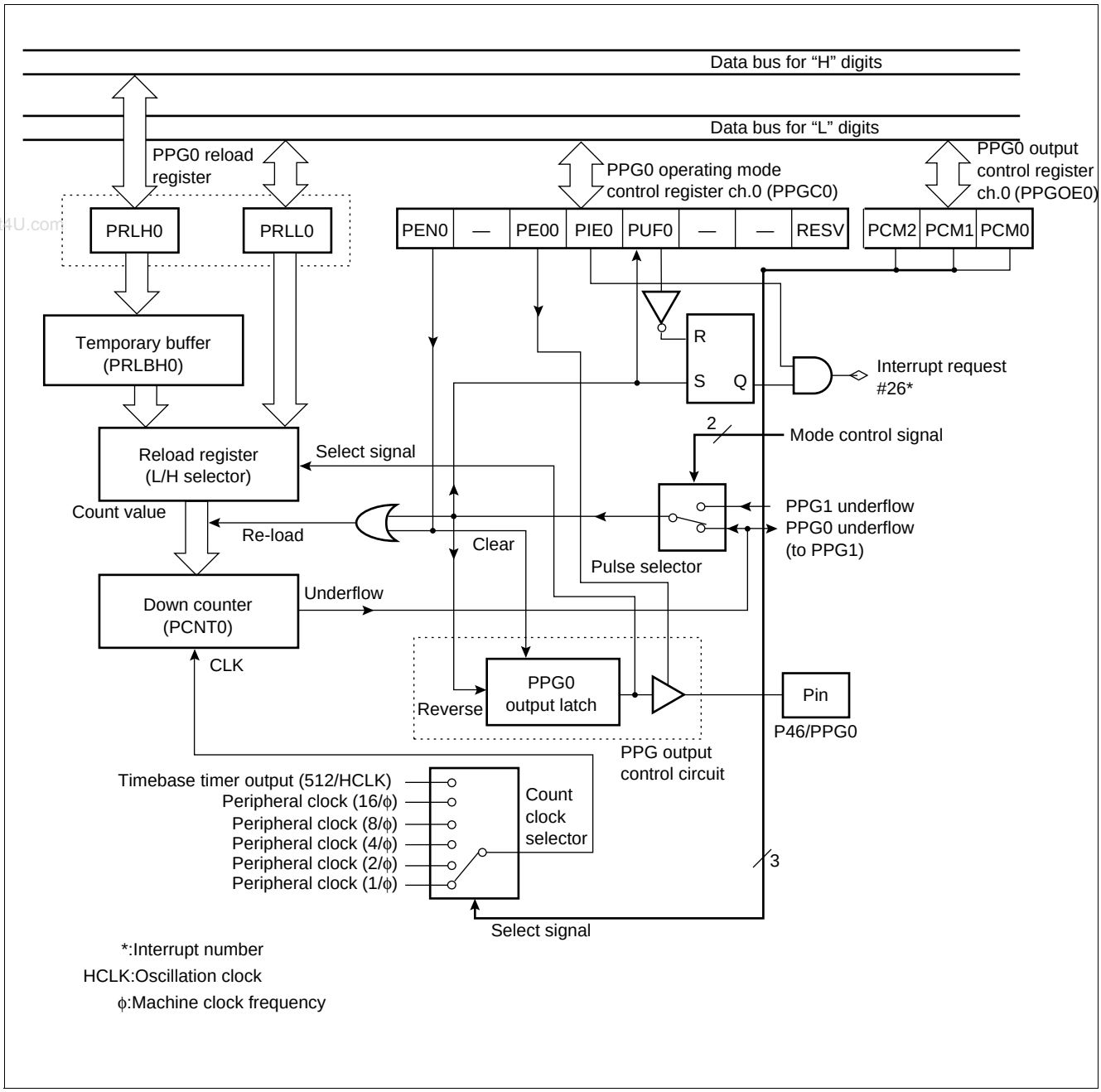
- PPG1 reload register L ch.1 (PRLL1)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000042H | (PRLH1) | | | | | | | | | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

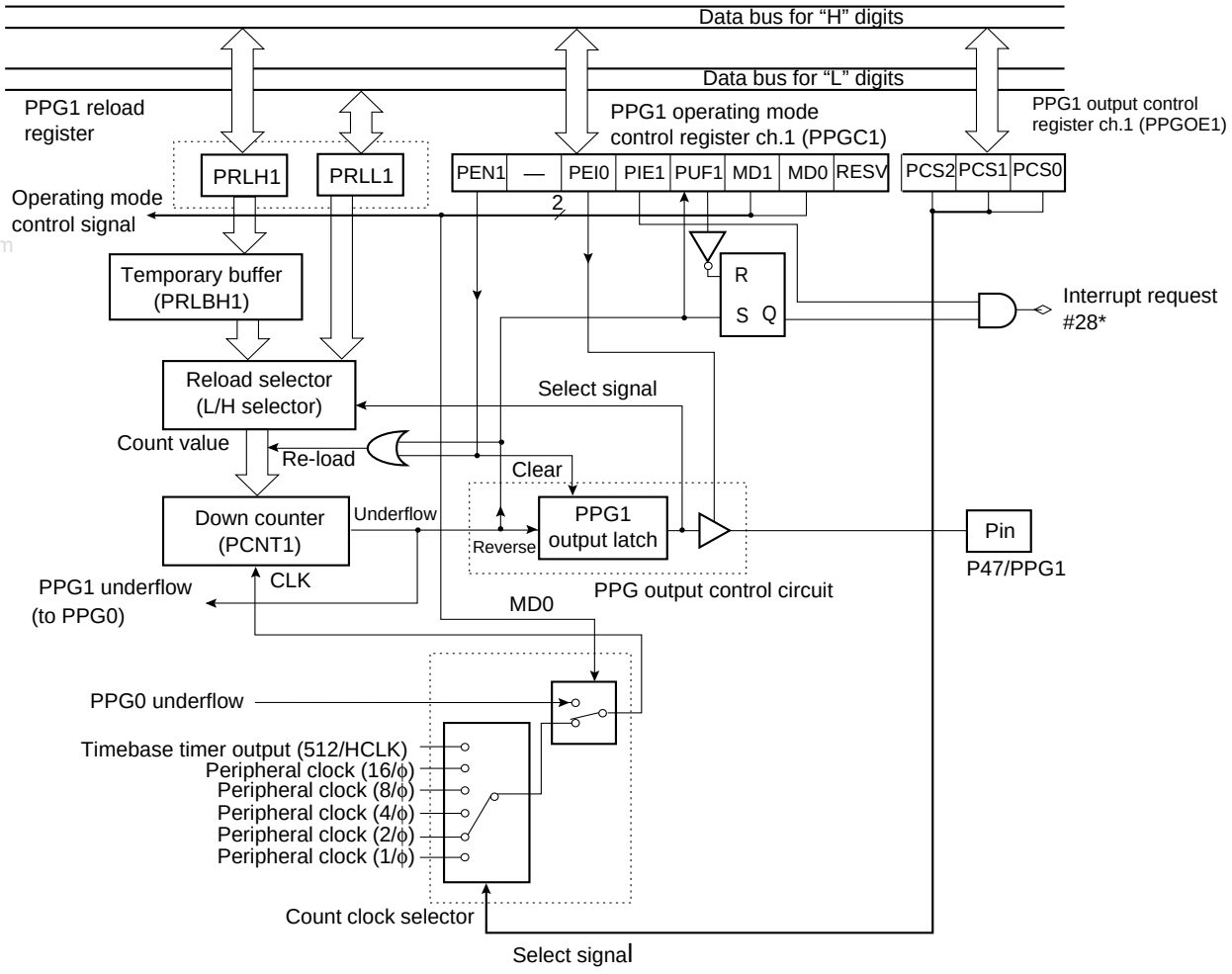
R/W:Readable and writable
—:Reserved
X:Undefined
RESV: Reserved bit

### (2) Block Diagram

- **Block diagram of 8/16-bit PPG timer (ch.0)**



- **Block diagram of 8/16-bit PPG timer (ch.1)**

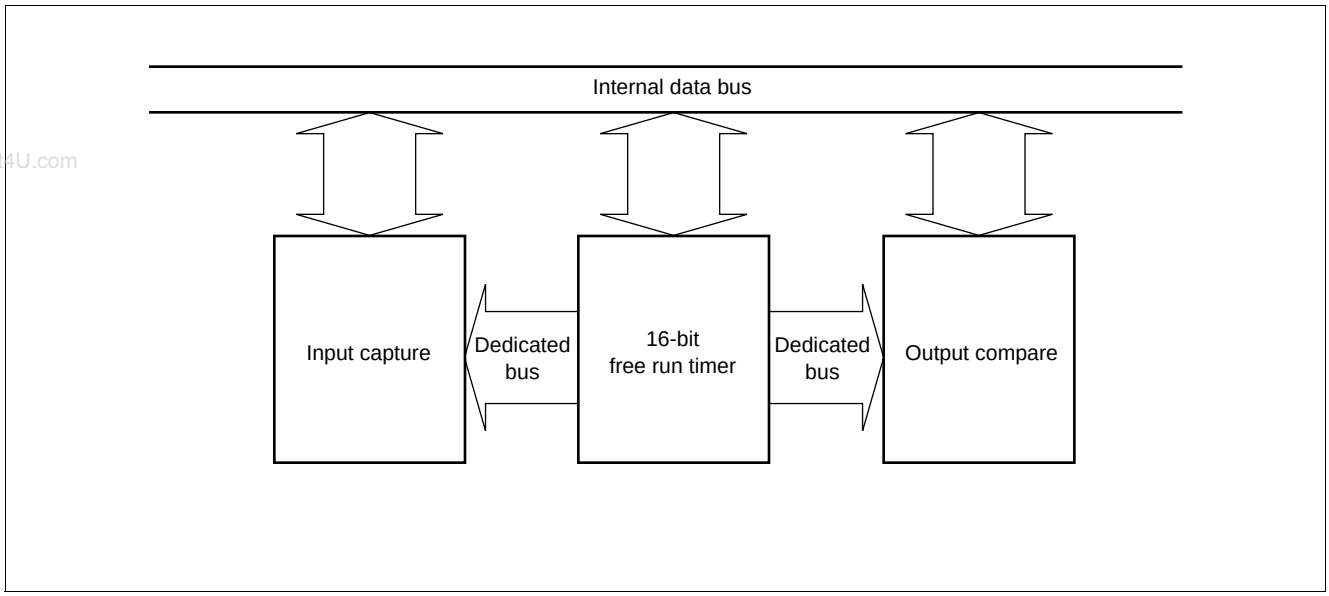



*:Interrupt number
HCLK:Oscillation clock
ϕ:Machine clock frequency

## 5. 16-bit I/O timer

The 16-bit I/O timer module consists of one 16-bit free run timer, two input capture circuits, and four output comparators. This module allows two independent waveforms to be output on the basis of the 16-bit free run timer. Input pulse width and external clock periods can, therefore, be measured.

- **Block Diagram**



### (1) 16-bit free run Timer

The 16-bit free run timer consists of a 16-bit up counter, a control register, and a communications prescaler register. The value output from the timer counter is used as basic timer (base timer) for input capture (ICU) and output compare (OCU).

- A counter operation clock can be selected from four internal clocks (ϕ/4, ϕ/16, ϕ/32 and ϕ/64).
- An interrupt can be generated by overflow of counter value or compare match with OCU compare register 0. (Compare match requires mode setup.)
- The counter value can be initialized to "0000H" by a reset, software clear or compare match with OCU compare register 0.



- **Register Configuration**

- free run timer data register (TCDT)

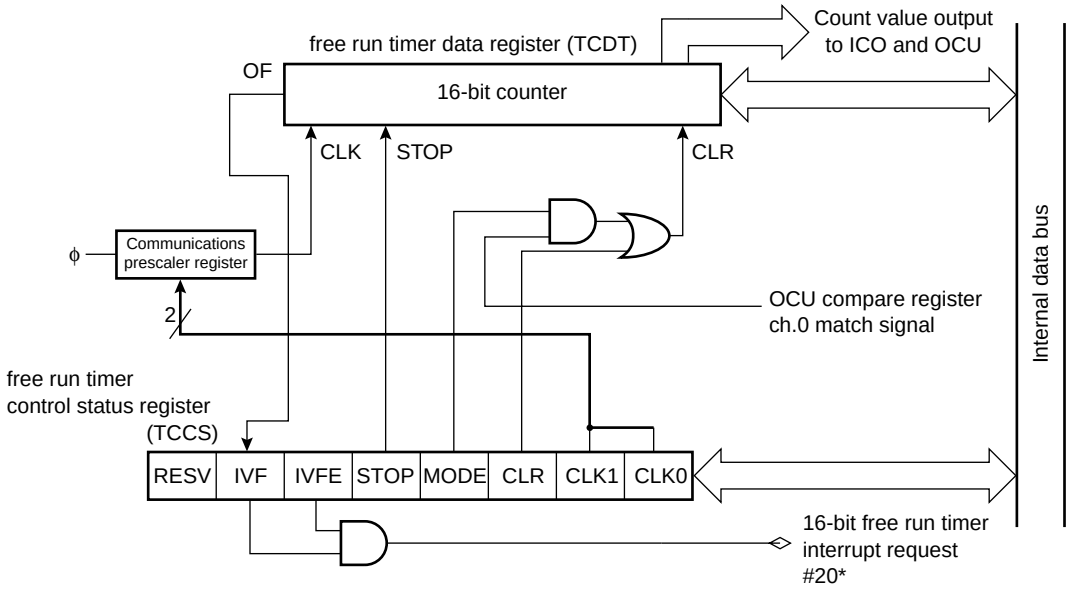
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000056H<br>000057H | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- free run timer control status register (TCCS)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000058H | (Disabled) | RESV | IVF | IVFE | STOP | MODE | CLR | CLK1 | CLK0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W: Readable and writable
RESV: Reserved bit

- **Block Diagram**




*:Interrupt number
ϕ:Machine clock frequency
OF:Overflow

### (2) Input Capture (ICU)

The input capture (ICU) generates an interrupt request to the CPU simultaneously with a storing operation of current counter value of the 16-bit free run timer to the ICU data register (IPCP) upon an input of a trigger edge to the external pin.

There are four sets (four channels) of the input capture external pins and ICU data registers, enabling measurements of maximum of four events.

- The input capture has two sets of external input pins (IN0, IN1) and ICU registers (IPCP), enabling measurements of maximum of four events.
- A trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 16-bit free run timer to the ICU data register (IPCP).
- The input compare conforms to the extended intelligent I/O service (EI$^2$OS).
- The input capture (ICU) function is suited for measurements of intervals (frequencies) and pulse widths.



- **Register Configuration**

- ICU data register ch.0, ch.1 (IPCP0, IPCP1)

| | Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IPCP0(high): | 000051H | CP15 | CP14 | CP13 | CP12 | CP11 | CP10 | CP09 | CP08 | (IPCP0 low, IPCP1 low) | XXXXXXXXB |
| IPCP1(high): | 000053H | | | | | | | | | | |
| | | R | R | R | R | R | R | R | R | | |

| | Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IPCP0(low): | 000050H | (IPCP0 high, IPCP1 high) | CP07 | CP06 | CP05 | CP04 | CP03 | CP02 | CP01 | CP00 | XXXXXXXXB |
| IPCP1(low): | 000052H | | | | | | | | | | |
| | | | R | R | R | R | R | R | R | R | |

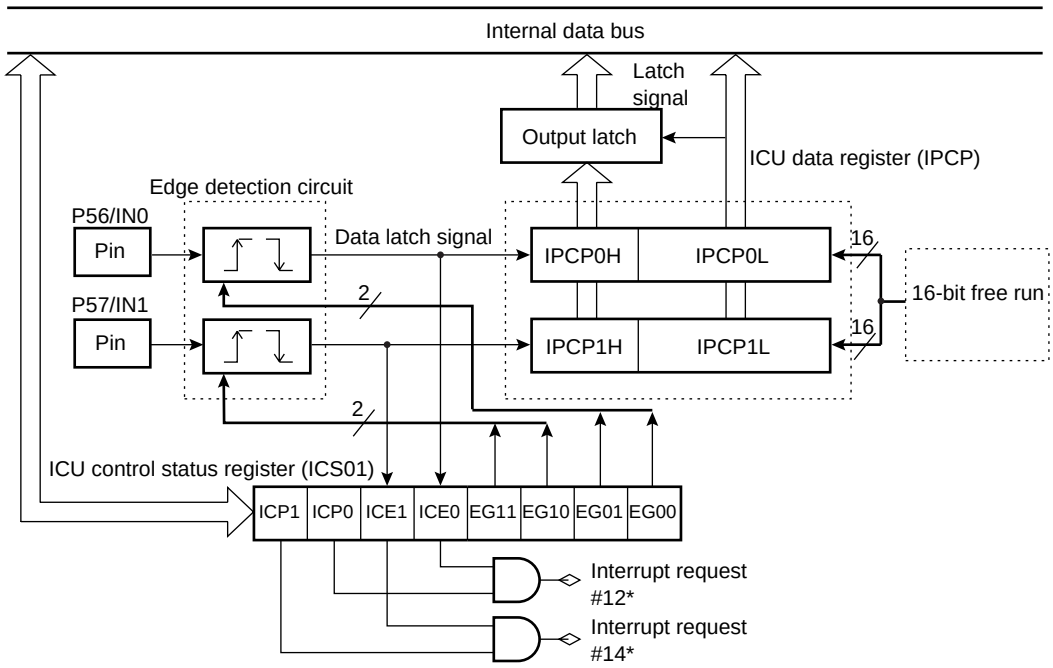
Note: This register holds a 16-bit free run timer value when the valid edge of the corresponding external pin input waveform is detected. (You can word-access this register, but you cannot program it.)

- ICU control status register (ICS01)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000054H | (Disabled) | ICP1 | ICP0 | ICE1 | ICE0 | EG11 | EG10 | EG01 | EG00 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
R:Read only
X:Undefined

- **Block Diagram**




*: Interrupt number

### (3) Output Compare (OCU)

The output compare (OCU) is two sets of compare units consisting of four-channel OCU compare registers, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 16-bit free run timer.

The OUT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the CMOD bit.

- **Register Configuration**



- OCU control status register ch.1, ch.3 (OCS1, OCS3)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000063H<br>000065H | — | — | — | CMOD | OTE1 | OTE0 | OTD1 | OTD0 | (OCS0, OCS2) | ---00000B |
| | — | — | — | R/W | R/W | R/W | R/W | R/W | | |

- OCU control status register ch.0, ch.2 (OCS0, OCS2)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000062H<br>000064H | (OCS1, OCS3) | ICP1 | ICP0 | ICE1 | ICE0 | — | — | CST1 | CST0 | 0000--00B |
| | | R/W | R/W | R/W | R/W | — | — | R/W | R/W | |

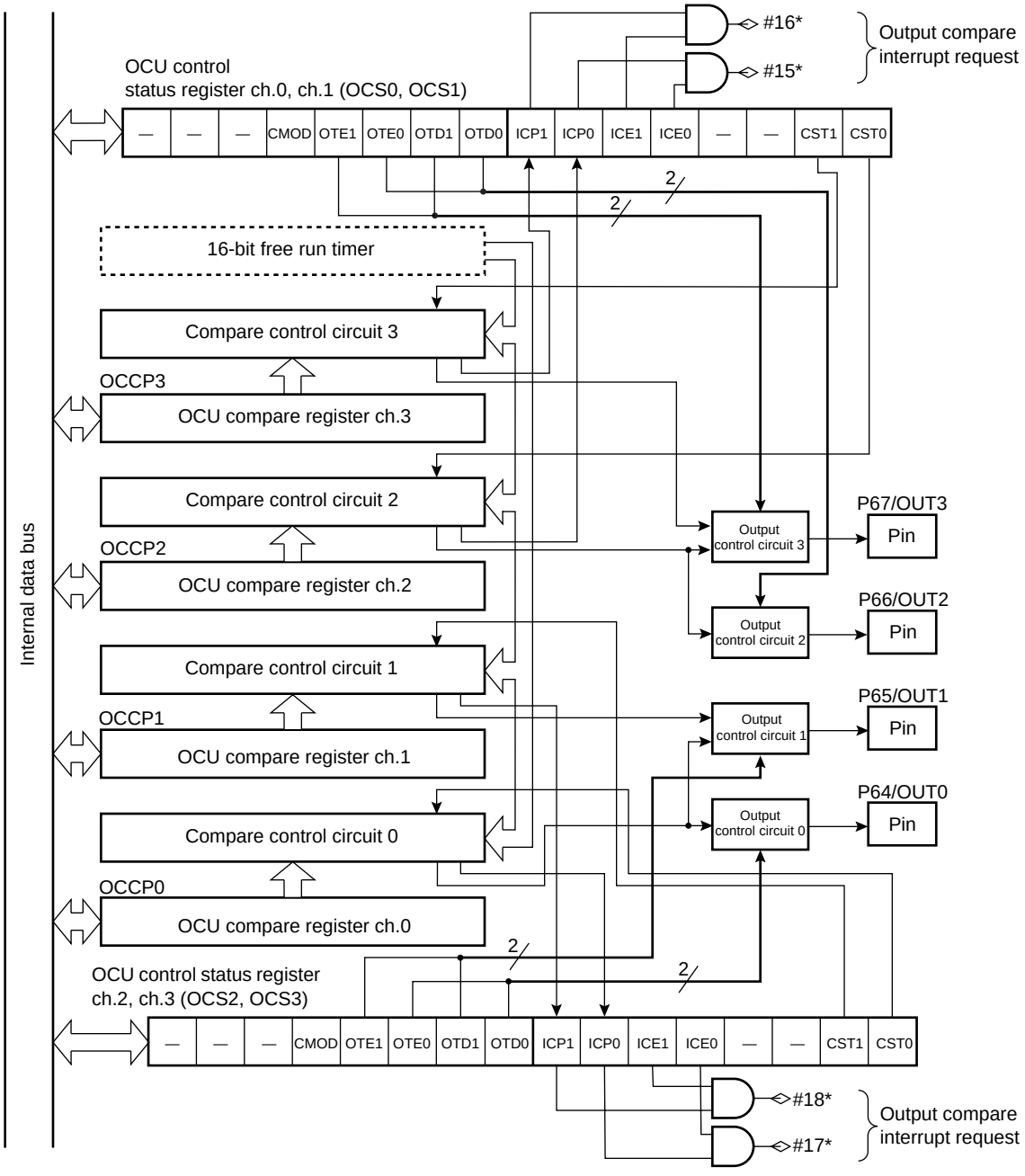
- OCU compare register ch.0 to ch.3 (OCCP0 to OCCP3)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| OCCP0 (high order address): 00005BH<br>OCCP1 (high order address): 00005DH<br>OCCP2 (high order address): 00005FH<br>OCCP3 (high order address): 000061H | C15 | C14 | C13 | C12 | C11 | C10 | C09 | C08 | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| OCCP0 (low order address): 00005AH<br>OCCP1 (low order address): 00005CH<br>OCCP2 (low order address): 00005EH<br>OCCP3 (low order address): 000060H | C07 | C06 | C05 | C04 | C03 | C02 | C01 | C00 | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
—:Reserved
X:Undefined

- **Block diagram**



## 6. 8/16-bit up/down counter/timer

The 8/16-bit up/down counter/timer consists of six event input pins, two 8-bit up/down counters, two 8-bit reload compare registers, and their controllers.

### (1) Register configuration

- Up/down count register 0 (UDCR0)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000070H | (UDCR1) | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B |
| | | R | R | R | R | R | R | R | R | |



- Up/down count register 1 (UDCR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000071H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | (UDCR0) | 00000000B |
| | R | R | R | R | R | R | R | R | | |

- Reload compare register 0 (RCR0)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000072H | (RCR1) | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | 00000000B |
| | | W | W | W | W | W | W | W | W | |

- Reload compare register 1 (RCR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000073H | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | (RCR0) | 00000000B |
| | W | W | W | W | W | W | W | W | | |

- Counter status register 0, 1 (CSR0, CSR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000074H<br>000078H | (Reserved area) | CSTR | CITE | UDIE | CMPF | OVFF | UDFF | UDF1 | UDF0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R | R | |

- Counter control register 0, 1 (CCRL0, CCRL1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000076H<br>00007AH | (CCRH0, CCRH1) | — | CTUT | UCRE | RLDE | UDCC | CGSC | CGE1 | CGE0 | -0000000B |
| | | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Counter control register 0 (CCRH0)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000077H | M16E | CDCF | CFIE | CLKS | CMS1 | CMS0 | CES1 | CES0 | (CCRL0) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

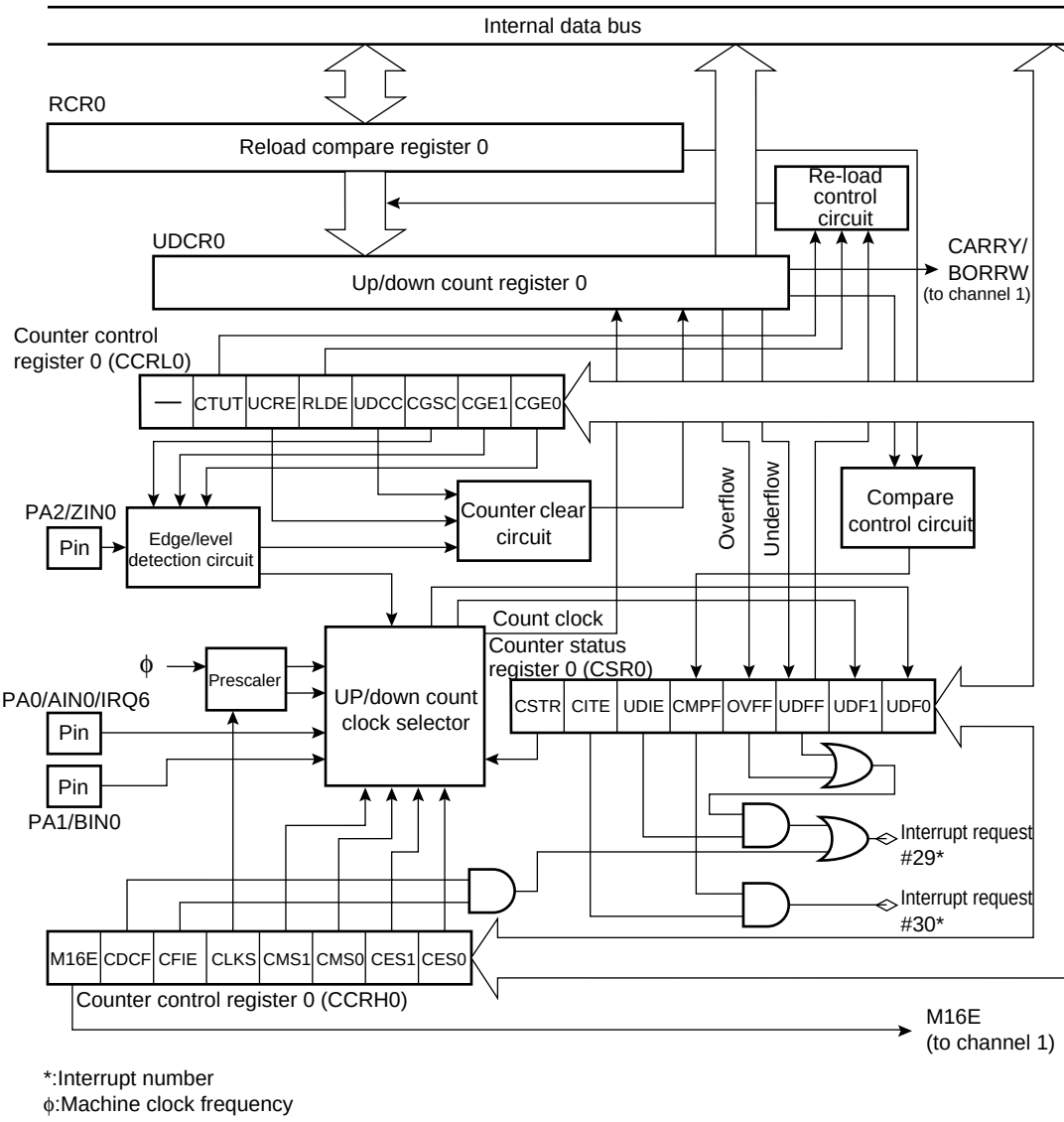
- Counter control register 1 (CCRH1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00007BH | — | CDCF | CFIE | CLKS | CMS1 | CMS0 | CES1 | CES0 | (CCRL1) | -0000000B |
| | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

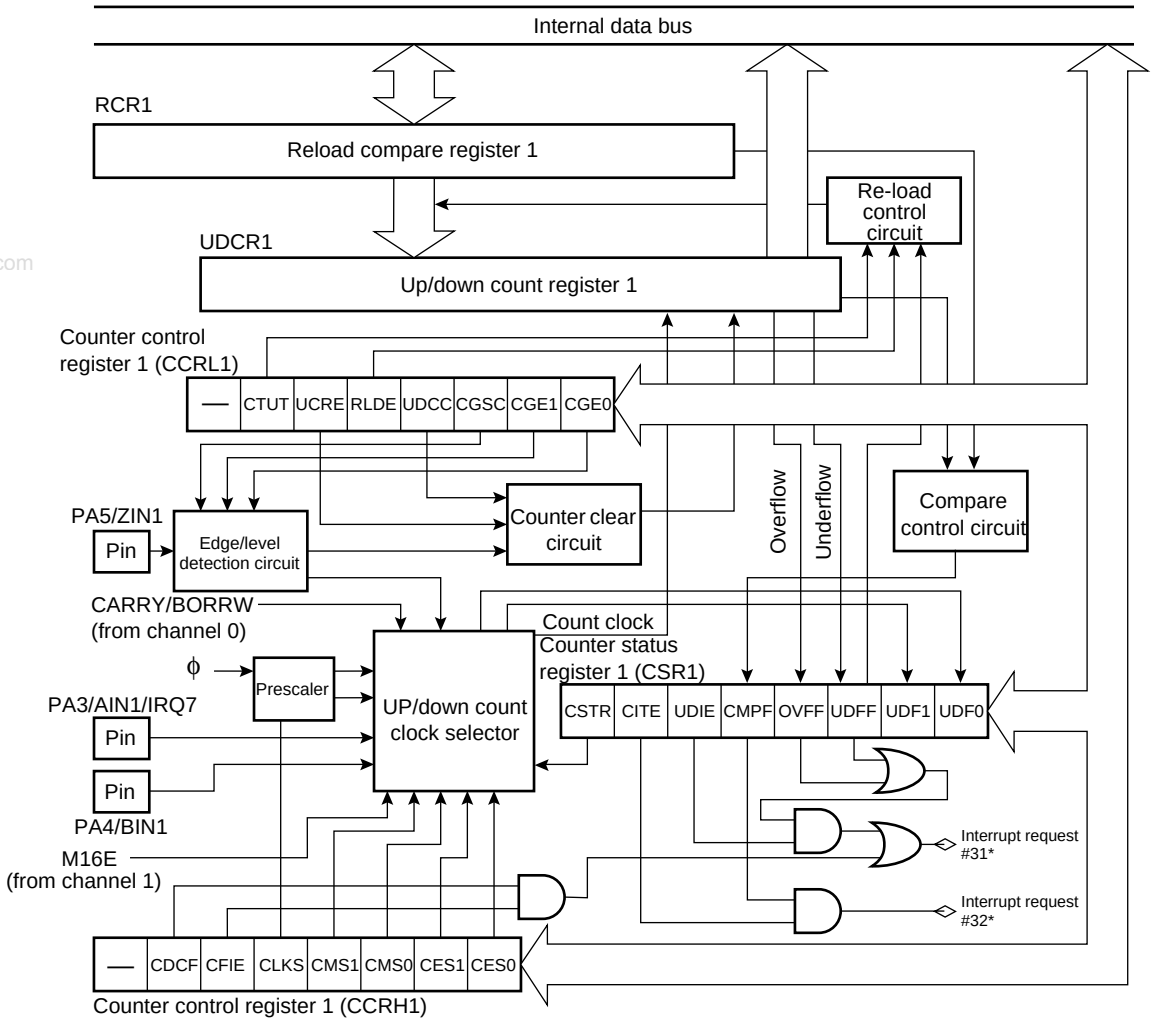
R/W:Readable and writable
R:Read only
W:Write only
—:Undefined

### (2) Block Diagram

- **Block diagram of 8/16-bit up/down counter/timer 0**



- **Block diagram of 8/16-bit up/down counter/timer 1**




*:Interrupt number
ϕ:Machine clock frequency

## 7. Extended I/O serial interface

The extended I/O serial interface transfers data using a clock synchronization system having an 8-bit x 1 channel configuration.

For data transfer, you can select LSB first/MSB first.

### (1) Register Configuration

- Serial mode control upper status register 0 to 2 (SMCSH0 to SMCSH2)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| SMCSH0: 000049H<br>SMCSH1: 00004DH<br>SMCSH2: 00007DH | SMD2 | SMD1 | SMD0 | SIE | SIR | BUSY | STOP | STRT | (SMCSL) | 00000010B |
| | R/W | R/W | R/W | R/W | R/W | R | R/W | R/W | | |

- Serial mode control lower status register 0 to 2 (SMCSL0 to SMCSL2)

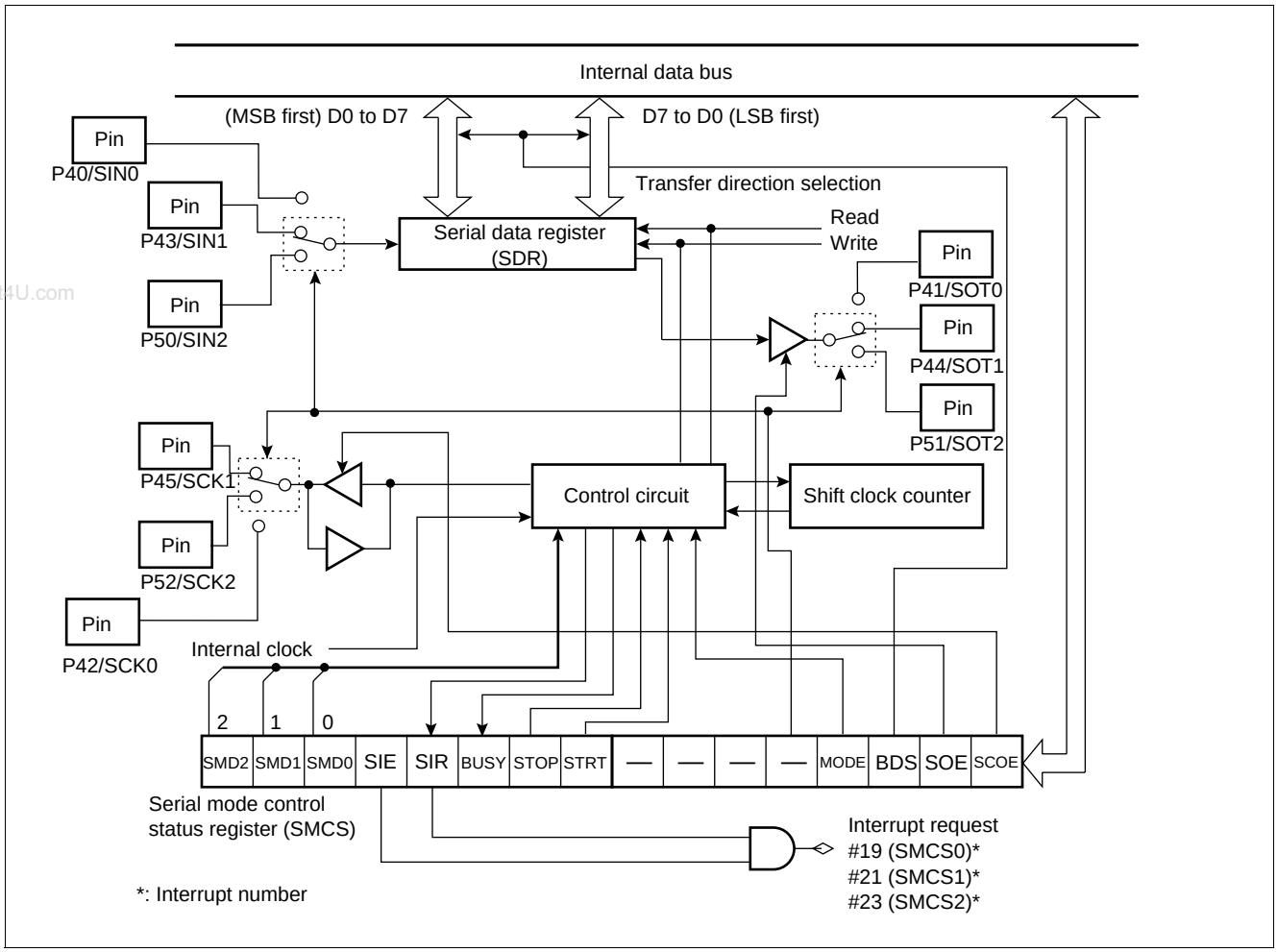
| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| SMCSL0: 000048H<br>SMCSL1: 00004CH<br>SMCSL2: 00007CH | (SMCSH) | — | — | — | — | MODE | BDS | SOE | SCOE | ----0000B |
| | | — | — | — | — | R/W | R/W | R/W | R/W | |

- Serial data register 0 to 2 (SDR0 to SDR2)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| SDR0: 00004AH<br>SDR1: 00004EH<br>SDR2: 00007EH | (Disabled) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
R:Read only
—:Reserved
X:Undefined

### (2) Block Diagram



## 8. I²C Interface

The I²C interface is a serial I/O port supporting Inter IC BUS operating as master/slave devices on I²C bus.

The MB90570/A series contains one channel of an I²C interface, having the following features.

- Master/slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transmission direction detection function
- Repeated generation function start condition and detection function
- Bus error detection function



### (1) Register Configuration

- I²C bus status register (IBSR)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000068H | (IBCR) | BB | RSC | AL | LRB | TRX | AAS | GCA | FBT | 00000000B |
| | | R | R | R | R | R | R | R | R | |

- I²C bus control register (IBCR)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000069H | BER | BEIE | SCC | MSS | ACK | GCAA | INTE | INT | (IBSR) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- I²C bus clock control register (ICCR)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00006AH | (IADR) | — | — | EN | CS4 | CS3 | CS2 | CS1 | CS0 | --0XXXXXB |
| | | — | — | R/W | R/W | R/W | R/W | R/W | R/W | |

- I²C bus address register (IADR)

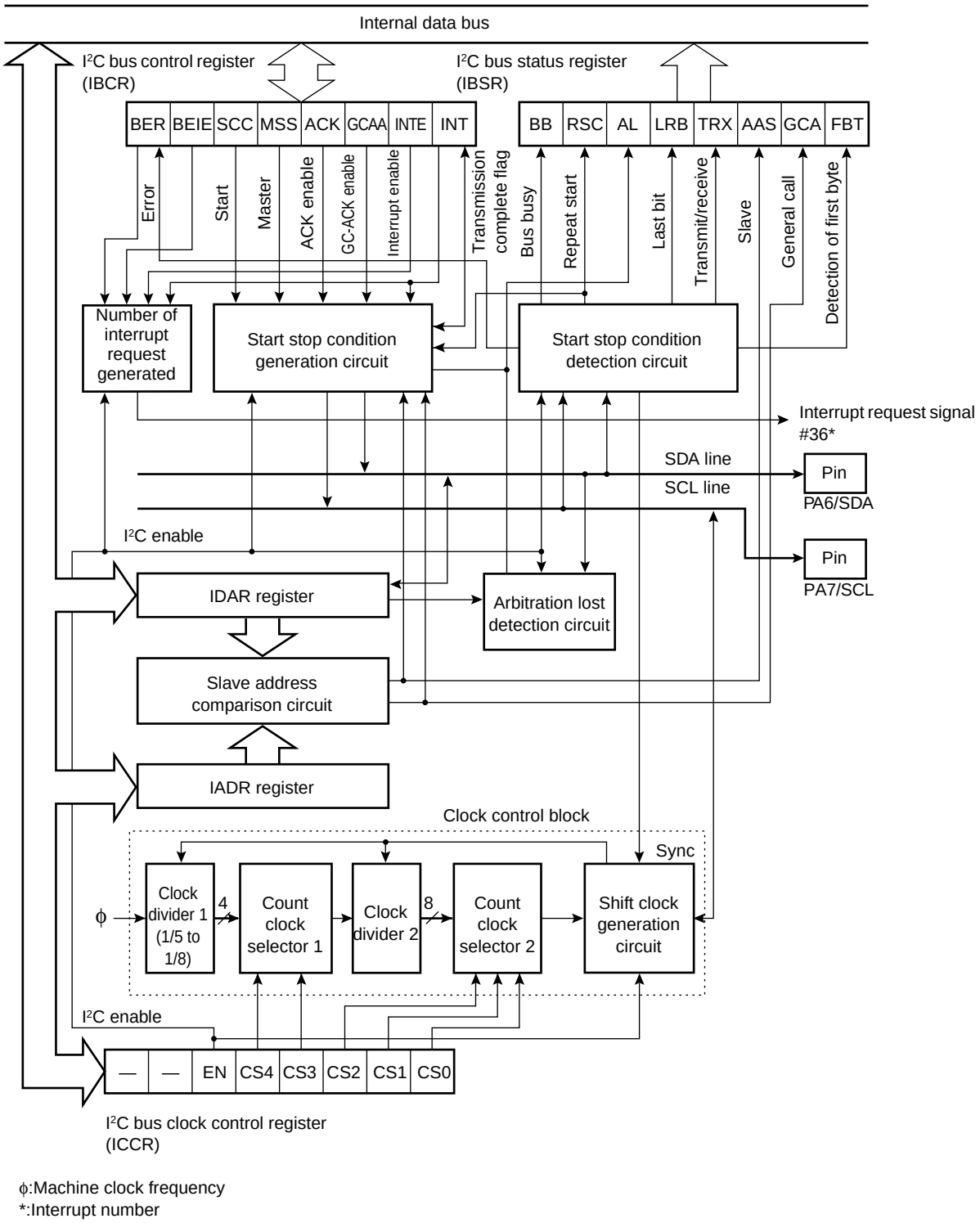
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ··· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00006BH | — | A6 | A5 | A4 | A3 | A2 | A1 | A0 | (ICCR) | -XXXXXXXB |
| | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- I²C bus data register (IDAR)

| Address | bit 15 ··· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00006CH | (Disabled) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W: Readable and writable
R: Read only
—: Reserved
X: Indeterminate

### (2) Block Diagram




ϕ:Machine clock frequency
*:Interrupt number

## 9. UART0 (SCI), UART1 (SCI)

UART0 (SCI) and UART1 (SCI) are general-purpose serial data communication interfaces for performing synchronous or asynchronous communication (start-stop synchronization system).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
  Clock asynchronized (start-stop synchronization system)
- Baud rate: Embedded dedicated baud rate generator
  External clock input possible
  Internal clock (a clock supplied from 8-bit PPG timer ch1 or 16-bit PPG timer can be used.)
  Asynchronization 9615 bps/31250 bps/4808 bps/2404 bps/1202 bps
  CLK synchronization 1 Mbps/500 kbps/250 kbps/125 kbps/62.5 kbps
  } Internal machine clock For 6 MHz, 8 MHz, 10 MHz 12 MHz and 16 MHz
- Data length: 7 bit to 9 bit selective (without a parity bit)
  6 bit to 8 bit selective (with a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
  Overrun error
  Parity error (multi-processor mode is supported, enabling setup of any baud rate by an external clock.)
- Interrupt request: Receive interrupt (receive complete, receive error detection)
  Transmit interrupt (transmission complete)
  Transmit/receive conforms to extended intelligent I/O service ($EI^2OS$)

### (1) Register Configuration

- Serial control register 0,1 (SCR0, SCR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000021H<br>000025H | PEN | P | SBL | CL | A/D | REC | RXE | TXE | (SMR0, SMR1) | 00000100B |
| | R/W | R/W | R/W | R/W | R/W | W | R/W | R/W | | |

- Serial mode register 0, 1 (SMR0, SMR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000020H<br>000024H | (SCR0, SCR1) | MD1 | MD0 | CS2 | CS1 | CS0 | RESV | SCKE | SOE | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



- Serial status register 0,1 (SSR0, SSR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000023H<br>000027H | PE | ORE | FRE | RDRF | TRDE | — | RIE | TIE | (SIDR0, SIDR1/SODR0,SODR1) | 00001-00B |
| | R | R | R | R | R | — | R/W | R/W | | |

- Serial input data register 0,1 (SIDR0, SIDR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000022H<br>000026H | (SSR0, SSR1) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | | R | R | R | R | R | R | R | R | |

- Serial output data register 0,1 (SODR0, SODR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000022H<br>000026H | (SSR0, SSR1) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | | W | W | W | W | W | W | W | W | |

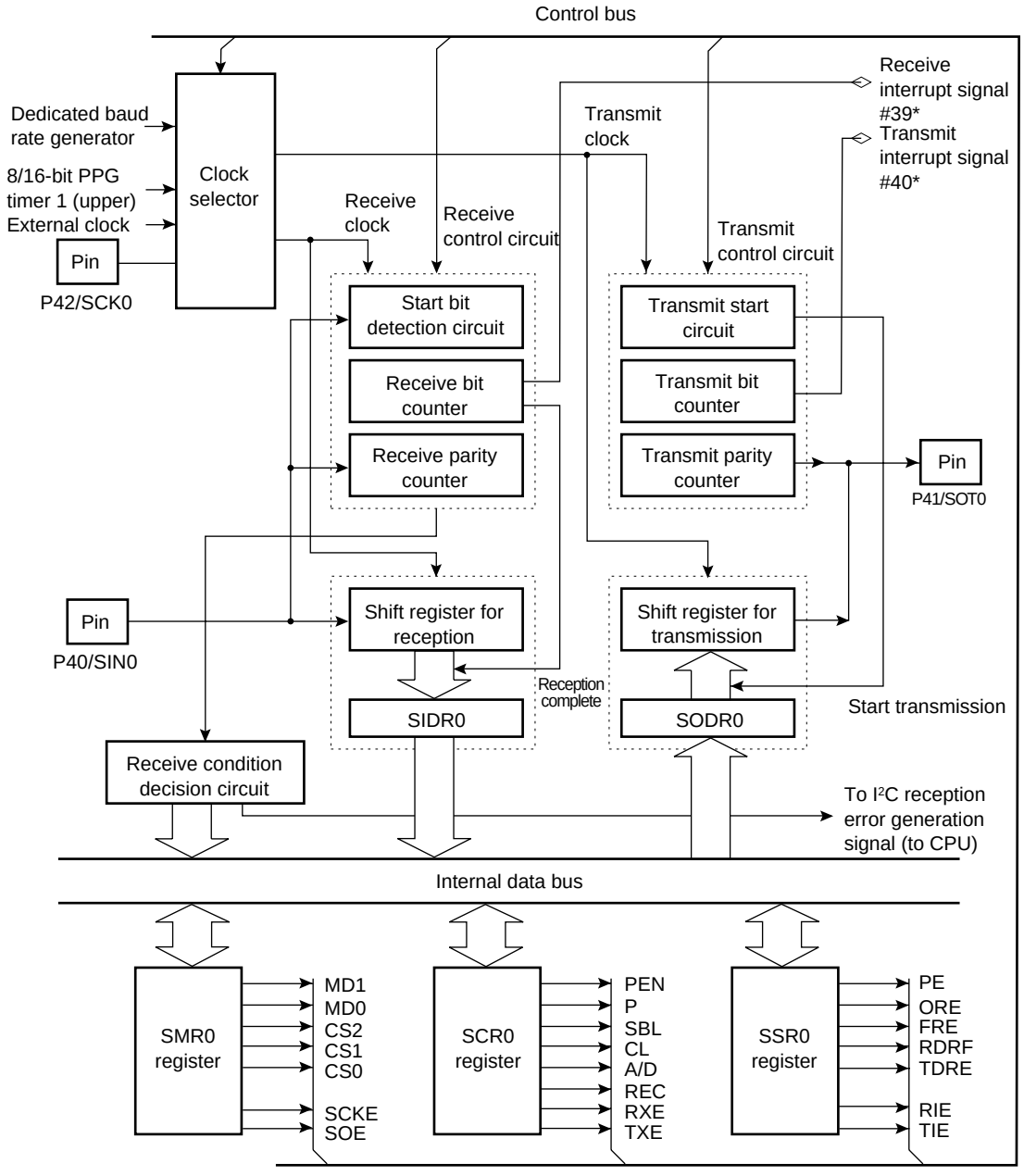
- Communications prescaler control register 0,1 (CDCR0, CDCR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000028H<br>00002AH | (Disabled) | MD | — | — | — | DIV3 | DIV2 | DIV1 | DIV0 | 0---1111B |
| | | R/W | — | — | — | R/W | R/W | R/W | R/W | |

R/W :Readable and writable
R :Read only
W :Write only
— :Reserved
X :Undefined
RESV: Reserved bit

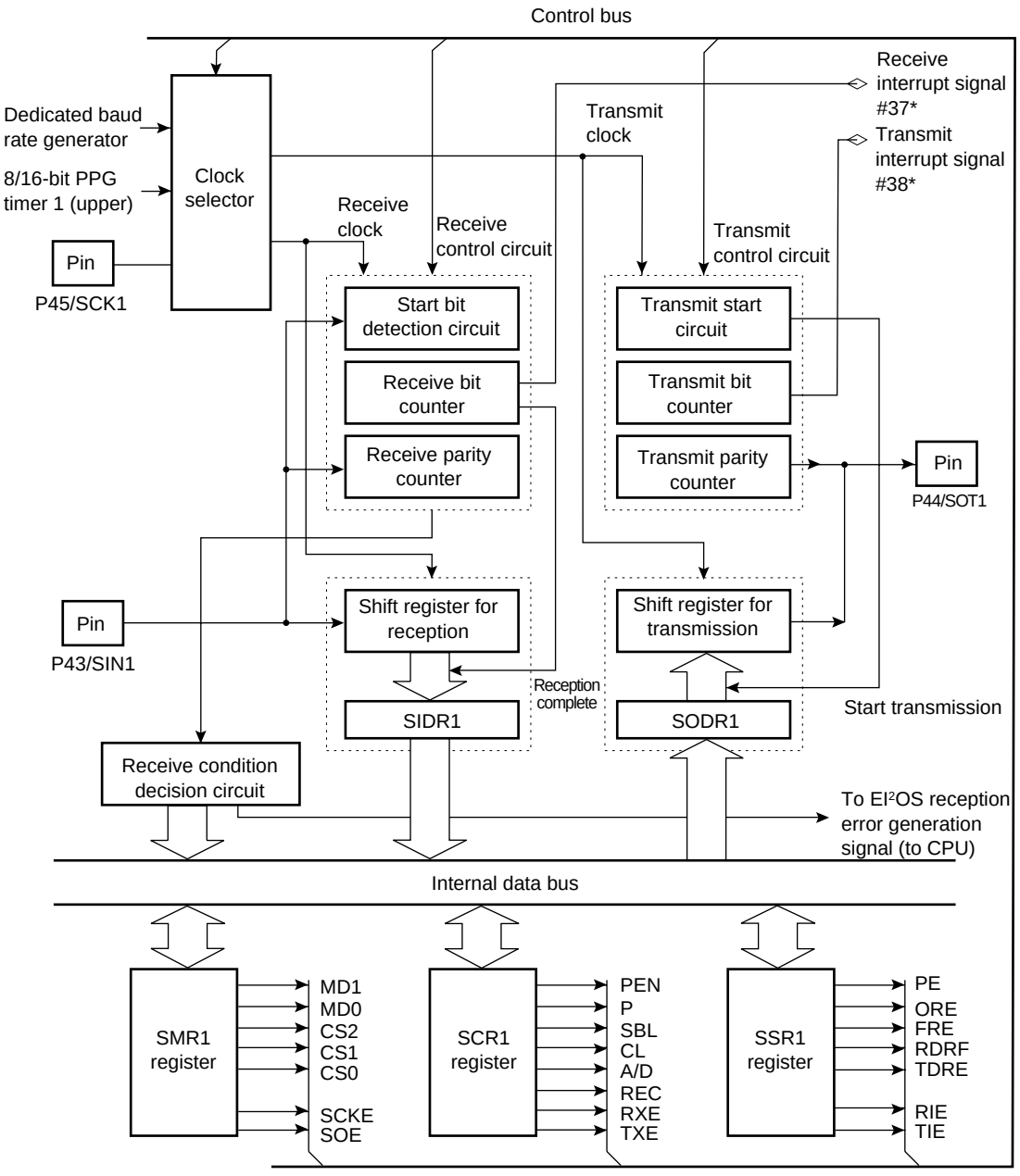
### (2) Block Diagram

- **UART0 (SCI)**




*: Interrupt number

- **UART1 (SCI)**




*: Interrupt number

## 10. DTP/External Interrupt Circuit

DTP (Data Transfer Peripheral), which is located between the peripheral circuit outside the device and the F²MC-16LX CPU, receives an interrupt request or DMA request generated by the external peripheral circuit* for transmission to the F²MC-16LX CPU. DTP is used to activate the intelligent I/O service or interrupt processing. As request levels for IRQ2 to IRQ7, two types of “H” and “L” can be selected for the intelligent I/O service. Rising and falling edges as well as “H” and “L” can be selected for an external interrupt request. For IRQ0 and IRQ1, a request by a level cannot be entered, but both edges can be entered.

* : The external peripheral circuit is connected outside the MB90570/A series device.

Note : IRQ0 and IRQ1 cannot be used for the intelligent I/O service and return from an interrupt.



### (1) Register Configuration

- DTP/interrupt factor register (EIRR)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 · · · · · · · · · · · · bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000031H | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | (ENIR) | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- DTP/interrupt enable register (ENIR)

| Address | bit 15 · · · · · · · · · · · · bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000030H | (EIRR) | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

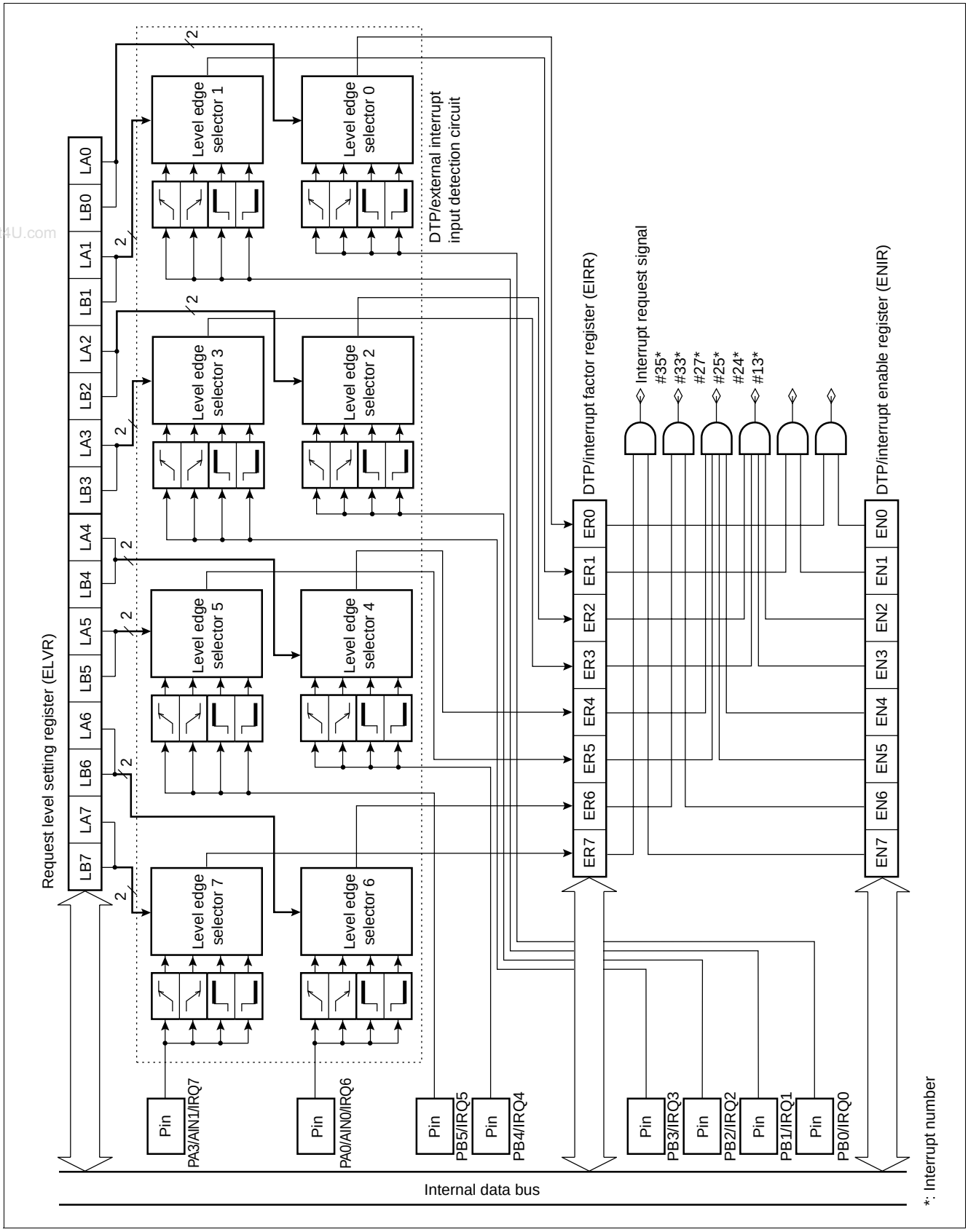
- Request level setting register (ELVR)

| Address | bit 15 · · · · · · · · · · · · bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| Low order address 000032H | (ELVR upper) | LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 · · · · · · · · · · · · bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| High order address 000033H | LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 | (ELVR lower) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

R/W:Readable and writable
X:Undefined

### (2) Block Diagram



## 11. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks for development on a real-time operating system (REALOS series). The module can be used to generate softwarewise generates hardware interrupt requests to the CPU and cancel the interrupts.

This module does not conform to the extended intelligent I/O service (EI$^2$OS).

### (1) Register Configuration



• Delayed interrupt factor generation/cancellation register (DIRR)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00009F$_H$ | — | — | — | — | — | — | — | R0 | (PACSR) | - - - - - - - 0$_B$ |
| | — | — | — | — | — | — | — | R/W | | |

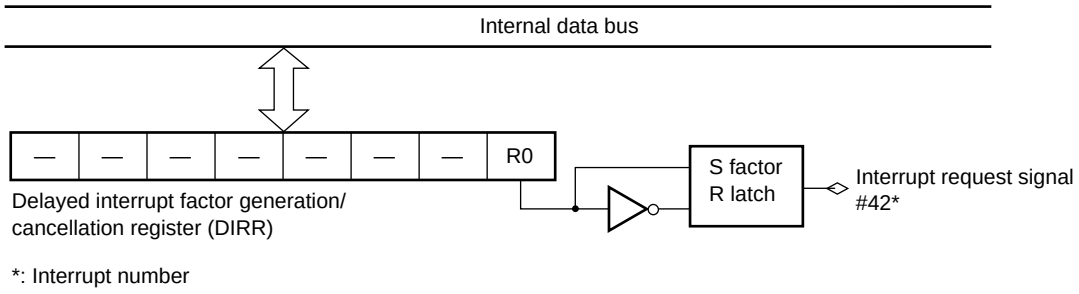
Note: Upon a reset, an interrupt is canceled.

R/W:Readable and writable

—:Reserved

The DIRR is the register used to control delay interrupt request generation/cancellation. Programming this register with “1” generates a delay interrupt request. Programming this register with “0” cancels a delay interrupt request. Upon a reset, an interrupt is canceled. The reserved bit area can be programmed with either “0” or “1”. For future extension, however, it is recommended that bit set and clear instructions be used to access this register.

### (2) Block Diagram




*: Interrupt number

## 12. 8/10-bit A/D Converter

The 8/10-bit A/D converter has a function of converting analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features.

- Minimum conversion time: 26.3 μs (at machine clock of 16 MHz, including sampling time)
- Minimum sampling time: 4 μs/256 μs (at machine clock of 16 MHz)
- Compare time: 176/352 machine cycles per channel (176 machine cycles are used for a machine clock below 8 MHz.)
- Conversion method: RC successive approximation method with a sample and hold circuit.
- 8-bit or 10-bit resolution
- Analog input pins: Selectable from eight channels by software
  Single conversion mode: Selects and converts one channel.
  Scan conversion mode:Converts two or more successive channels. Up to eight channels can be programmed.
  Continuous conversion mode: Repeatedly converts specified channels.
  Stop conversion mode:Stops conversion after completing a conversion for one channel and wait for the next activation (conversion can be started synchronously.)
- Interrupt requests can be generated and the extended intelligent I/O service (EI$^2$OS) can be started after the end of A/D conversion. Furthermore, A/D conversion result data can be transferred to the memory, enabling efficient continuous processing.
- When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
- Starting factors for conversion: Selected from software activation, and external trigger (falling edge).

### (1) Register Configuration

- A/D control status register upper digits (ADCS2)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000037H | BUSY | INT | INTE | PAUS | STS1 | STS0 | STRT | RESV | (ADCS1) | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | W | R/W | | |

- A/D control status register lower digits (ADCS1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000036H | (ADCS2) | MD1 | MD0 | ANS2 | ANS1 | ANS0 | ANE2 | ANE1 | ANE0 | 00000000B |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



- A/D data register upper digits (ADCR2)

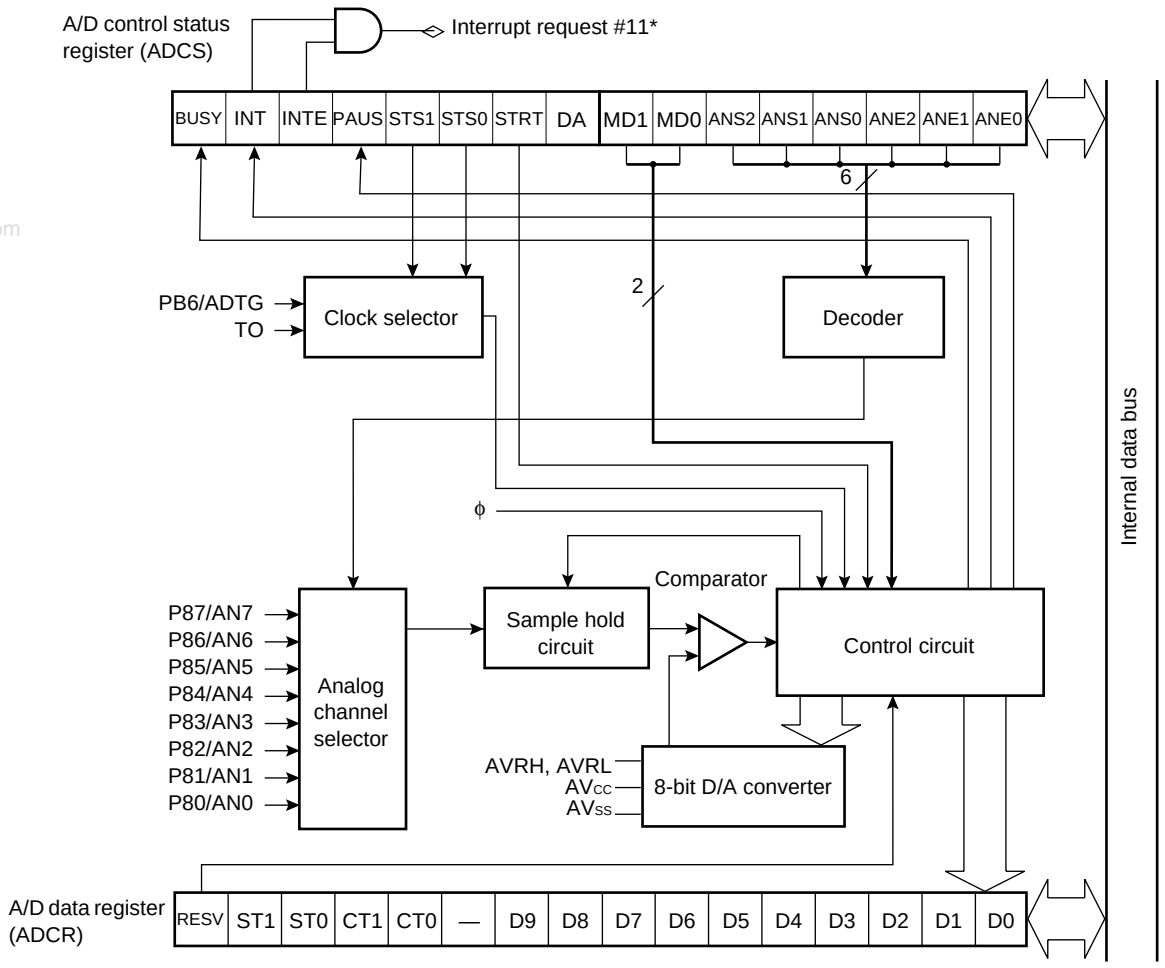
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000039H | DSEL | ST1 | ST0 | CT1 | XCT0 | — | D9 | D8 | (ADCR1) | 00001-XXB |
| | W | W | W | W | W | — | — | — | | |

- A/D data register lower digits (ADCR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000038H | (ADCR2) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| | | R | R | R | R | R | R | R | R | |

R/W :Readable and writable
R :Read only
W :Write only
— :Reserved
X :Undefined
RESV: Reserved bit

### (2) Block Diagram




ϕ:Machine clock frequency

TO:8/16-bit PPG timer channel 1 output

*:Interrupt number

## 13. 8-bit D/A Converter

The 8-bit D/A converter, which is based on the R-2R system, supports 8-bit resolution mode. It contains two channels each of which can be controlled in terms of output by the D/A control register.

### (1) Register Configuration

- D/A converter data register ch.0 (DADR0)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00003A$_H$ | (DADR1) | DA07 | DA06 | DA05 | DA04 | DA03 | DA02 | DA01 | DA00 | XXXXXXXX$_B$ |
| | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |



- D/A converter data register ch.1 (DADR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00003B$_H$ | DA17 | DA16 | DA15 | DA14 | DA13 | DA12 | DA11 | DA10 | (DADR0) | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

- D/A control register 0 (DACR0)

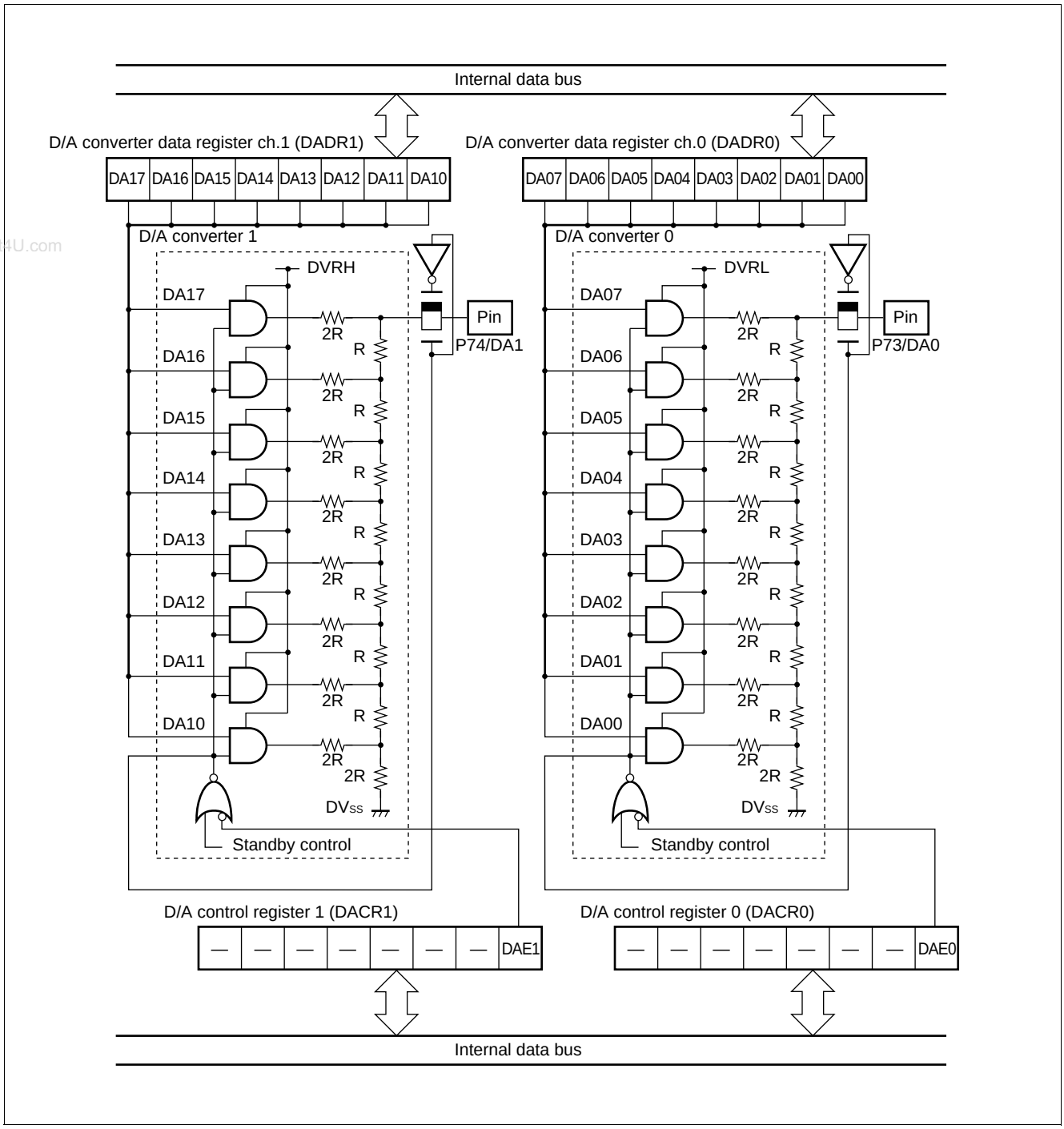
| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00003C$_H$ | (DACR1) | — | — | — | — | — | — | — | DAE0 | - - - - - - - 0$_B$ |
| | | — | — | — | — | — | — | — | R/W | |

- D/A control register 1 (DACR1)

| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00003D$_H$ | — | — | — | — | — | — | — | DAE1 | (DACR0) | - - - - - - - 0$_B$ |
| | — | — | — | — | — | — | — | R/W | | |

R/W:Readable and writable
—:Reserved
X:Undefined

**(2) Block Diagram**



## 14. Clock Timer

The clock timer control register (WTC) controls operation of the clock timer, and time for an interval interrupt.

### (1) Register Configuration

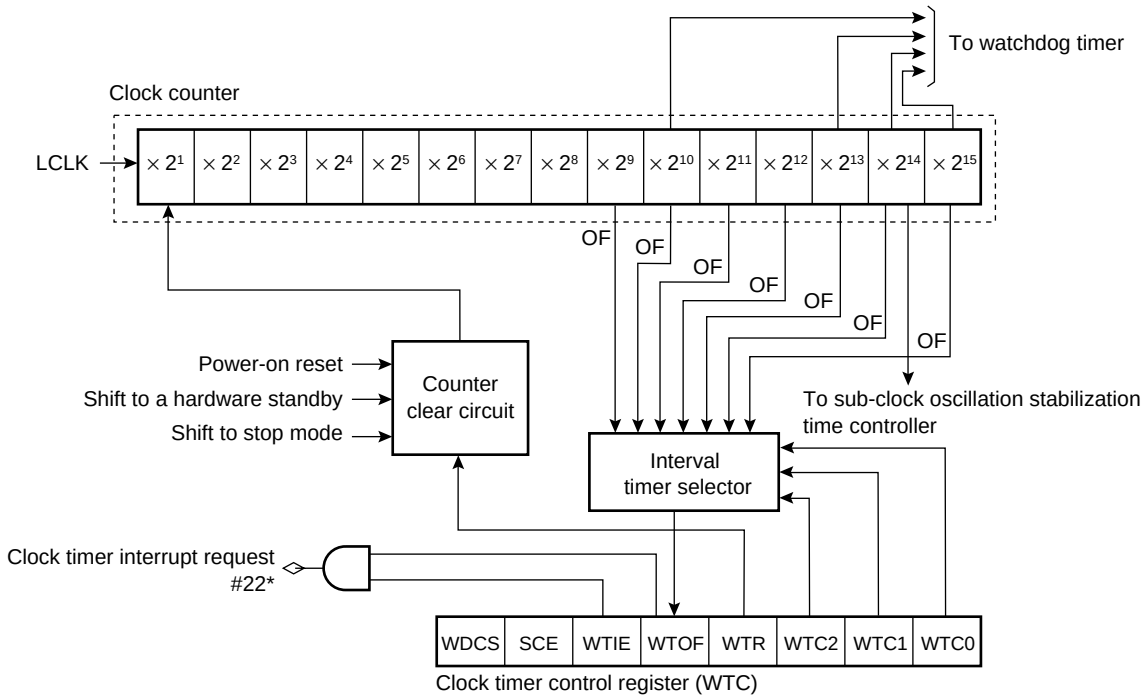
- Clock timer control register (WTC)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 0000AA$_H$ | (Disabled) | WDCS | SCE | WTIE | WTOF | WTR | WTC2 | WTC1 | WTC0 | 1X000000$_B$ |
| | | R/W | R | R/W | R/W | R/W | R | R/W | R/W | |



R/W:Readable and writable
R:Read only
X:Undefined

### (2) Block Diagram




*:Interrupt number
OF:Overflow
LCLK:Oscillation sub-clock frequency

## 15. Chip Select Output

This module generates a chip select signal for facilitating a memory and I/O unit, and is provided with eight chip select output pins. When access to an address is detected with a hardware-set area set for each pin register, a select signal is output from the pin.

### (1) Register Configuration

- Chip selection control register 1, 3, 5, 7 (CSCR1, CSCR3, CSCR5, CSCR7)

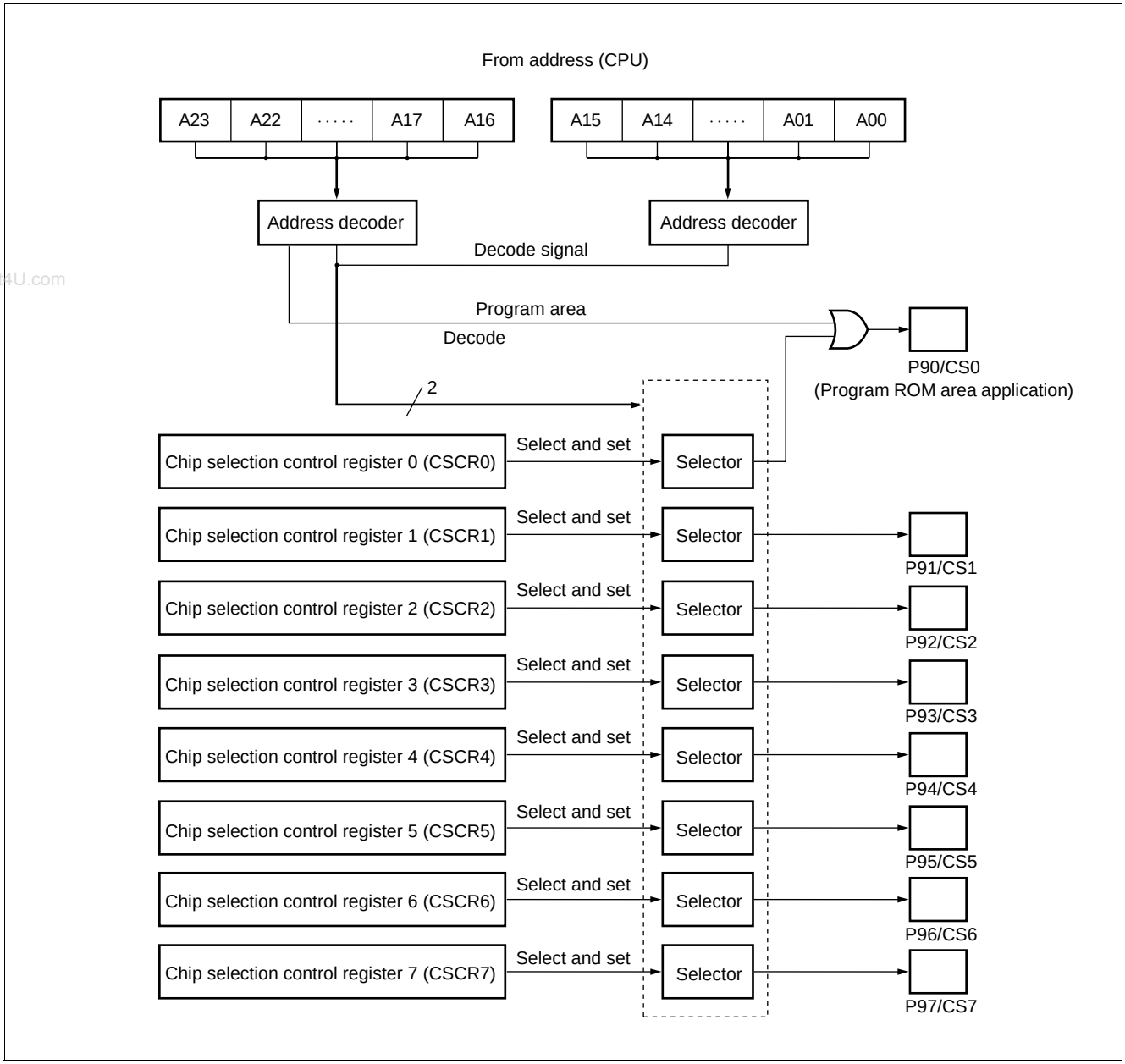
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| CSCR1: 000081H<br>CSCR3: 000083H<br>CSCR5: 000085H<br>CSCR7: 000087H | — | — | — | — | ACTL | OPEL | CSA1 | CSA0 | (CSCR0, CSCR2, CSCR4, CSCR6) | - - - - 0000B |
| | — | — | — | — | R/W | R/W | R/W | R/W | | |

- Chip selection control register 0, 2, 4, 6 (CSCR0, CSCR2, CSCR4, CSCR6)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| CSCR0: 000080H<br>CSCR2: 000082H<br>CSCR4: 000084H<br>CSCR6: 000086H | (CSCR1, CSCR3, CSCR5, CSCR7) | — | — | — | — | ACTL | OPEL | CSA1 | CSA0 | - - - - 0000B |
| | | — | — | — | — | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
—:Reserved

**(2) Block Diagram**



**(3) Decode Address Spaces**

| Pin name | CSA | | Decode space | Number of area bytes | Remarks |
|---|---|---|---|---|---|
| | 1 | 0 | | | |
| CS0 | 0 | 0 | F00000H to FFFFFFH | 1 Mbyte | Becomes active when the program ROM area or the program vector is fetched. |
| | 0 | 1 | F80000H to FFFFFFH | 512 kbyte | |
| | 1 | 0 | FE0000H to FFFFFFH | 128 kbyte | |
| | 1 | 1 | — | Disabled | |
| CS1 | 0 | 0 | E00000H to EFFFFFH | 1 Mbyte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | F00000H to F7FFFFH | 512 kbyte | |
| | 1 | 0 | FC0000H to FDFFFFH | 128 kbyte | |
| | 1 | 1 | 68FF80H to 68FFFFH | 128 byte | |
| CS2 | 0 | 0 | 003000H to 003FFFH | 4 kbyte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | FA0000H to FBFFFFH | 128 kbyte | |
| | 1 | 0 | 68FF80H to 68FFFFH | 128 byte | |
| | 1 | 1 | 68FF00H to 68FF7FH | 128 byte | |
| CS3 | 0 | 0 | F80000H to F9FFFFH | 128 kbyte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | 68FF00H to 68FF7FH | 128 byte | |
| | 1 | 0 | 68FE80H to 68FEFFH | 128 byte | |
| | 1 | 1 | — | Disabled | |
| CS4 | 0 | 0 | 002800H to 002FFFH | 2 kbyte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | 68FE80H to 68FEFFH | 128 byte | |
| | 1 | 0 | — | Disabled | |
| | 1 | 1 | — | Disabled | |
| CS5 | 0 | 0 | 68FF80H to 68FFFFH | 128 byte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | — | Disabled | |
| | 1 | 0 | — | Disabled | |
| | 1 | 1 | — | Disabled | |
| CS6 | 0 | 0 | 68FF00H to 68FF7FH | 128 byte | Adapted to the data ROM and RAM areas, and external circuit connection applications. |
| | 0 | 1 | — | Disabled | |
| | 1 | 0 | — | Disabled | |
| | 1 | 1 | — | Disabled | |
| CS7 | — | — | — | Disabled | Disabled |

## 16. Communications Prescaler Register

This register controls machine clock division.

Output from the communications prescaler register is used for UART0 (SCI), UART1 (SCI), and extended I/O serial interface.

The communications prescaler register is so designed that a constant baud rate may be acquired for various machine clocks.

### (1) Register Configuration



- Communications prescaler control register 0,1 (CDCR0, CDCR1)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 000028H<br>00002AH | (Disabled) | MD | — | — | — | DIV3 | DIV2 | DIV1 | DIV0 | 0 - - - 1111B |
| | | R/W | — | — | — | R/W | R/W | R/W | R/W | |

R/W:Readable and writable
—:Reserved

## 17. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at “1”, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

### (1) Register Configuration



- Program address detection register 0 to 2 (PADR0)

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR0 (Low order address): 001FF0H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR0 (Middle order address): 001FF1H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR0 (High order address): 001FF2H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Program address detection register 3 to 5 (PADR1)

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR1 (Low order address): 001FF3H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR1 (Middle order address): 001FF4H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

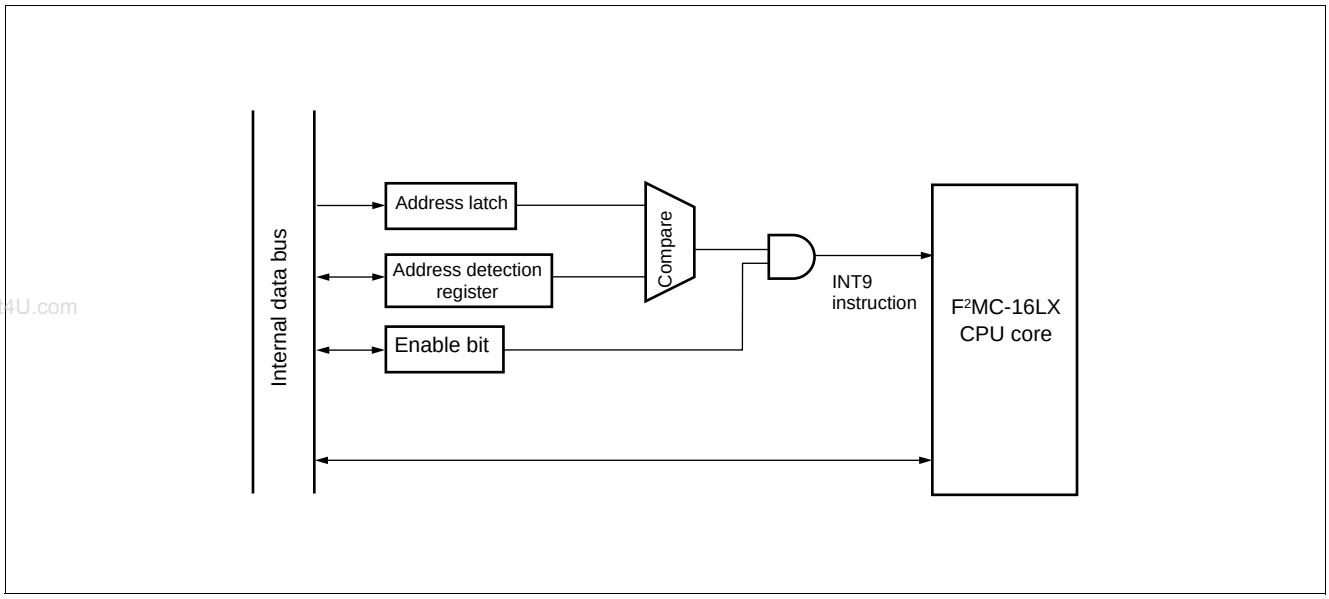
| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| PADR1 (High order address): 001FF5H | | | | | | | | | XXXXXXXXB |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

- Program address detection control status register (PACSR)

| Address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|
| 00009EH | RESV | RESV | RESV | RESV | AD1E | RESV | AD0E | RESV | 00000000B |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |

R/W :Readable and writable
X :Undefined
RESV:Reserved bit

**(2) Block Diagram**



## 18. ROM Mirroring Function Selection Module

The ROM mirroring function selection module can select what the FF bank allocated the ROM sees through the 00 bank according to register settings.

### (1) Register Configuration

- ROM mirroring function selection register (ROMM)

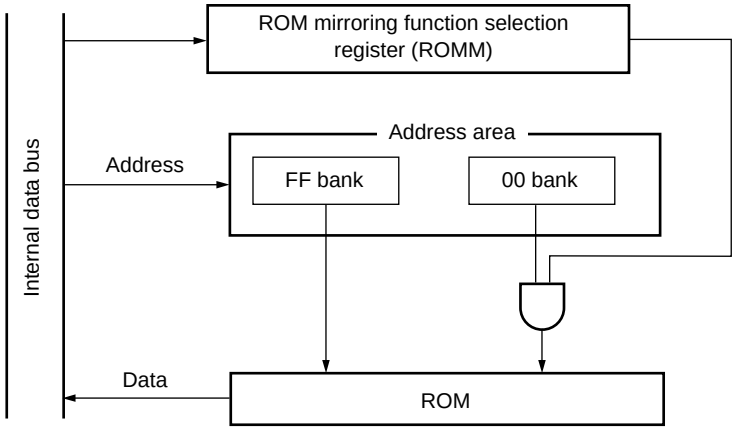
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 00006F$_H$ | — | — | — | — | — | — | — | MI | (Disabled) | - - - - - - - 1$_B$ |
| | — | — | — | — | — | — | — | W | | |

W:Write only
—:Reserved



Note : Do not access this register during operation at addresses 004000$_H$ to 00FFFF$_H$.

### (2) Block Diagram



## 19. Low-power Consumption (Standby) Mode

The F²MC-16LX has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- **Clock mode**

  PLL clock mode: A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock (HCLK).

  Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscil lation clock (HCLK).
  The PLL multiplication circuits stops in the main clock mode.



- **CPU intermittent operation mode**

  The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high-speed.

- **Hardware standby mode**

  The hardware standby mode is a mode for reducing power consumption by stopping clock supply to the CPU by the low-power consumption control circuit, stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware standby mode). Of these modes, modes other than the PLL clock mode are power consumption modes.

### (1) Register Configuration

- Clock select register (CKSCR)

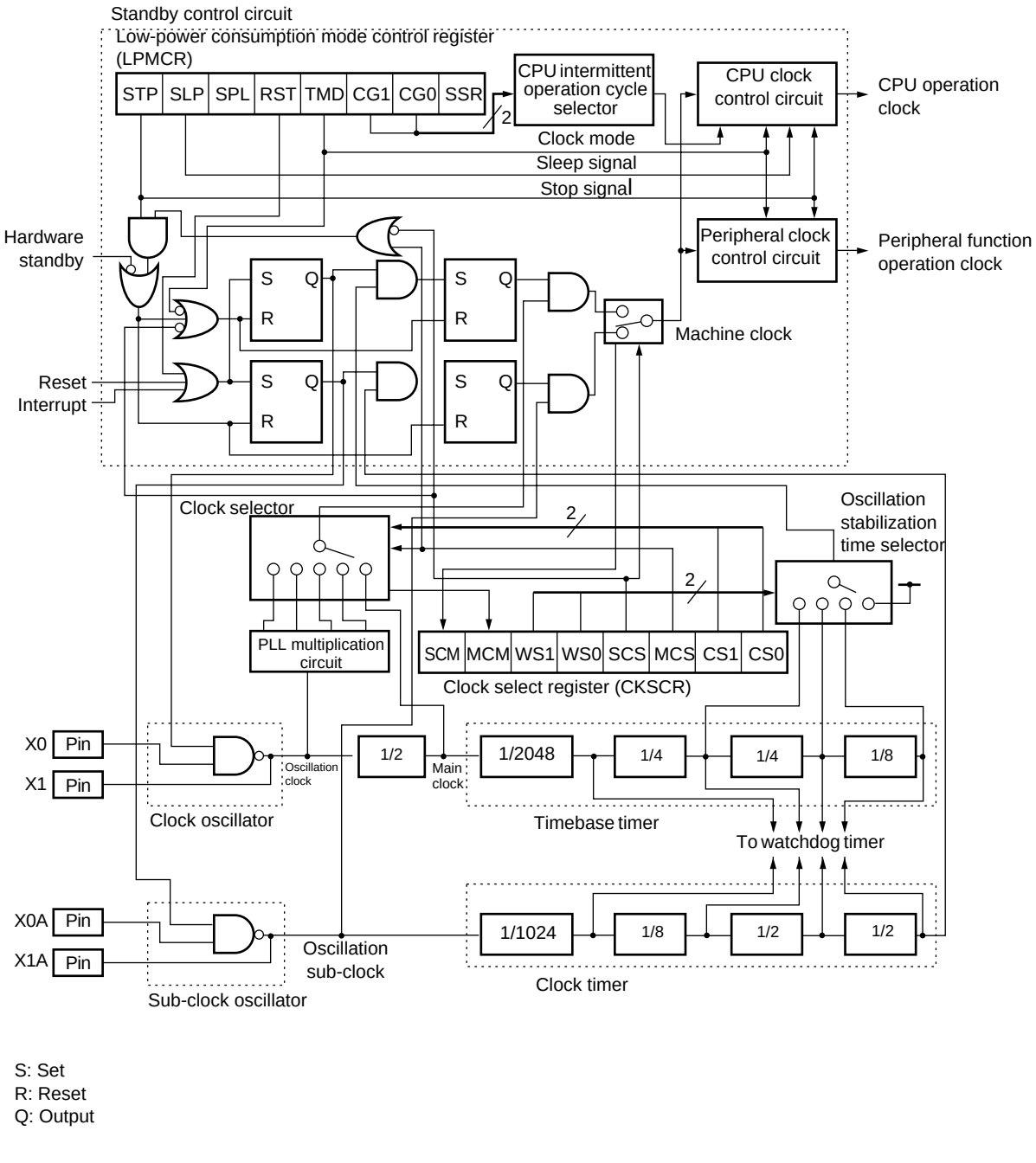
| Address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 | bit 7 ····· bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 0000A1H | SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 | (LPMCR) | 11111100B |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W | | |

- Low-power consumption mode control register (LPMCR)

| Address | bit 15 ····· bit 8 | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| 0000A0H | (CKSCR) | STP | SLP | SPL | RST | TMD | CG1 | CG0 | SSR | 00011000B |
| | | W | W | R/W | W | R/W | W | R/W | R/W | |

R/W: Readable and writable
R: Read only
W: Write only

### (2) Block Diagram



## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *1 |
| | AVRH, AVRL | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *1 |
| | DVRH | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *1 |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *3 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *4 |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *5 |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | *3 |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | *4 |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | –100 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | –50 | mA | *5 |
| Power consumption | $P_D$ | — | 300 | mW | MB90573/4 MB90V570/A |
| | | — | 500 | mW | MB90574C |
| | | — | 800 | mW | MB90F574/A |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | Tstg | –55 | +150 | °C | |

*1 : Care must be taken that $AV_{CC}$, AVRH, AVRL, and DVRH do not exceed $V_{CC}$. Also, care must be taken that AVRH and AVRL do not exceed $AV_{CC}$, and AVRL does not exceed AVRH.

*2 : $V_I$ and $V_O$ shall never exceed $V_{CC}$ + 0.3 V.

*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note : Average output current = operating × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | 3.0 | 5.5 | V | Normal operation (MB90574/C) |
| | $V_{CC}$ | 4.5 | 5.5 | V | Normal operation (MB90F574/A) |
| | $V_{CC}$ | 3.0 | 5.5 | V | Retains status at the time of operation stop |
| Smoothing capacitor | $C_S$ | 0.1 | 1.0 | µF | * |
| Operating temperature | $T_A$ | –40 | +85 | °C | |



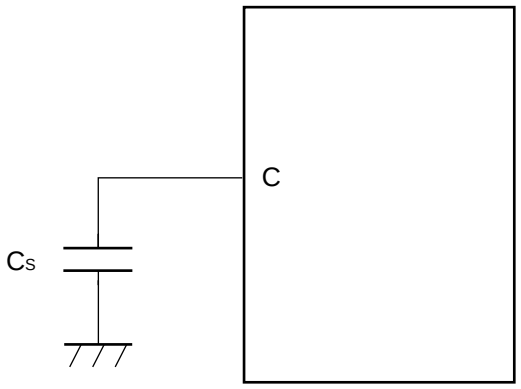
* : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the $V_{CC}$ pin must have a capacitance value higher than $C_S$.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

• **C pin connection circuit**



### 3. DC Characteristics

($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHS}$ | CMOS hysteresis input pin | $V_{CC}$ = 3.0 V to 5.5 V (MB90573) (MB90574) $V_{CC}$ = 4.5 V to 5.5 V (MB90F574) | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHM}$ | MD pin input | | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{ILS}$ | CMOS hysteresis input pin | | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| | $V_{ILM}$ | MD pin input | | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | |
| "H" level output voltage | $V_{OH}$ | Other than PA6 and PA7 | $V_{CC}$ = 4.5 V $I_{OH}$ = –2.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | All output pins | $V_{CC}$ = 4.5 V $I_{OL}$ = 2.0 mA | — | — | 0.4 | V | |
| Open-drain output leakage current | $I_{leak}$ | PA6, PA7 | — | — | 0.1 | 5 | µA | |
| Input leakage current | $I_{IL}$ | Other than PA6 and PA7 | $V_{CC}$ = 5.5 V $V_{SS}$ < $V_I$ < $V_{CC}$ | –5 | — | 5 | µA | |
| Pull-up resistance | $R_{UP}$ | P00 to P07, P10 to P17, P60 to P67, $\overline{RST}$, MD0, MD1 | — | 15 | 30 | 100 | kΩ | |
| Pull-down resistance | $R_{DOWN}$ | MD0 to MD2 | — | 15 | 30 | 100 | kΩ | |
| Power supply current | $I_{CC}$ | $V_{CC}$ | Internal operation at 16 MHz $V_{CC}$ at 5.0 V Normal operation | — | 30 | 40 | mA | MB90574 |
| | $I_{CC}$ | $V_{CC}$ | | — | 85 | 130 | mA | MB90F574/A |
| | $I_{CC}$ | $V_{CC}$ | | — | 50 | 80 | mA | MB90574C |
| | $I_{CC}$ | $V_{CC}$ | Internal operation at 16 MHz $V_{CC}$ at 5.0 V A/D converter operation | — | 35 | 45 | mA | MB90574 |
| | $I_{CC}$ | $V_{CC}$ | | — | 90 | 140 | mA | MB90F574/A |
| | $I_{CC}$ | $V_{CC}$ | | — | 55 | 85 | mA | MB90574C |
| | $I_{CC}$ | $V_{CC}$ | Internal operation at 16 MHz $V_{CC}$ at 5.0 V D/A converter operation | — | 40 | 50 | mA | MB90574 |
| | $I_{CC}$ | $V_{CC}$ | | — | 95 | 145 | mA | MB90F574/A |
| | $I_{CC}$ | $V_{CC}$ | | — | 65 | 85 | mA | MB90574C |

*(Continued)*

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CC}$ | $V_{CC}$ | When data written in flash mode programming of erasing | — | 95 | 140 | mA | MB90F574/A |
| | $I_{CCS}$ | $V_{CC}$ | Internal operation at 16 MHz $V_{CC}$ = 5.0 V In sleep mode | — | 7 | 12 | mA | MB90574 |
| | $I_{CCS}$ | $V_{CC}$ | | — | 5 | 10 | mA | MB90F574/A |
| | $I_{CCS}$ | $V_{CC}$ | | — | 15 | 20 | mA | MB90574C |
| | $I_{CCL}$ | $V_{CC}$ | Internal operation at 8 kHz $V_{CC}$ = 5.0 V $T_A$ = +25°C Subsystem operation | — | 0.1 | 1.0 | mA | MB90574 |
| | $I_{CCL}$ | $V_{CC}$ | | — | 4 | 7 | mA | MB90F574/A |
| | $I_{CCL}$ | $V_{CC}$ | | — | 0.03 | 1 | mA | MB90574C |
| | $I_{CCLS}$ | $V_{CC}$ | Internal operation at 8 kHz $V_{CC}$ = 5.0 V $T_A$ = +25°C In subsleep mode | — | 30 | 50 | µA | MB90574 |
| | $I_{CCLS}$ | $V_{CC}$ | | — | 0.1 | 1 | mA | MB90F574/A |
| | $I_{CCLS}$ | $V_{CC}$ | | — | 10 | 50 | µA | MB90574C |
| | $I_{CCT}$ | $V_{CC}$ | Internal operation at 8 kHz $V_{CC}$ = 5.0 V $T_A$ = +25°C In clock mode | — | 15 | 30 | µA | MB90574 |
| | $I_{CCT}$ | $V_{CC}$ | | — | 30 | 50 | µA | MB90F574/A |
| | $I_{CCT}$ | $V_{CC}$ | | — | 1.0 | 30 | µA | MB90574C |
| | $I_{CCH}$ | $V_{CC}$ | $T_A$ = +25°C In stop mode | — | 5 | 20 | µA | MB90574 |
| | $I_{CCH}$ | $V_{CC}$ | | — | 0.1 | 10 | µA | MB90F574/A MB90574C |
| Input capacitance | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, $V_{CC}$, $V_{SS}$ | — | — | 10 | 80 | pF | |

## 4. AC Characteristics

### (1) Reset, Hardware Standby Input Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

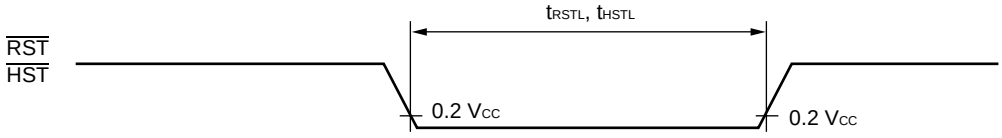
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 4 $t_{CP}$ | — | ns | Under normal operation |
| | | | | Oscillation time of oscillator * + 4 $t_{CP}$ | — | ms | In stop mode |
| Hardware standby input time | $t_{HSTL}$ | $\overline{HST}$ | | 4 $t_{CP}$ | — | ns | |



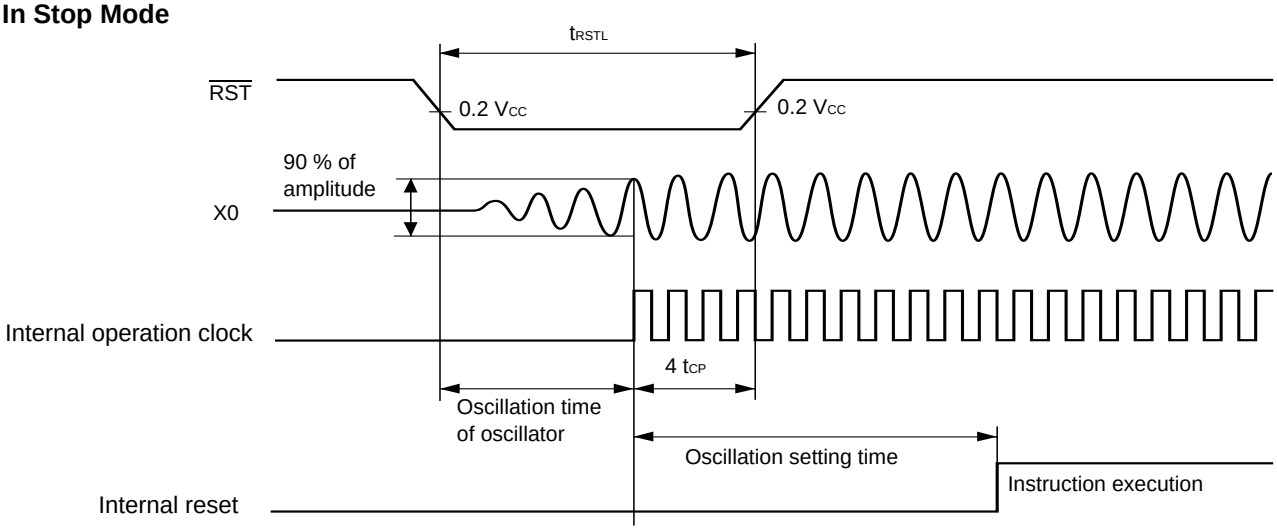
* : Oscillation time of oscillator is time that the amplitude reached the 90 %.
In the crystal oscillator, the oscillation time is between several ms to tens ms. In FAR/ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

Note : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

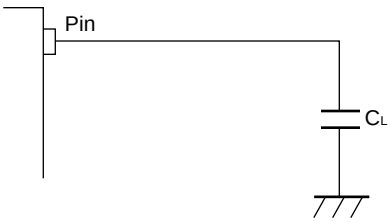
**Under Normal operation**




**In Stop Mode**




- **Measurement conditions for AC characteristics**




$C_L$ is a load capacitance connected to a pin under test.

Capacitors of $C_L$ = 30 pF must be connected to CLK and ALE pins, while $C_L$ of 80 pF must be connected to address data bus (AD15 to AD00), $\overline{RD}$, $\overline{WRL}$, and $\overline{WRH}$ pins.

### (2) Specification for Power-on Reset

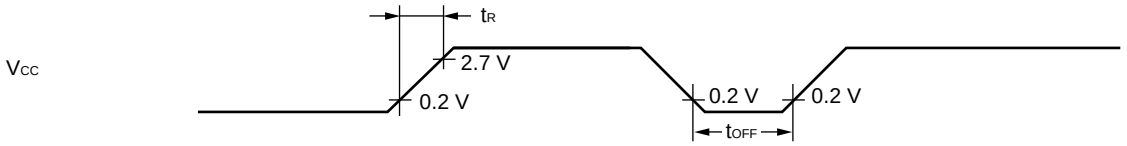
($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | * |
| Power supply cut-off time | $t_{OFF}$ | $V_{CC}$ | | 4 | — | ms | Due to repeated operations |

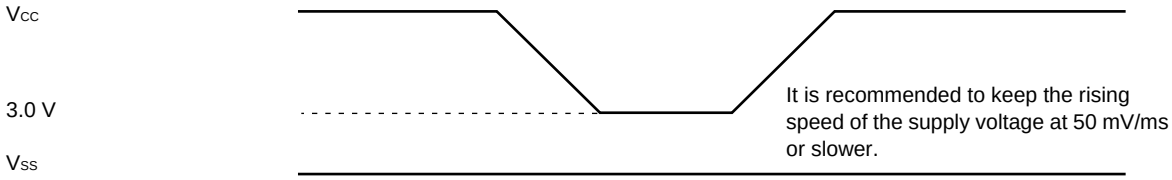
* : $V_{CC}$ must be kept lower than 0.2 V before power-on.



Note : • The above ratings are values for causing a power-on reset.
• There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.




Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V/s or fewer per second, however, you can use the PLL clock.



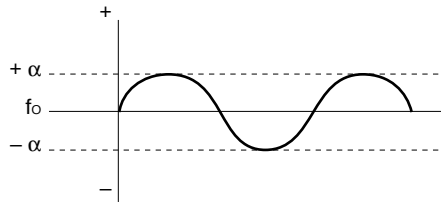
### (3) Clock Timings

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_C$ | X0, X1 | | 3 | — | 16 | MHz | |
| | $F_{CL}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | | 62.5 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | | 10 | — | — | ns | Recommend duty ratio of 30% to 70% |
| | $P_{WLH}$, $P_{WLL}$ | X0A | | — | 15.2 | — | µs | |
| Input clock rising/falling time | $t_{CR}$, $t_{CF}$ | X0, X0A | — | — | — | 5 | ns | External clock operation |
| Internal operating clock frequency | $f_{CP}$ | — | | 1.5 | — | 16 | MHz | Main clock operation |
| | $f_{LCP}$ | — | | — | 8.192 | — | kHz | Subclock operation |
| Internal operating clock cycle time | $t_{CP}$ | — | | 62.5 | — | 333 | ns | External clock operation |
| | $t_{LCP}$ | — | | — | 122.1 | — | µs | Subclock operation |
| Frequency fluctuation rate locked | $\Delta f$ | — | | — | — | 5 | % | * |

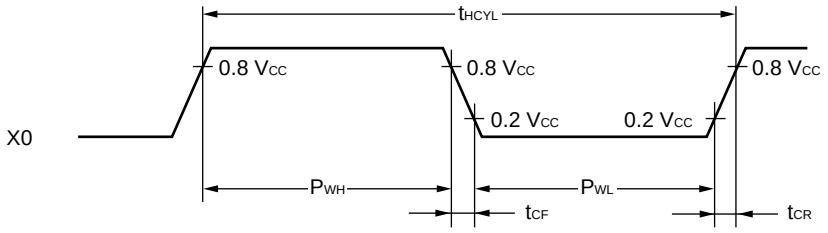
* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%)$$ Center frequency



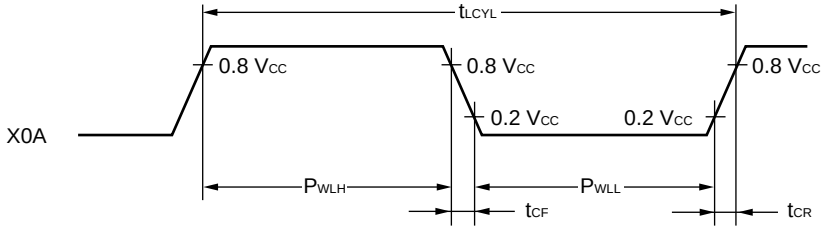

The PLL frequency deviation changes periodically from the preset frequency “(about CLK × (1CYC to 50 CYC)”, thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

- **X0, X1 clock timing**



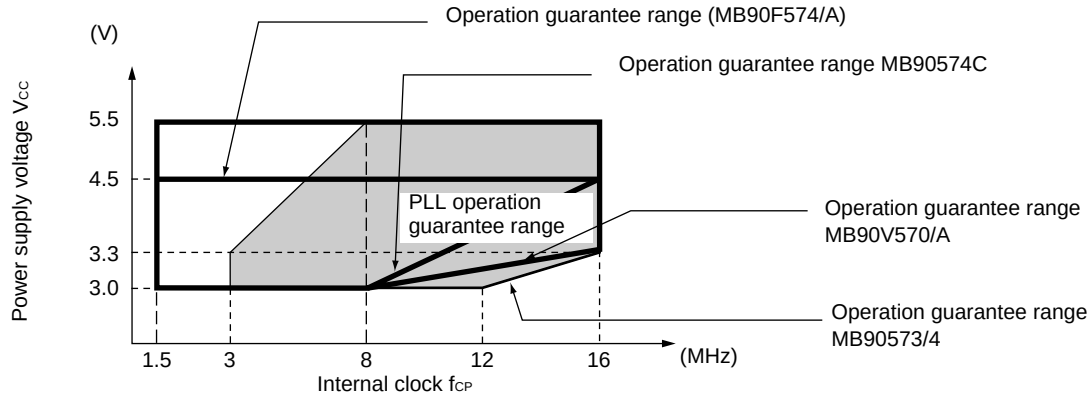



- **X0A, X1A clock timing**

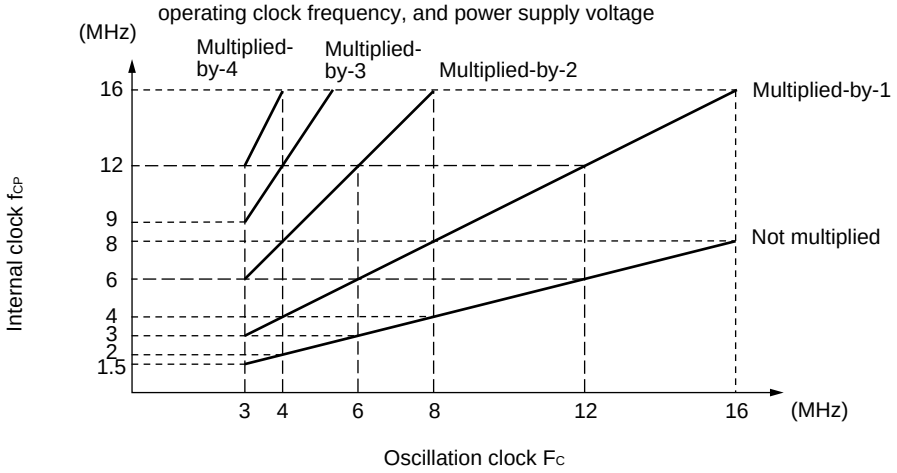



- **PLL operation guarantee range**

Relationship between internal operating clock frequency and power supply voltage



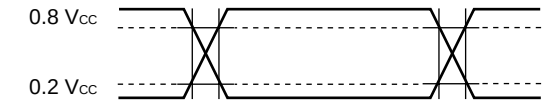

Relationship between oscillating frequency, internal operating clock frequency, and power supply voltage



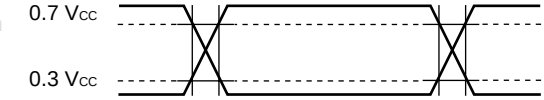
The AC ratings are measured for the following measurement reference voltages.

- **Input signal waveform**

Hystheresis input pin




Pins other than hystheresis input/MD input



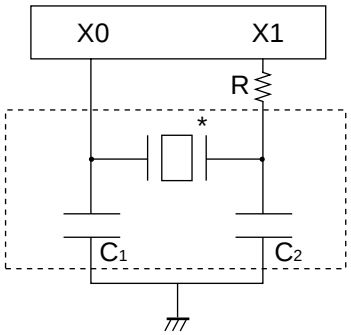

- **Output signal waveform**

Hystheresis input pin




**(4) Recommended Resonator Manufacturers**

**•Sample application of ceramic resonator**




- **Mask ROM product (MB90574)**

| Resonator manufacturer* | Resonator | Frequency (MHz) | $C_1$ (pF) | $C_1$ (pF) | R |
|---|---|---|---|---|---|
| Murata Mfg. Co., Ltd. | CSA2.00MG040 | 2.00 | 100 | 100 | No required |
| | CSA4.00MG040 | 4.00 | 100 | 100 | No required |
| | CSA8.00MTZ | 8.00 | 30 | 30 | No required |
| | CSA16.00MXZ040 | 16.00 | 15 | 15 | No required |
| | CSA32.00MXZ040 | 32.00 | 5 | 5 | No required |
| TDK Corporation | CCR3.52MC3 to CCR6.96MC3 | 3.52 to 6.96 | Built-in | Built-in | No required |
| | CCR7.0MC5 to CCR12.0MC5 | 7.00 to 12.00 | Built-in | Built-in | No required |
| | CCR20.0MSC6 to CCR32.0MSC6 | 20.00 to 32.00 | Built-in | Built-in | No required |

*(Continued)*

*(Continued)*

- **Flash product (MB90F574)**

| Resonator manufacturer* | Resonator | Frequency (MHz) | $C_1$ (pF) | $C_2$ (pF) | R |
|---|---|---|---|---|---|
| Murata Mfg. Co., Ltd. | CSA2.00MG040 | 2.00 | 100 | 100 | No required |
| | CSA4.00MG040 | 4.00 | 100 | 100 | No required |
| | CSA8.00MTZ | 8.00 | 30 | 30 | No required |
| | CSA16.00MXZ040 | 16.00 | 15 | 15 | No required |
| | CSA32.00MXZ040 | 32.00 | 5 | 5 | No required |
| TDK Corporation | CCR3.52MC3 to CCR6.96MC3 | 3.52 to 6.96 | Built-in | Built-in | No required |
| | CCR7.0MC5 to CCR12.0MC5 | 7.00 to 12.00 | Built-in | Built-in | No required |
| | CCR20.0MSC6 to CCR32.0MSC6 | 20.00 to 32.00 | Built-in | Built-in | No required |



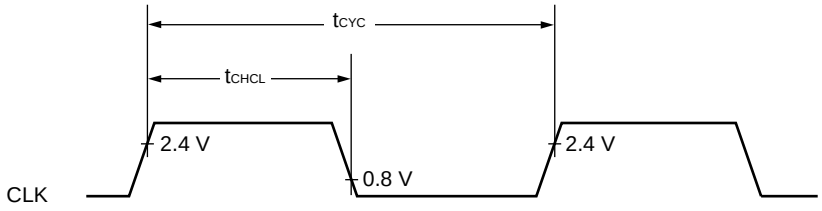
Inquiry: Murata Mfg. Co., Ltd.
- •Murata Electronics North America, Inc.: TEL 1-404-436-1300
- •Murata Europe Management GmbH: TEL 49-911-66870
- •Murata Electronics Singapore (Pte.): TEL 65-758-4233

TDK Corporation
- •TDK Corporation of America
  Chicago Regional Office: TEL 1-708-803-6100
- •TDK Electronics Europe GmbH
  Components Division: TEL 49-2102-9450
- •TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- •TDK Hongkong Co., Ltd.: TEL: 852-736-2238
- •Korea Branch, TDK Corporation: TEL 82-2-554-6636

**(5) Clock Output Timing**

($AV_{CC} = V_{CC} = 5.0$ V ±10%, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | CLK | — | 62.5 | — | ns | |
| CLK ↑ → CLK ↓ | $t_{CHCL}$ | CLK | | 20 | — | ns | |

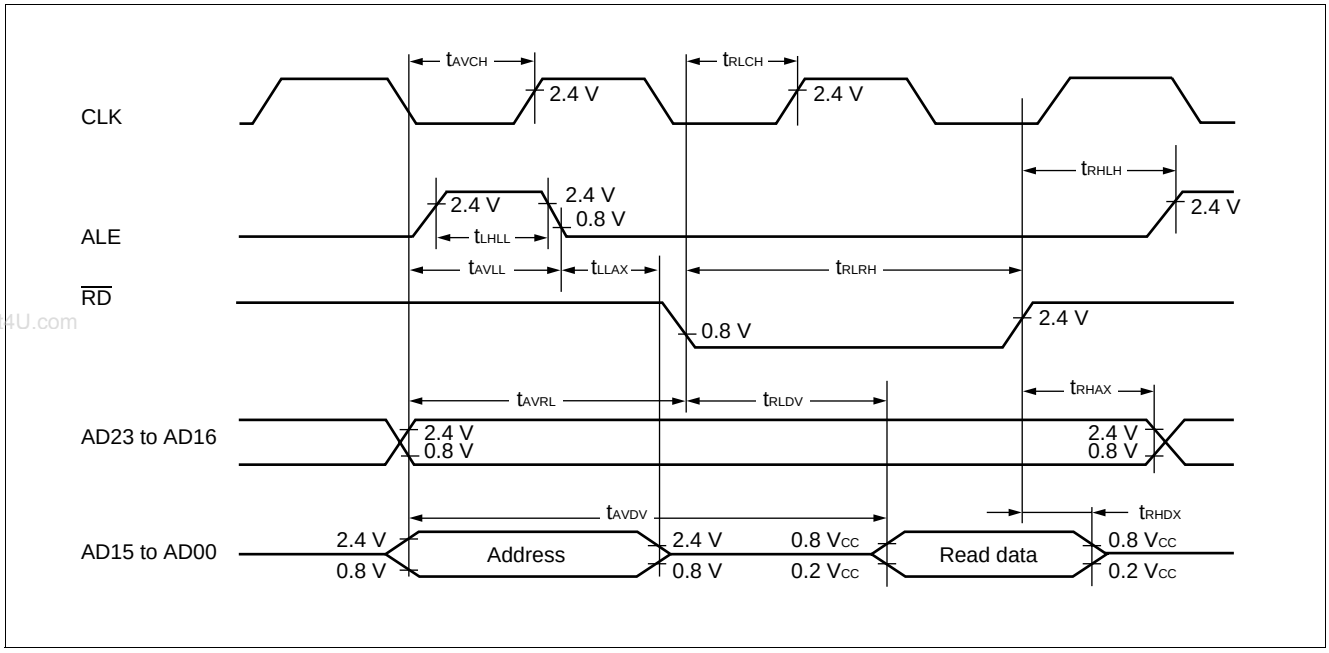


### (6) Bus Read Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | — | 1 $t_{CP}$*/2 – 20 | — | ns | |
| Effective address → ALE ↓ time | $t_{AVLL}$ | ALE, A23 to A16, AD15 to AD00 | | 1 $t_{CP}$*/2 – 20 | — | ns | |
| ALE ↓ → address effective time | $t_{LLAX}$ | ALE, AD15 to AD00 | | 1 $t_{CP}$*/2 – 15 | — | ns | |
| Effective address → $\overline{RD}$ ↓ time | $t_{AVRL}$ | $\overline{RD}$, A23 to A16, AD15 to AD00 | | 1 $t_{CP}$* – 15 | — | ns | |
| Effective address → valid data input | $t_{AVDV}$ | A23 to A16, AD15 to AD00 | | — | 5 $t_{CP}$*/2 – 60 | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | | 3 $t_{CP}$*/2 – 20 | — | ns | |
| $\overline{RD}$ ↓ → valid data input | $t_{RLDV}$ | $\overline{RD}$, AD15 to AD00 | | — | 3 $t_{CP}$*/2 – 60 | ns | |
| $\overline{RD}$ ↑ → data hold time | $t_{RHDX}$ | $\overline{RD}$, AD15 to AD00 | | 0 | — | ns | |
| $\overline{RD}$ ↑ → ALE ↑ time | $t_{RHLH}$ | ALE, $\overline{RD}$ | | 1 $t_{CP}$*/2 – 15 | — | ns | |
| $\overline{RD}$ ↑ → address effective time | $t_{RHAX}$ | ALE, A23 to A16 | | 1 $t_{CP}$*/2 – 10 | — | ns | |
| Effective address → CLK ↑ time | $t_{AVCH}$ | CLK, A23 to A16, AD15 to AD00 | | 1 $t_{CP}$*/2 – 20 | — | ns | |
| $\overline{RD}$ ↓ → CLK ↑ time | $t_{RLCH}$ | CLK, $\overline{RD}$ | | 1 $t_{CP}$*/2 – 20 | — | ns | |
| ALE ↓ → $\overline{RD}$ ↓ time | $t_{ALRL}$ | ALE, $\overline{RD}$ | | 1 $t_{CP}$*/2 – 15 | — | ns | |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

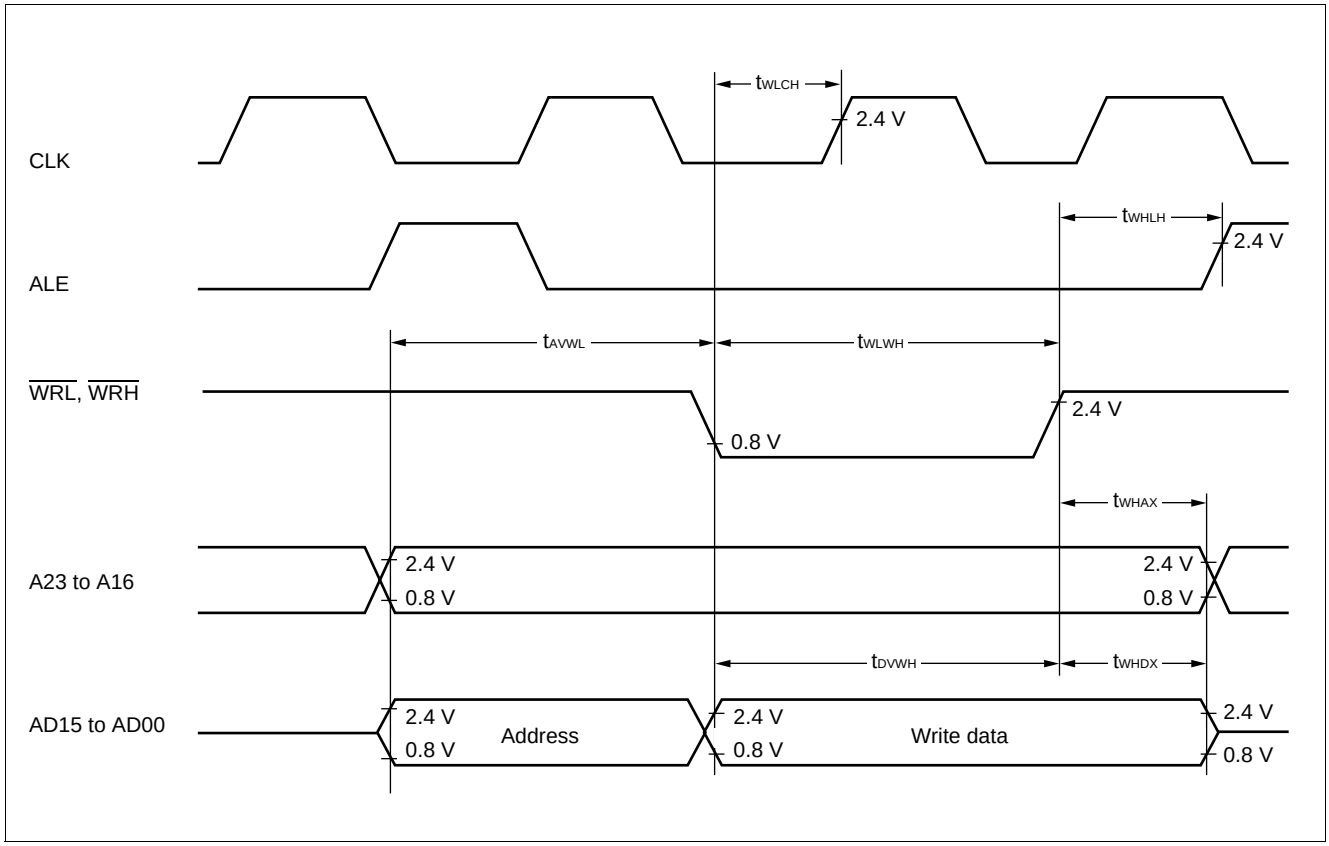


### (7) Bus Write Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Effective address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | $\overline{WRL}$, $\overline{WRH}$, A23 to A16, AD15 to AD00 | — | 1 $t_{CP}$ – 15 | — | ns | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WRL}$, $\overline{WRH}$ | | 3 $t_{CP}$*/2 – 20 | — | ns | |
| Write data → $\overline{WR}$ ↑ time | $t_{DVWH}$ | $\overline{WRL}$, $\overline{WRH}$, AD15 to AD00 | | 3 $t_{CP}$*/2 – 20 | — | ns | |
| $\overline{WR}$ ↑ → data hold time | $t_{WHDX}$ | $\overline{WRL}$, $\overline{WRH}$, AD15 to AD00 | | 20 | — | ns | |
| $\overline{WR}$ ↑ → address effective time | $t_{WHAX}$ | $\overline{WRL}$, $\overline{WRH}$, A23 to A16 | | 1 $t_{CP}$*/2 – 10 | — | ns | |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | ALE, $\overline{WRL}$ | | 1 $t_{CP}$*/2 – 15 | — | ns | |
| $\overline{WR}$ ↓ → CLK ↑ time | $t_{WLCH}$ | CLK, $\overline{WRH}$ | | 1 $t_{CP}$*/2 – 20 | — | ns | |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”



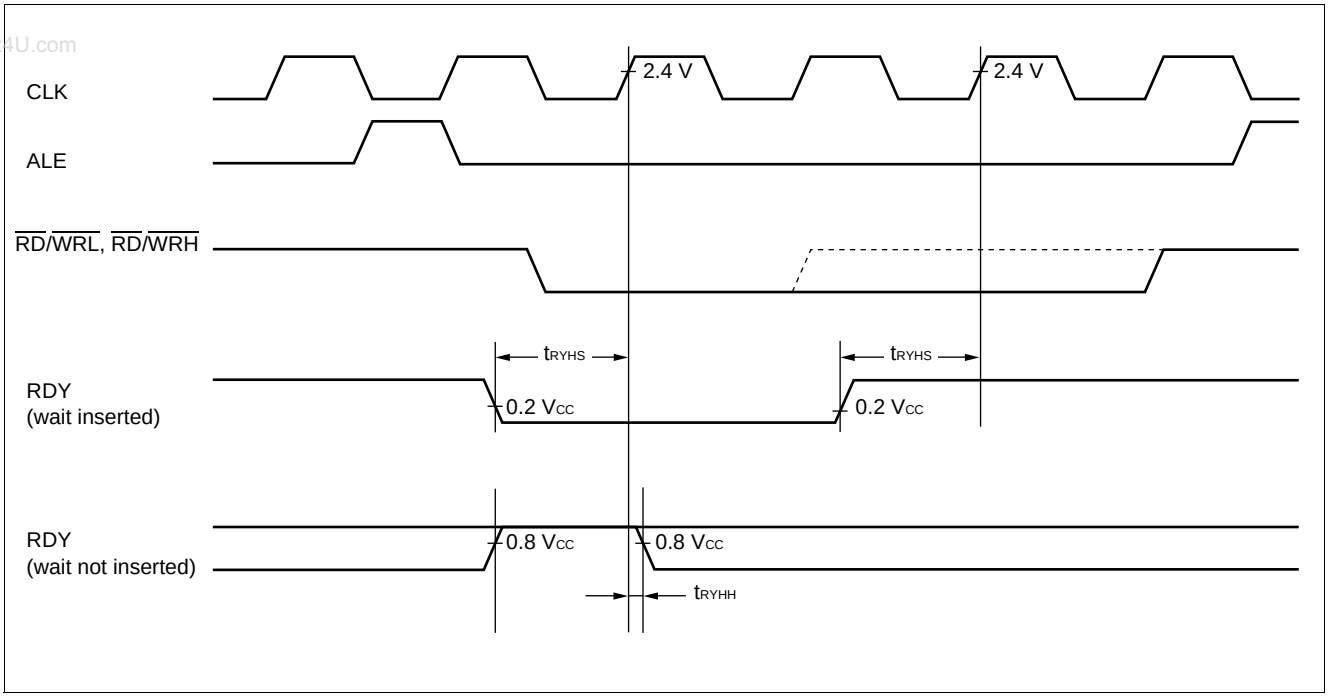
### (8) Ready Input Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note : Use the automatic ready function when the setup time for the rising edge of the RDY signal is not sufficient.





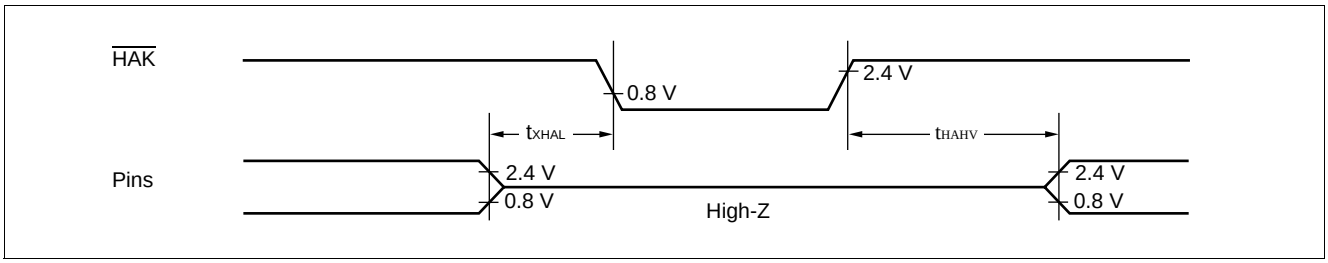

### (9) Hold Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Pins in floating status → $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | 1 $t_{CP}$* | ns | |
| $\overline{HAK}$ ↑ → pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | | 1 $t_{CP}$* | 2 $t_{CP}$* | ns | |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

Note : More than 1 machine cycle is needed before $\overline{HAK}$ changes after HRQ pin is fetched.



### (10) UART0 (SCI), UART1 (SCI) Timing

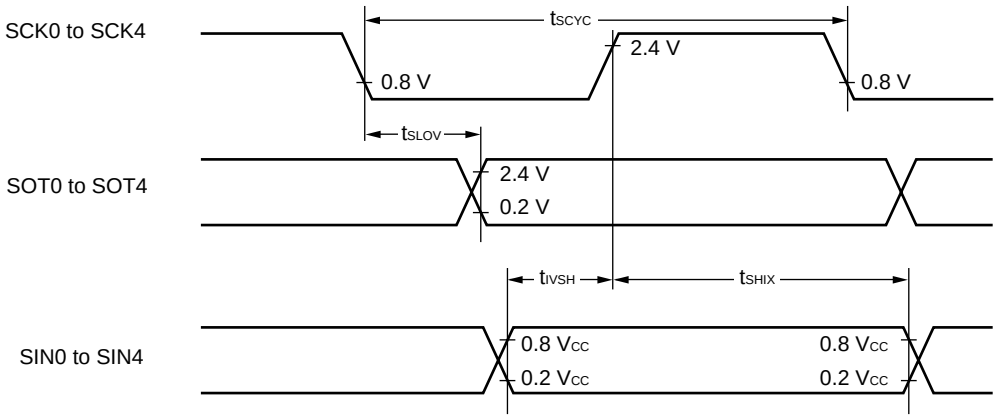
($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK4 | Internal shift clock mode<br>$C_L$ = 80 pF<br>+ 1 TTL for an output pin | 8 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK4, SOT0 to SOT4 | | – 80 | 80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK4, SIN0 to SIN4 | | 100 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0 to SCK4 | External shift clock mode<br>$C_L$ = 80 pF<br>+ 1 TTL for an output pin | 4 $t_{CP}$* | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK0 to SCK4 | | 4 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK4, SOT0 to SOT4 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |

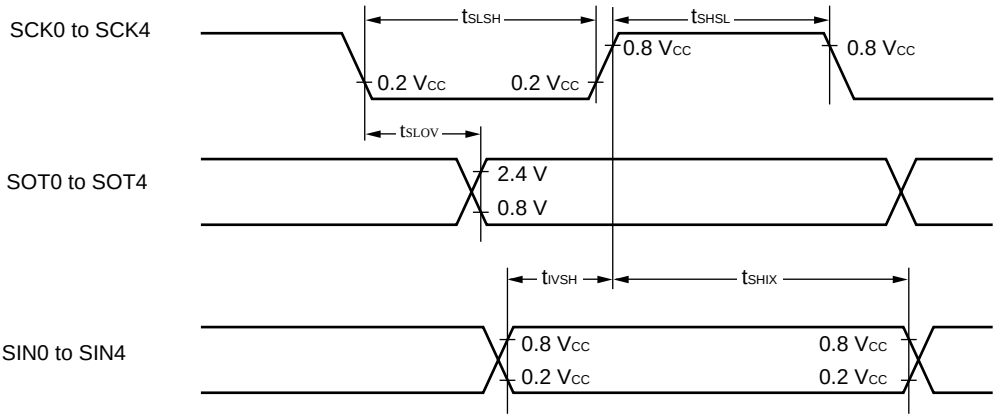
* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

Notes : • These are AC ratings in the CLK synchronous mode.
• $C_L$ is the load capacitance value connected to pins while testing.

- **Internal shift clock mode**




- **External shift clock mode**



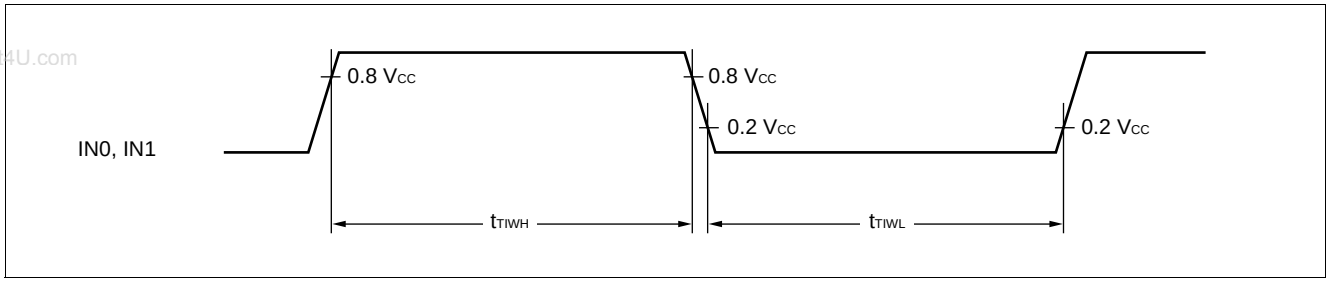
### (11) Timer Input Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$, $t_{TIWL}$ | IN0, IN1 | — | 4 $t_{CP}$* | — | ns | |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

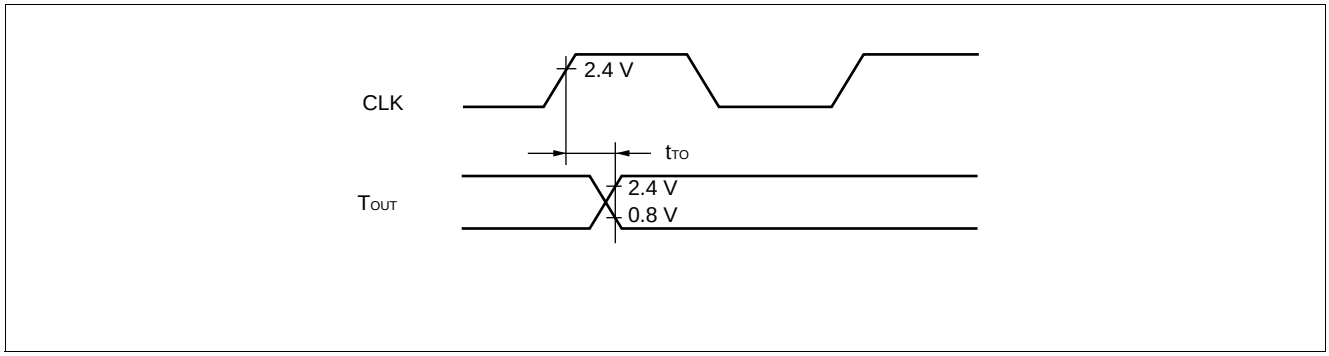





### (12) Timer Output Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK ↑ → $T_{OUT}$ transition time | $t_{TO}$ | OUT0 to OUT3, PPG0, PPG1 | — | 30 | — | ns | |



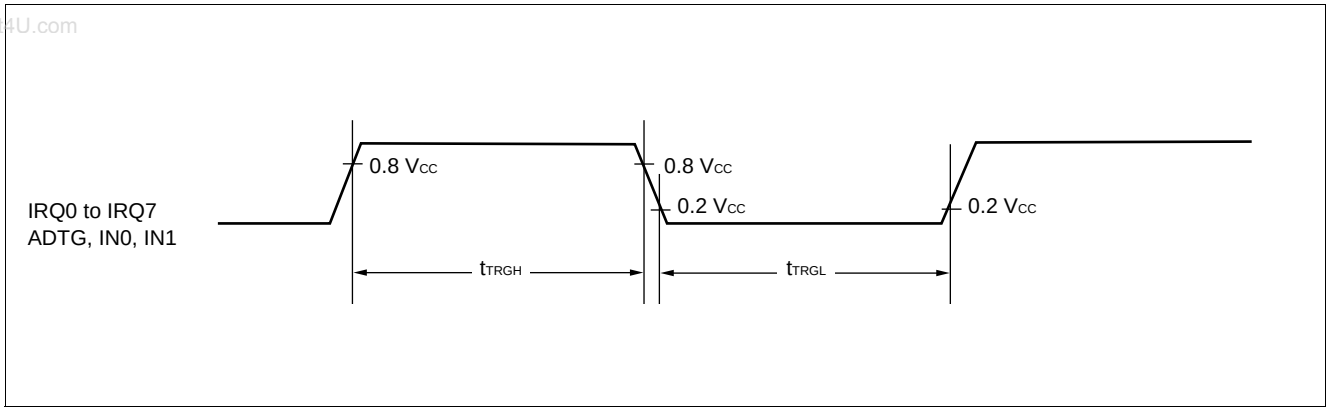
### (13) Trigger Input Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | IRQ0 to IRQ7, ADTG, IN0, IN1 | — | 5 $t_{CP}$ * | — | ns | Under normal operation |
| | | IRQ0 to IRQ5 | | 1 | — | µs | In stop mode |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”





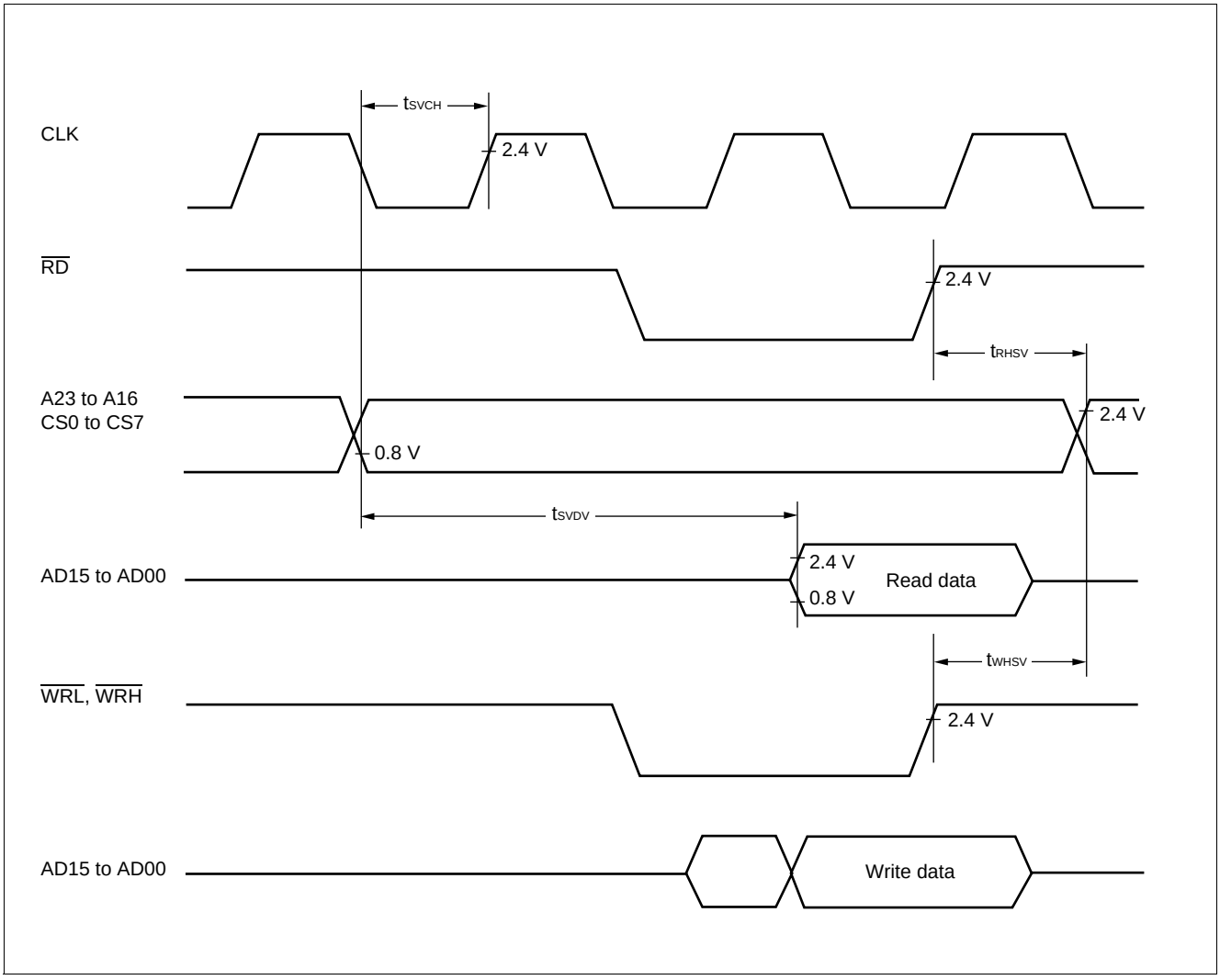
### (14) Chip Select Output Timing

($AV_{CC}$ = $V_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid chip select output → Valid data input time | $t_{SVDV}$ | CS0 to CS7, AD15 to AD00 | — | — | 5 $t_{CP}$*/2 – 60 | ns | |
| $\overline{RD}$ ↑ → chip select output effective time | $t_{RHSV}$ | $\overline{RD}$, CS0 to CS7 | | 1 $t_{CP}$*/2 – 10 | — | ns | |
| $\overline{WR}$ ↑ → chip select output effective time | $t_{WHSV}$ | CS0 to CS7, $\overline{WRL}$, $\overline{WRH}$ | | 1 $t_{CP}$*/2 – 10 | — | ns | |
| Valid chip select output → CLK ↑ time | $t_{SVCH}$ | CLK, CS0 to CS7 | | 1 $t_{CP}$*/2 – 20 | — | ns | |



* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”



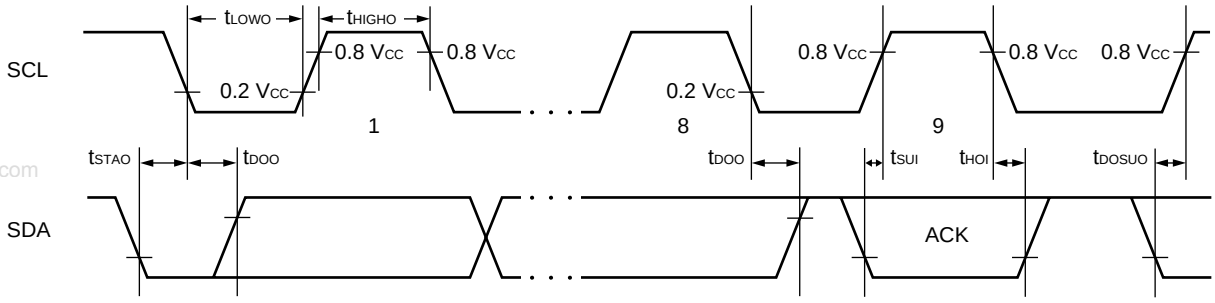
### (15) I²C Timing

($AV_{CC}$ = $V_{CC}$ = 2.7 V to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Internal clock cycle time | $t_{CP}$ | — | — | 62.5 | 666 | ns | All products |
| Start condition output | $t_{STAO}$ | SDA,SCL | | $t_{CP}\times m\times n/2-20$ | $t_{CP}\times m\times n/2+20$ | ns | Only as master |
| Stop condition output | $t_{STOO}$ | | | $t_{CP}(m\times n/2+4)-20$ | $t_{CP}(m\times n/2+4)+20$ | ns | |
| Start condition detection | $t_{STAI}$ | | | $3t_{CP}+40$ | — | ns | Only as slave |
| Stop condition detection | $t_{STOI}$ | | | $3t_{CP}+40$ | — | ns | |
| SCL output “L” width | $t_{LOWO}$ | SCL | | $t_{CP}\times m\times n/2-20$ | $t_{CP}\times m\times n/2+20$ | ns | Only as master |
| SCL output “H” width | $t_{HIGHO}$ | | | $t_{CP}(m\times n/2+4)-20$ | $t_{CP}(m\times n/2+4)+20$ | ns | |
| SDA output delay time | $t_{DOO}$ | SDA,SCL | | $2t_{CP}-20$ | $2t_{CP}+20$ | ns | |
| Setup after SDA output interrupt period | $t_{DOSUO}$ | | | $4t_{CP}-20$ | — | ns | |
| SCL input “L” width | $t_{LOWI}$ | SCL | | $3t_{CP}+40$ | — | ns | |
| SCL input “H” width | $t_{HIGHI}$ | | | $t_{CP}+40$ | — | ns | |
| SDA input setup time | $t_{SUI}$ | SDA,SCL | | 40 | — | ns | |
| SDA input hold time | $t_{HOI}$ | | | 0 | — | ns | |

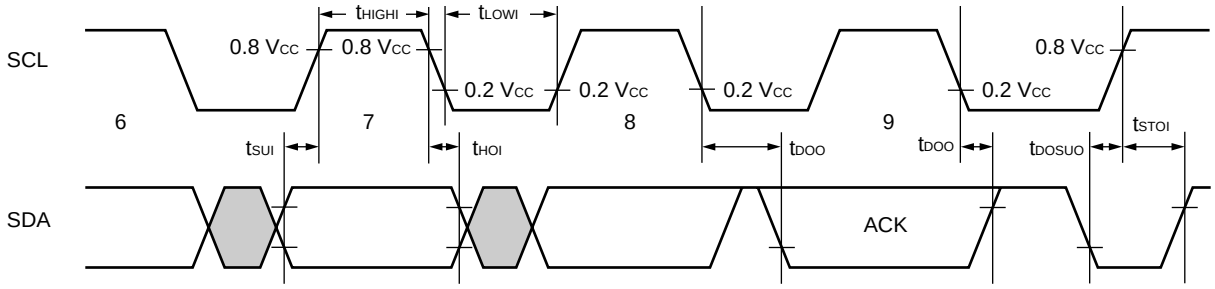
Notes : • “m” and “n” in the above table represent the values of shift clock frequency setting bits (CS4-CS0) in the clock control register “ICCR”. For details, refer to the register description in the hardware manual.
• $t_{DOSUO}$ represents the minimum value when the interrupt period is equal to or greater than the SCL “L” width.
• The SDA and SCL output values indicate that rise time is 0 ns.
• For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”

- **I²C interface [data transmitter (master/slave)]**






- **I²C interface [data receiver (master/slave)]**



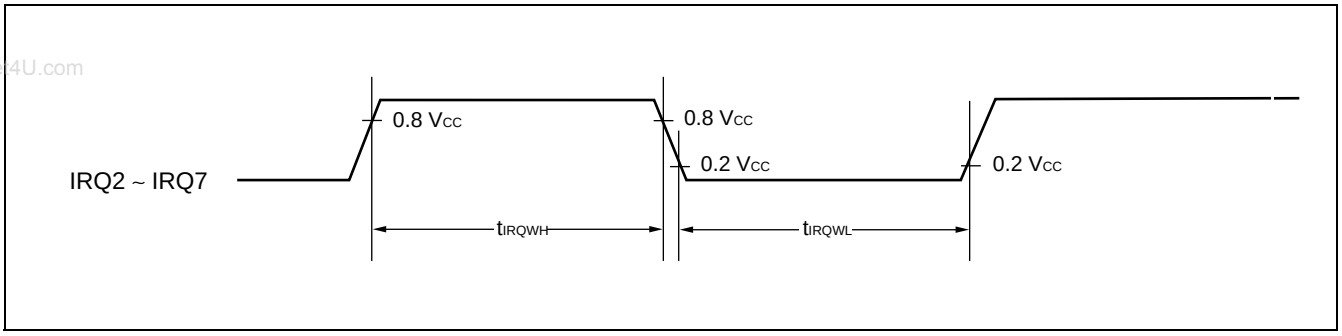
### (16) Pulse Width on External Interrupt Pin at Return from STOP Mode

($AV_{CC}$ = $V_{CC}$ = 2.7 V to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, TA = –40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{IRQWH}$<br>$t_{IRQWL}$ | IRQ2 to IRQ7 | — | $6t_{CP}$ * | — | ns | |

* : For $t_{CP}$ (internal operating clock cycle time), refer to “(3) Clock Timings.”





## 5. A/D Converter Electrical Characteristics

($AV_{CC}$ = $V_{CC}$ = 2.7 V to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, 2.7 V ≦ AVRH – AVRL, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Resolution | — | — | — | — | 8/10 | — | bit |
| Total error | — | — | | — | — | ±5.0 | LSB |
| Non-linear error | — | — | | — | — | ±2.5 | LSB |
| Differential linearity error | — | — | | — | — | ±1.9 | LSB |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | | –3.5 LSB | +0.5 LSB | +4.5 LSB | mV |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN7 | | AVRH –6.5 LSB | AVRH –1.5 LSB | AVRH +1.5 LSB | mV |
| A/D conversion time | — | — | $V_{CC}$ = 5.0 V ±10% at machine clock of 16 MHz | 416$t_{CP}$ | — | — | µs |
| Sampling period | — | — | $V_{CC}$ = 5.0 V ±10% at machine clock of 6 MHz | 64$t_{CP}$ | — | — | µs |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | — | 10 | µA |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | | AVRL | — | AVRH | V |
| Reference voltage | — | AVRH | | AVRL +3.0 | — | $AV_{CC}$ | V |
| | — | AVRL | | 0 | — | AVRH –3.0 | V |
| Power supply current | $I_A$ | $AV_{CC}$ | | — | 5 | — | mA |
| | $I_{AH}$ | $AV_{CC}$ | CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) | — | — | 5 | µA |
| Reference voltage supply current | $I_R$ | AVRH | — | — | 400 | — | µA |
| | $I_{RH}$ | AVRH | CPU stopped and 8/10-bit A/D converter not in operation ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) | — | — | 5 | µA |
| Offset between channels | — | AN0 to AN7 | — | — | — | 4 | LSB |

## 6. A/D Converter Glossary

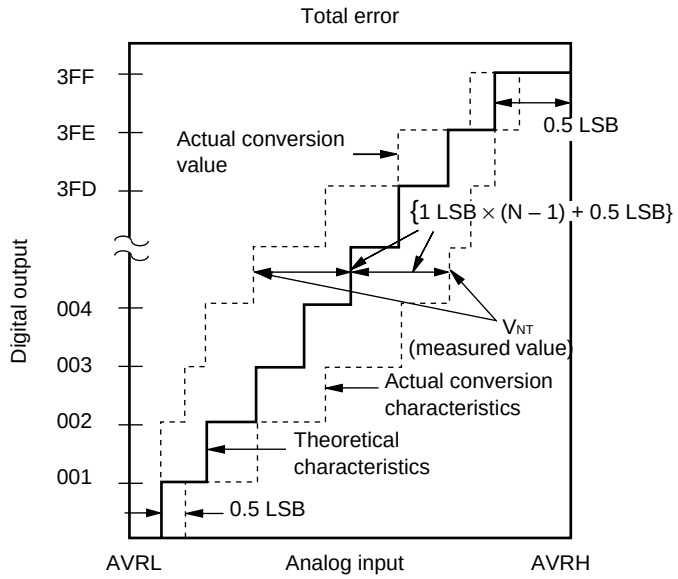
Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.






1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

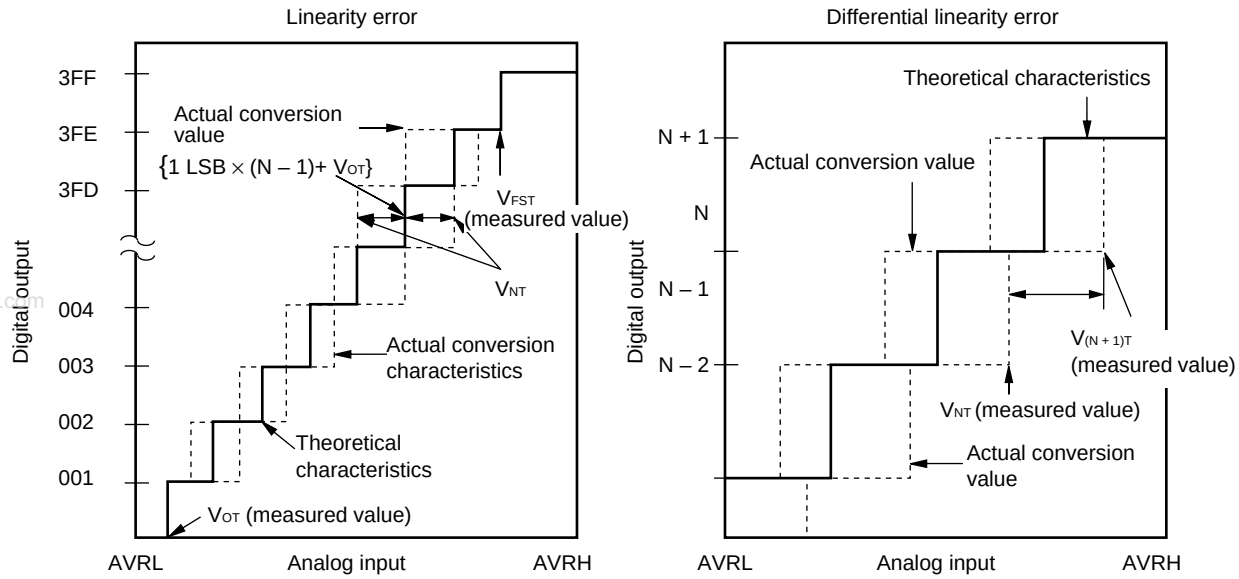
$V_{OT}$ (Theoretical value) = AVRL + 0.5 LSB[V]

$V_{NT}$: Voltage at a transition of digital output from (N – 1) to N

$V_{FST}$ (Theoretical value) = AVRH – 1.5 LSB[V]

*(Continued)*

*(Continued)*




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$V_{OT}$: Voltage at transition of digital output from "$000_H$" to "$001_H$"
$V_{FST}$: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

## 7. Notes on Using A/D Converter

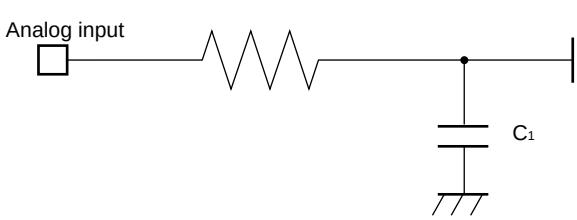
Select the output impedance value for the external circuit of analog input according to the following conditions. Output impedance values of the external circuit MB90V570/V570A/573/574 are 5 kΩ or lower, MB90F574/574A/574C are 10 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz).



- **Equipment of analog input circuit model**




| | |
|---|---|
| MB90573/4, MB90V570/A | R ≅ 3.2 kΩ, C ≅ 30 pF |
| MB90F574/A | R ≅ 7.1 kΩ, C ≅ 48.3 pF |
| MB90574C | R ≅ 2.2 kΩ, C ≅ 45 pF |

Note : Listed values must be considered as standards.

- **Error**

  The smaller the | AVRH – AVRL |, the greater the error would become relatively.

## 8. D/A Converter Electrical Characteristics

($AV_{CC}$ = $V_{CC}$ = $DV_{CC}$ = 5.0 V ±10%, $AV_{SS}$ = $V_{SS}$ = $DV_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 8 | — | bit | |
| Differential linearity error | — | — | — | — | ±0.9 | LSB | |
| Absolute accuracy | — | — | — | — | ±1.2 | % | |
| Linearity error | — | — | — | — | ±1.5 | LSB | |
| Conversion time | — | — | — | 10 | 20 | µs | Load capacitance: 20 pF |
| Analog reference voltage | — | $DV_{CC}$ | $V_{SS}$ + 3.0 | — | $AV_{CC}$ | V | |
| Reference voltage supply current | $I_{DVR}$ | $DV_{CC}$ | — | 120 | 300 | µA | Conversion under no load |
| | $I_{DVRS}$ | $DV_{CC}$ | — | — | 10 | µA | In sleep mode |
| Analog output impedance | — | — | — | 20 | — | kΩ | |

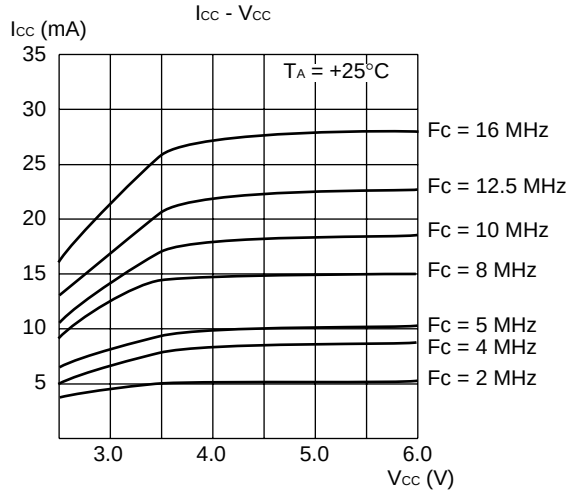


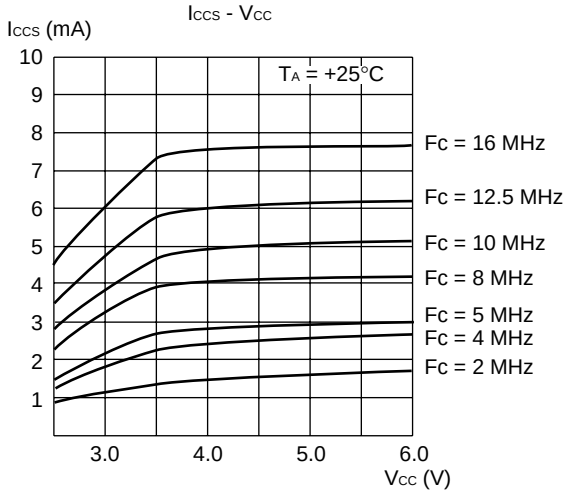
## 9. Flash Memory Program/Erase Characteristics

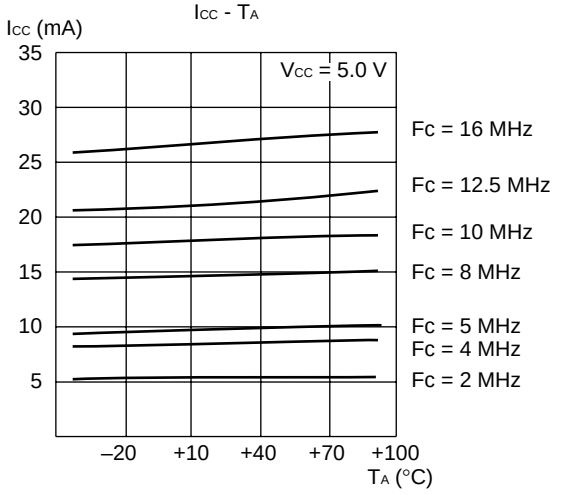
| Parameter | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = + 25°C $V_{CC}$ = 5.0 V | — | 1.5 | 30 | s | Except for the write time before internal erase operation |
| Chip erase time | | — | 13.5 | — | s | Except for the write time before internal erase operation |
| Word (16bit width) programming time | | — | 32 | 1,000 | µs | Except for the over head time of the system |
| Program/Erase time | — | 10,000 | — | — | cycle | |
| Data hold time | — | 100,000 | — | — | h | |

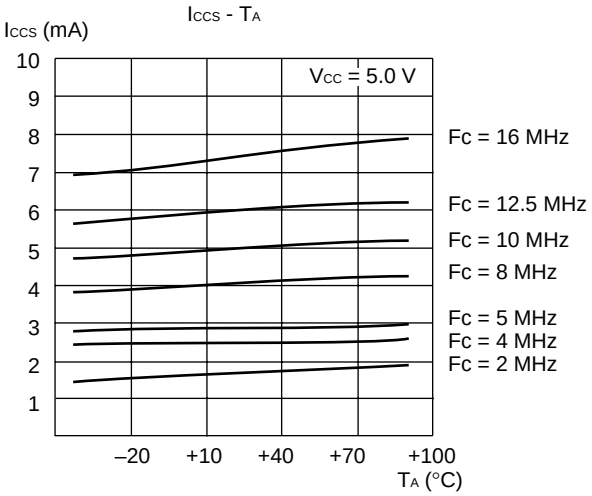
## ■ EXAMPLE CHARACTERISTICS

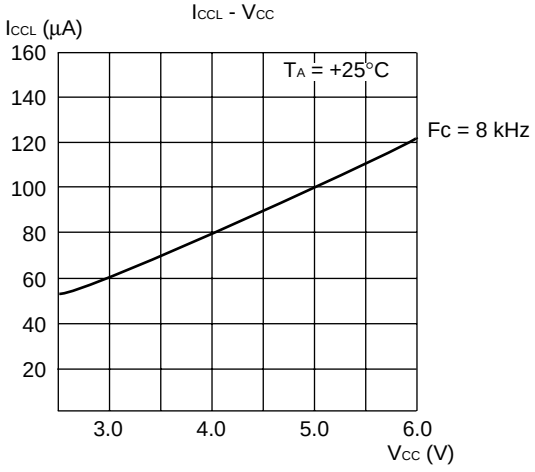
### (1) Power Supply Current (MB90574)

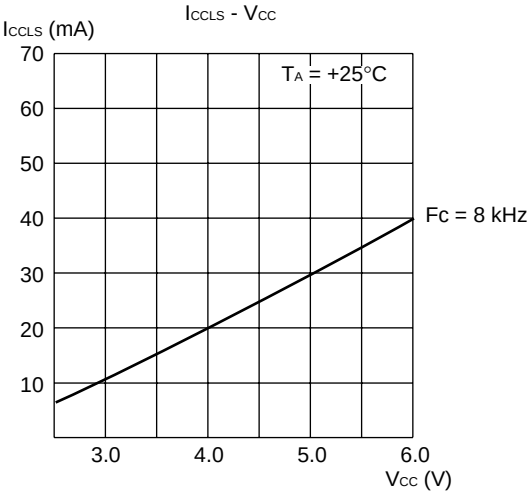
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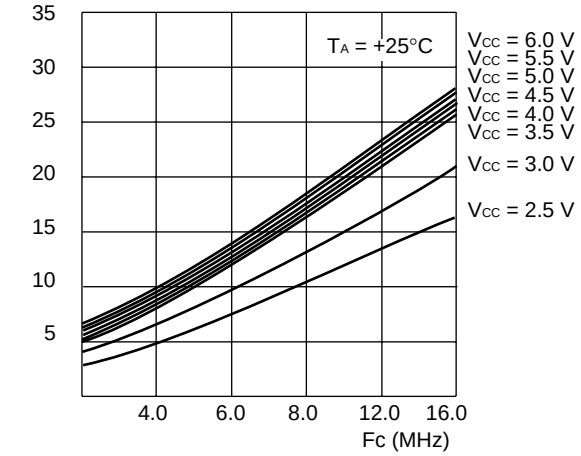
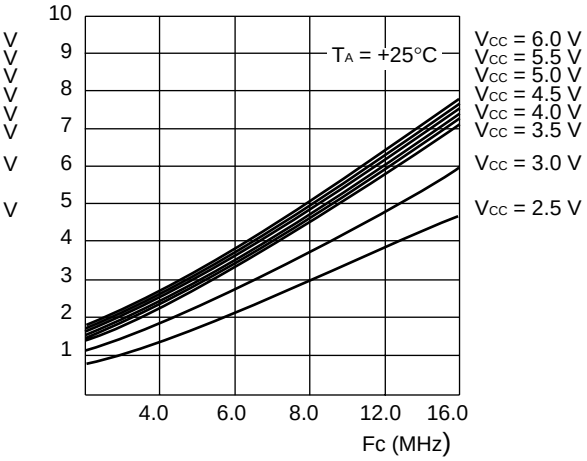
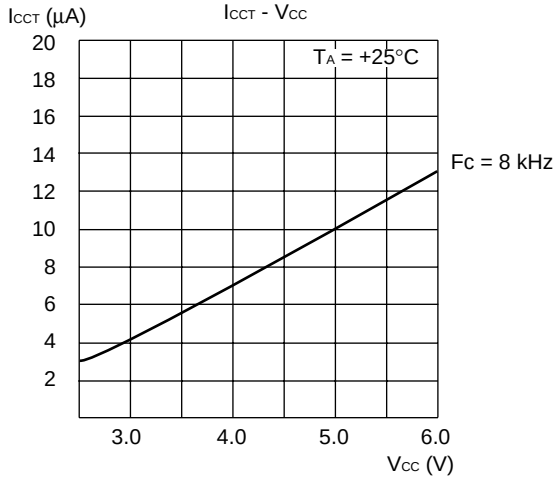
$I_{CC}$ - Fc



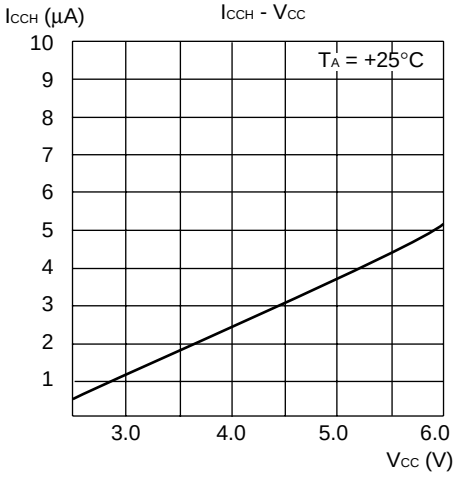

$I_{CCS}$ - Fc



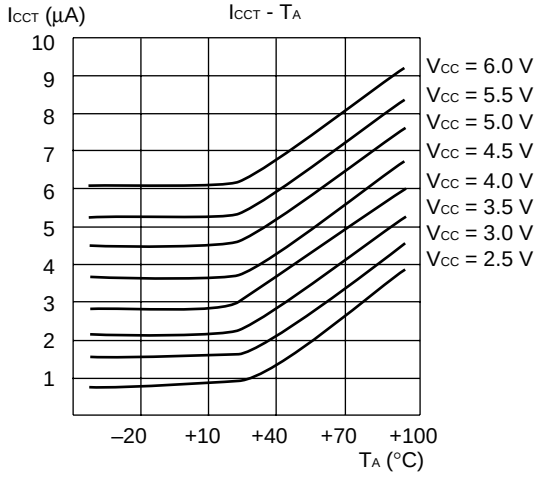

$I_{CCT}$ - $V_{CC}$



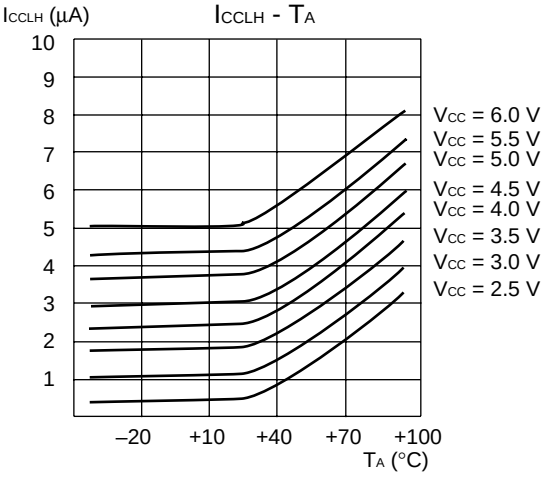

$I_{CCH}$ - $V_{CC}$




$I_{CCT}$ - $T_A$




$I_{CCLH}$ - $T_A$

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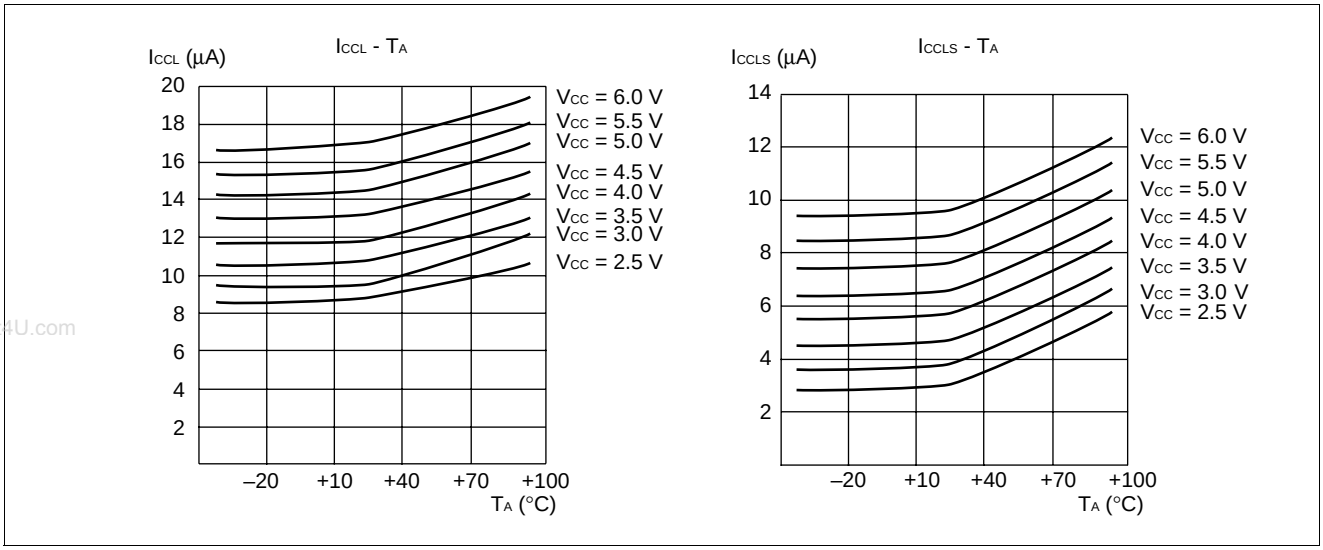
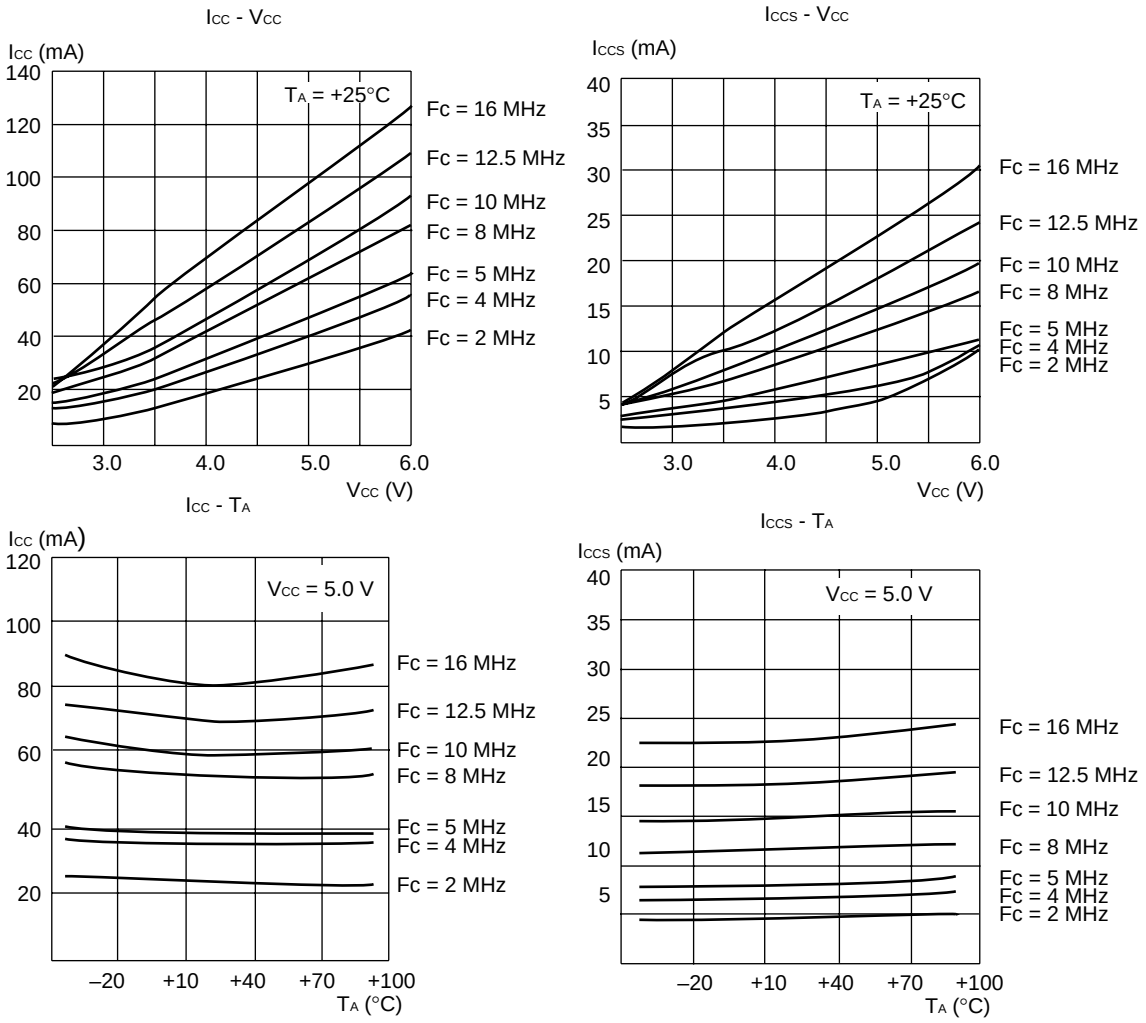


### (2) Power Supply Current (MB90F574)



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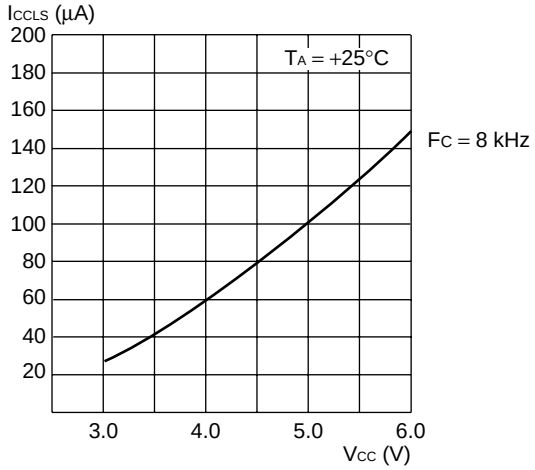
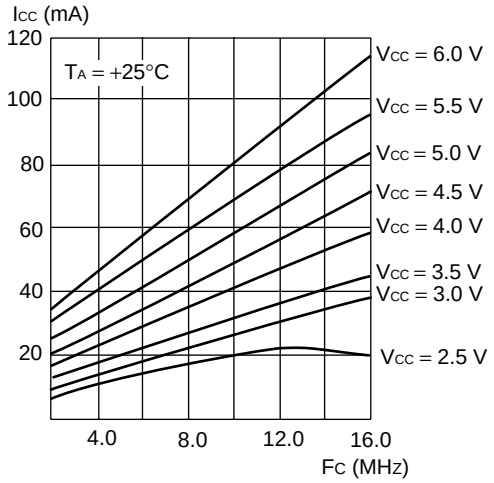
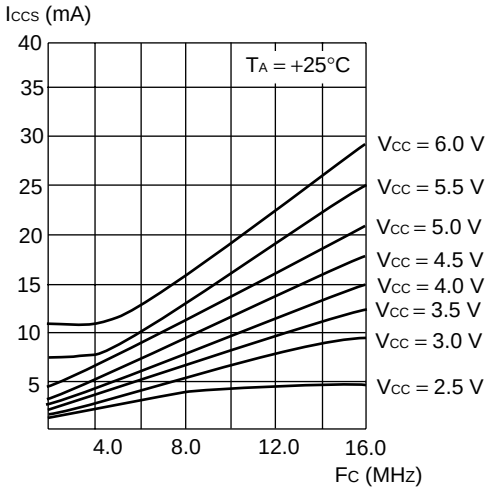
$I_{CCLS}$ - $V_{CC}$



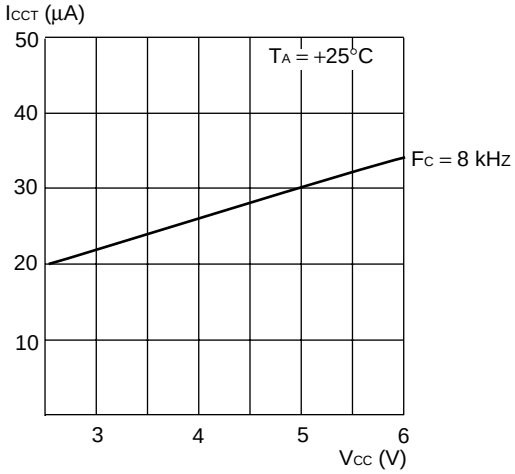

$I_{CC}$ - $F_C$



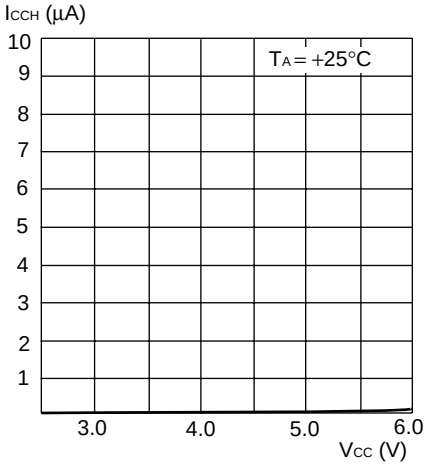

$I_{CCS}$ - $F_C$




$I_{CCT}$ - $V_{CC}$




$I_{CCH}$ -$V_{CC}$

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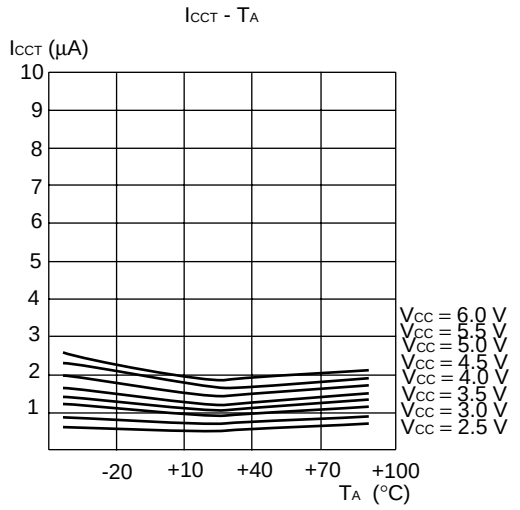
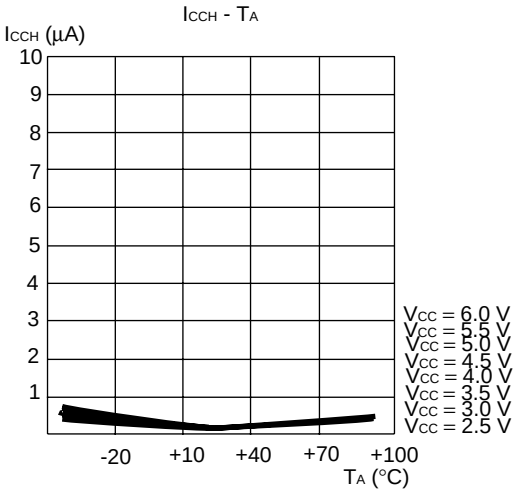
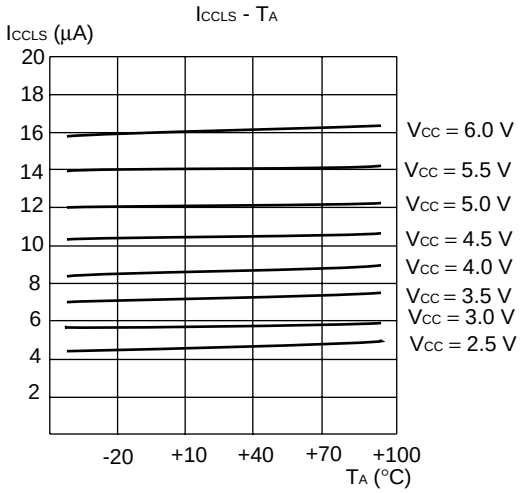
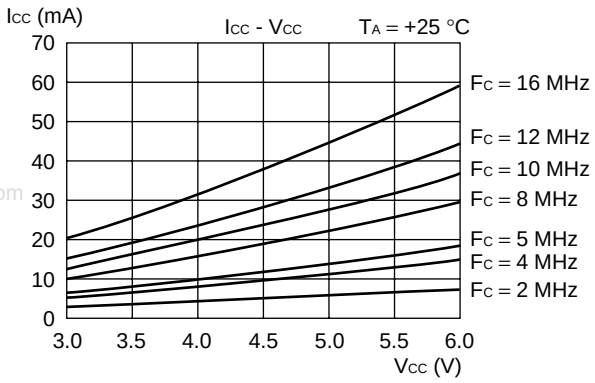


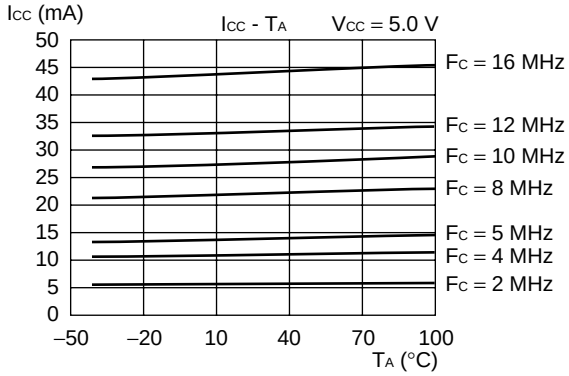



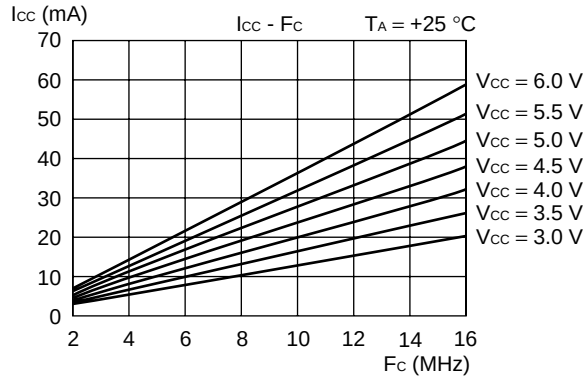



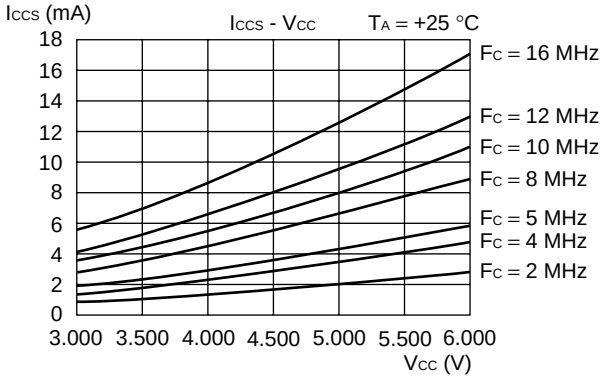
### (3) Power Supply Current (MB90574C)

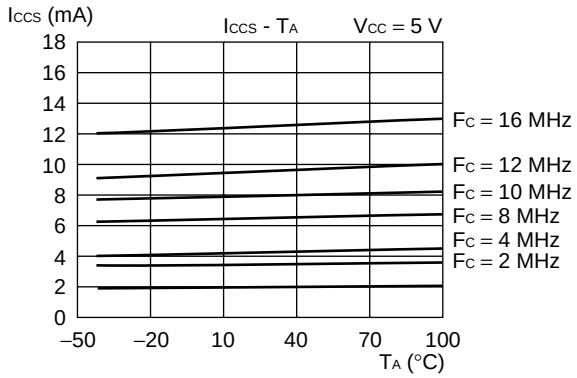


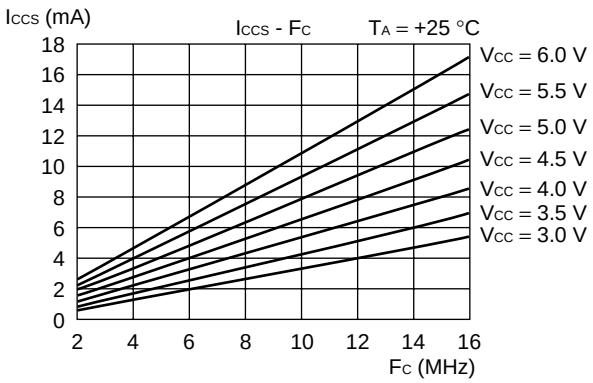
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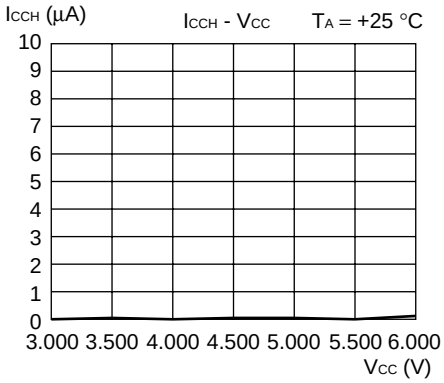


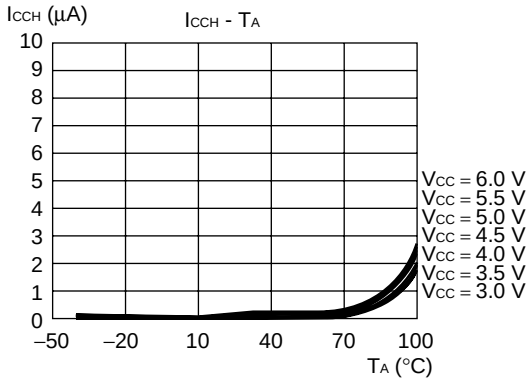


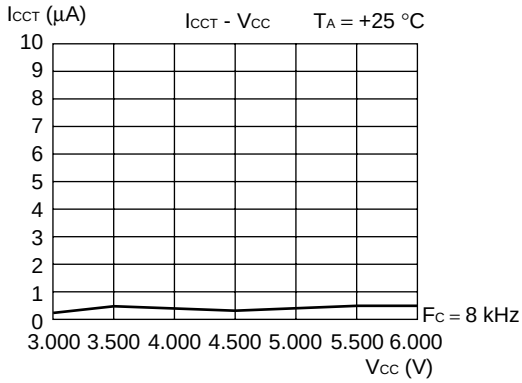


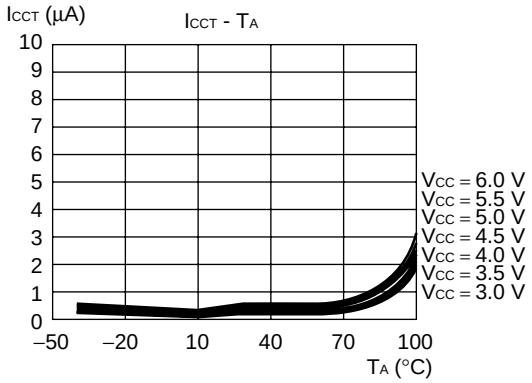


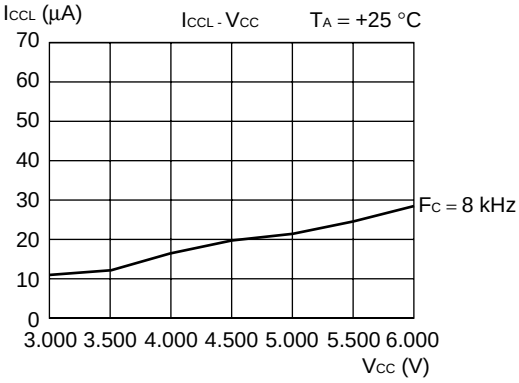


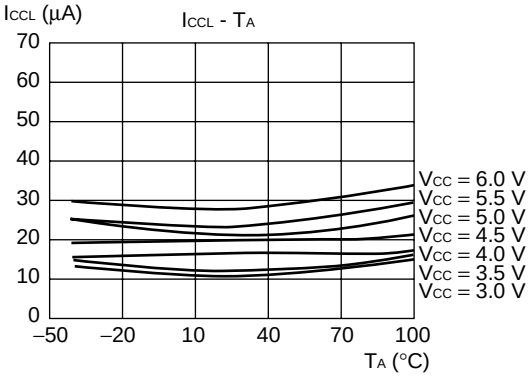


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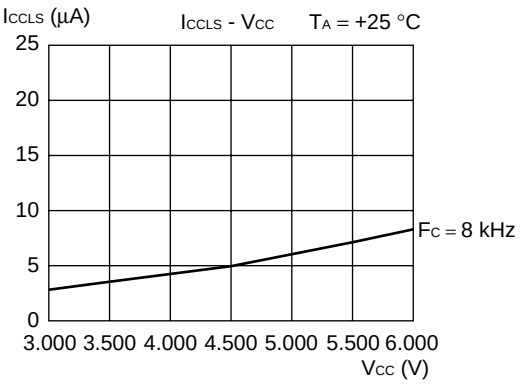
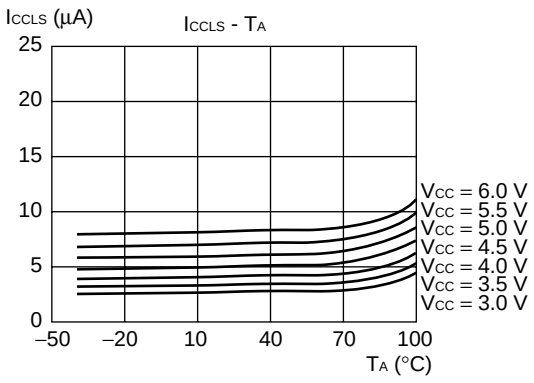


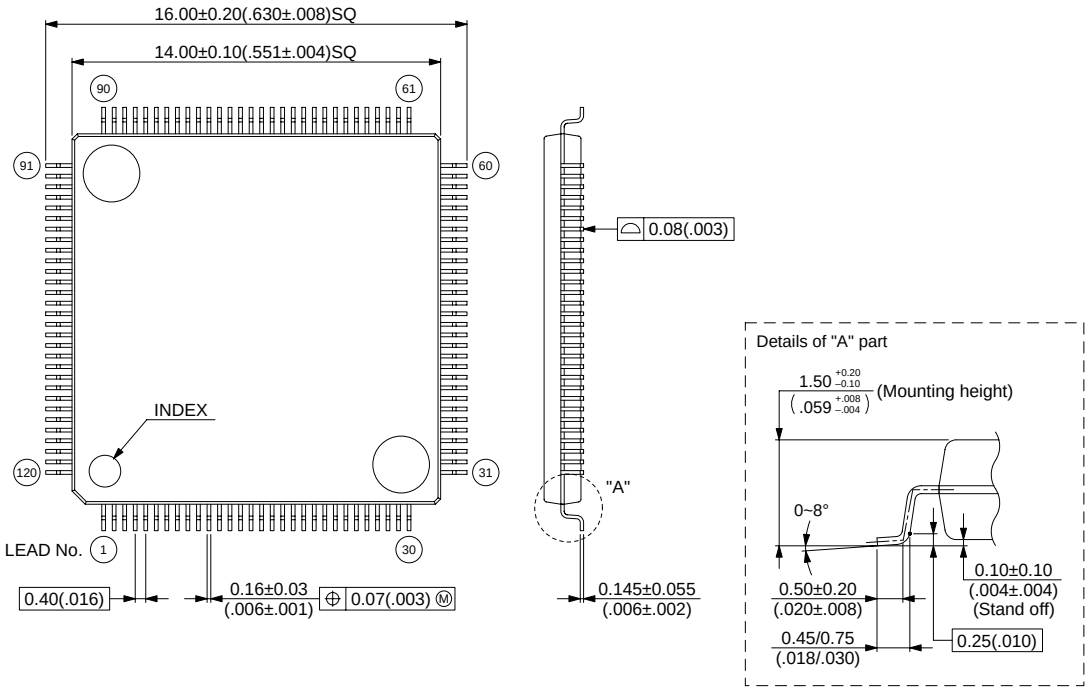



## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90573PFF<br>MB90574PFF<br>MB90F574PFF<br>MB90F574APFF | 120-pin Plastic LQFP<br>(FPT-120P-M05) | |
| MB90573PFV<br>MB90574PFV<br>MB90574CPFV<br>MB90F574PFV<br>MB90F574APFV | 120-pin Plastic QFP<br>(FPT-120P-M13) | |
| MB90574CPMT<br>MB90F574APMT | 120-pin Plastic LQFP<br>(FPT-120P-M21) | |

## ■ PACKAGE DIMENSIONS

120-pin plastic LQFP
(FPT-120P-M05)






Dimensions in mm (inches)

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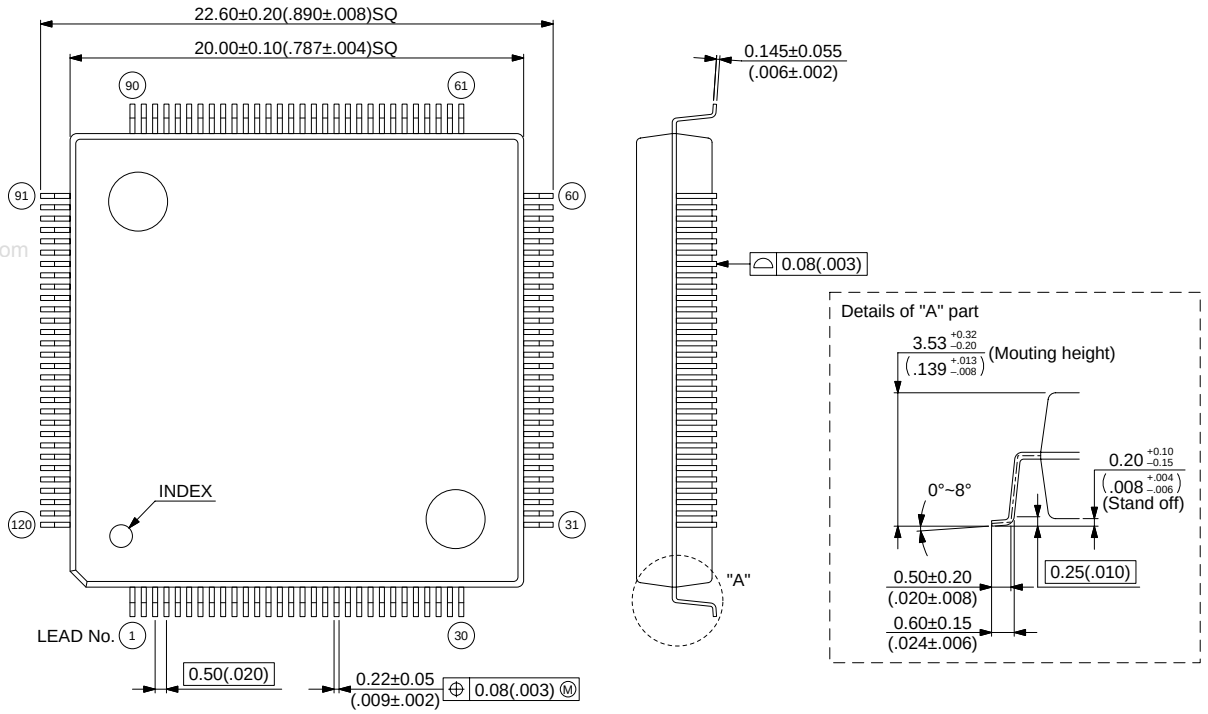
120-pin plastic QFP
(FPT-120P-M13)



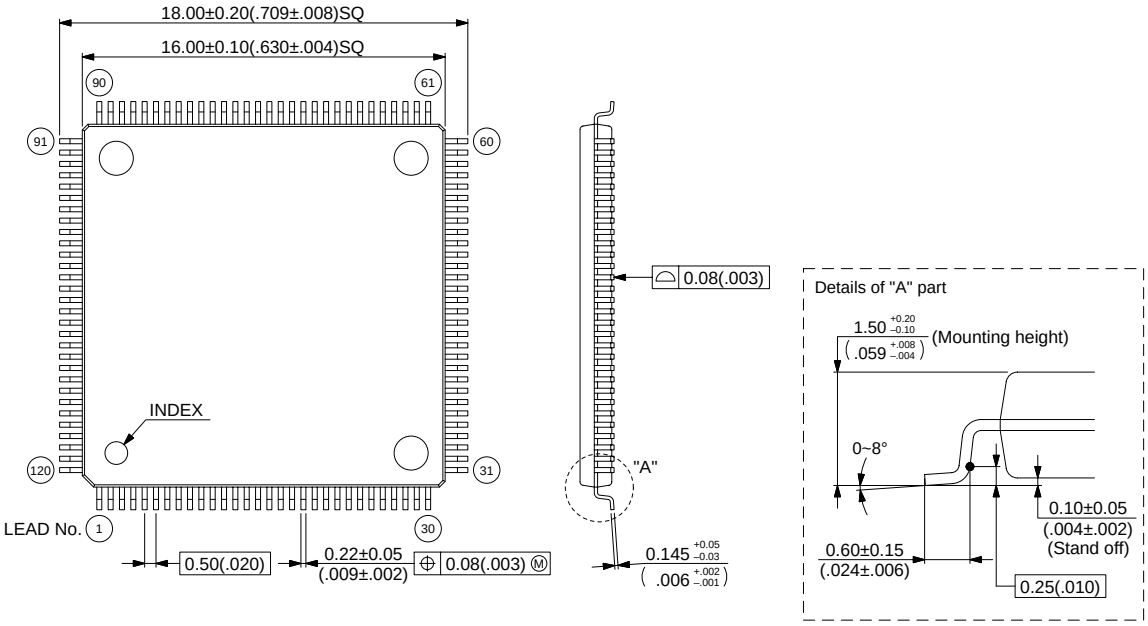



Dimensions in mm (inches)

*(Continued)*

*(Continued)*

120-pin plastic LQFP
(FPT-120P-M21)








Dimensions in mm (inches)

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