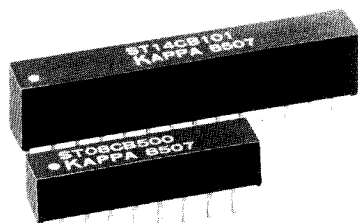


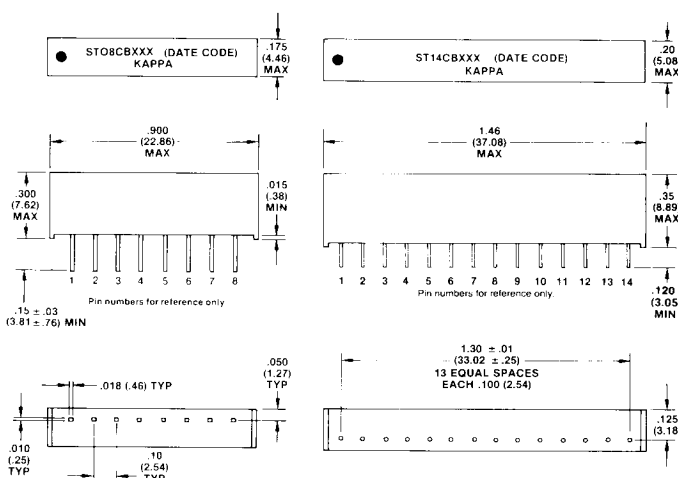
SERIES ST08C/ST14C TTL SCHOTTKY (8-PIN/14-PIN) 5-&10-TAP SIP DELAY LINES



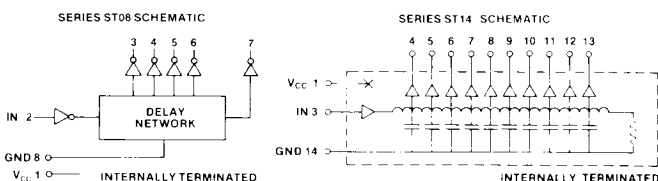
FEATURES

- 8-Pin (ST08C) and 14-Pin (ST14C) SIP Package
- TTL Schottky interfaced
- 5/10 equally-spaced taps
- Risettime: 4 ns max⁽⁵⁾⁽⁶⁾
- Total delays from 25-1000 ns

MARKINGS AND DIMENSIONS, in (mm)



24 AWG round leads may be used.



RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V _{CC} Supply Voltage	4.75	5.00	5.25	V
V _{IH} High-Level Input Voltage	2.0			V
V _{IL} Low-Level Input Voltage			0.8	V
I _{IK} Input Clamp Current			-18	mA
I _{OH} High-Level Output Current			-1.0	mA
I _{OL} Low-Level Output Current			20	mA
T _A Operating Free-Air Temperature	0	+25	+70	°C

DC ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

V _{OH} High-Level Output Voltage	V _{CC} = min, V _{IH} = min, I _{OH} = max	2.7	3.4		V
V _{OL} Low-Level Output Voltage	V _{CC} = min, V _{IL} = max, I _{OL} = max			0.5	V
V _{IK} Input Clamp Voltage	V _{CC} = min, I _I = I _{IK}			-1.2	V
I _{IH} High-Level Input Current	V _{CC} = max, V _{IN} = 2.7V			50	μA
	V _{CC} = max, V _{IN} = 5.25V			1.0	mA
I _{IL} Low-Level Input Current	V _{CC} = max, V _{IN} = 0.5V			-2	mA
I _{OS} Short Circuit Output Current	V _{CC} = max, V _{OUT} = 0, one output at a time	-40		-100	mA
I _{CCH} High-Level Supply Current	V _{CC} = max, V _{IN} = OPEN		30/60	45/75	mA
I _{CCL} Low-Level Supply Current	V _{CC} = max, V _{IN} = 0		65/120	75/150	mA
N _H Fanout High-Level Output	V _{CC} = max, V _{OH} = 2.7V			20	TTL load
N _L Fanout Low-Level Output	V _{CC} = max, V _{OL} = 0.5V			10	TTL load

INPUT PULSE TEST CONDITIONS

E _{IN} Pulse Voltage	3.1	3.2	3.3	V
T _{RI} Pulse Rise-Time			2.0	ns
T _W Pulse Width, of Total Delay	40/20	100		%
d Duty Cycle		33.3	50	%

PART NUMBER ⁽⁷⁾	Total Delay (ns) ^{(1) (2)}	Tap Delay (ns) ^{(1) (2)}
ST08CB250	25	5
ST08CB500	50	10
ST08CB750	75	15
ST08CB101	100	20
ST08CB251	250	50
ST08CB501	500	100
ST14CD500	50	5
ST14CD101	100	10
ST14CD151	150	15
ST14CD201	200	20
ST14CD251	250	25
ST14CD501	500	50
ST14CD102	1000	100

Notes:

1. Delays measured at 1.5V level on leading edge only.
2. Delay tolerances: ±5% or ±2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: V_{CC} = T_{yp}, T_A = T_{yp}, E_{IN} = T_{yp}, T_{RI} = max, T_W = T_{yp}, P_{RR} = 1MHz (or d/t_w, whichever is less), R_L 1 megohm and C_L 2pf.
3. Temperature coefficient of delay will vary, depending upon total delay, according to the formula: T_{PTA} = (100 + (25,000/T_{PLH})).
4. Delay will vary approximately 4% for every 5% change in supply voltage.
5. Risettime measured from 0.75V to 2.4V level.
6. Measured with no loads on taps.
7. Other delays also available upon request.

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TECHNOLOGIES, INC.

U.S.A. Factory Direct: 1443 Pinewood Street, Rahway, NJ 07065, Phone (908) 396-9400, Toll Free 800-223-0603