DATA SHEET

TDA8540
4 × 4 video switch matrix

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

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PHILIPS

4 × 4 video switch matrix | TDA8540

FEATURES

- I²C-bus or non-I²C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Slave receiver in the I²C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.

APPLICATIONS

- Colour Television (CTV) receivers
- Peritelevision sets
- Satellite receivers.

GENERAL DESCRIPTION

The TDA8540 has been designed for switching between composite video signals, therefore the minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, to enable parallel connection of several devices.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	–	8.8	V
I_{CC}	supply current		–	20	30	mA
I_{SO}	isolation 'OFF' state	at f = 5 MHz	60	80	–	dB
B	3 dB bandwidth		12	–	–	MHz
α_{ct}	crosstalk attenuation between channels		60	70	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8540	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA8540T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

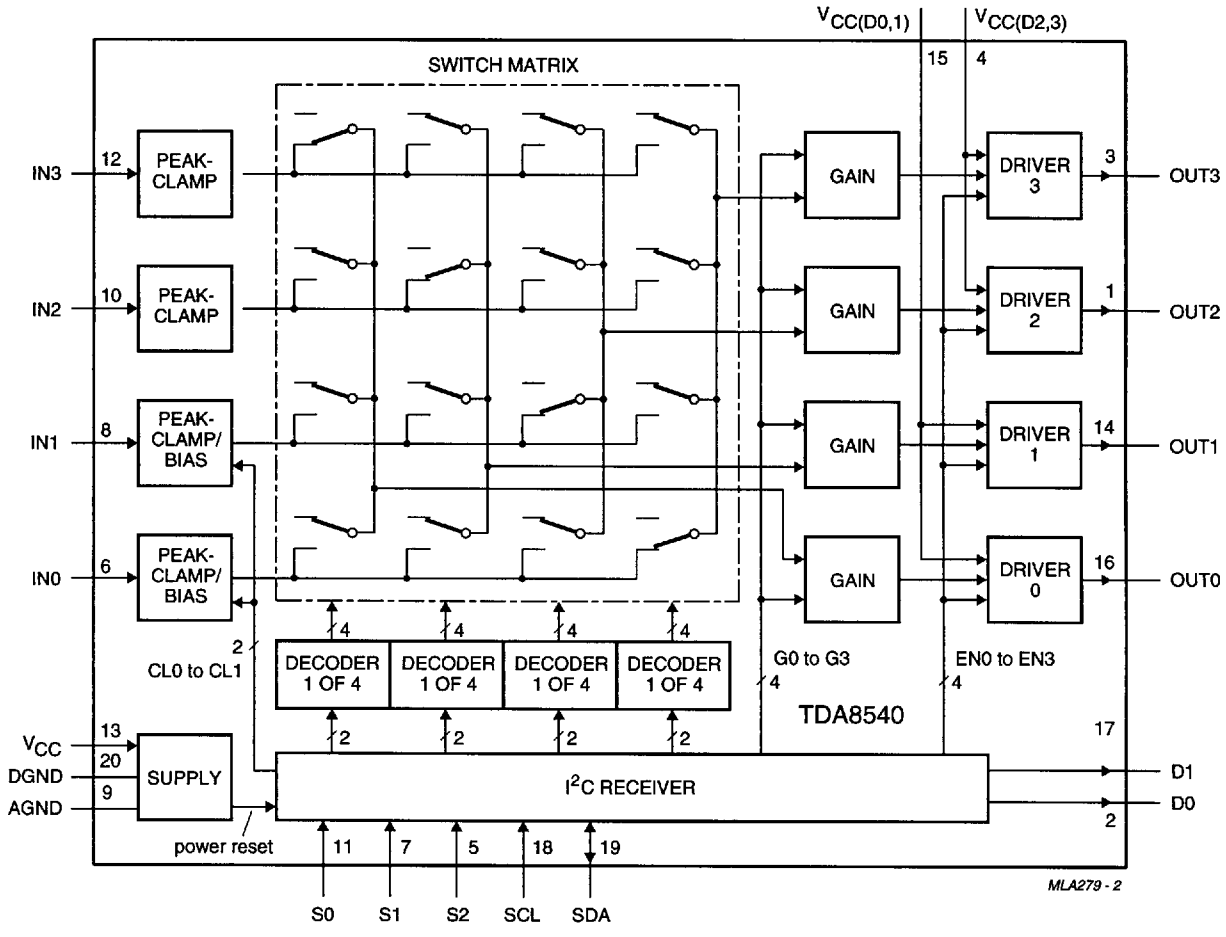


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT2	1	video output 2
D0	2	control output 0
OUT3	3	video output 3
$V_{CC(D2,3)}$	4	driver supply voltage; for drivers 2 and 3
S2	5	sub-address input 2
IN0	6	video input 0 (CVBS or chrominance signal)
S1	7	sub-address input 1
IN1	8	video input 1 (CVBS or chrominance signal)
AGND	9	analog ground
IN2	10	video input 2 (CVBS or luminance signal)
S0	11	sub-address input 0
IN3	12	video input 3 (CVBS or luminance signal)
V_{CC}	13	general supply voltage
OUT1	14	video output 1
$V_{CC(D0,1)}$	15	driver supply voltage; for drivers 0 and 1
OUT0	16	video output 0
D1	17	control output 1
SCL	18	serial clock input
SDA	19	serial data input/output
DGND	20	digital ground

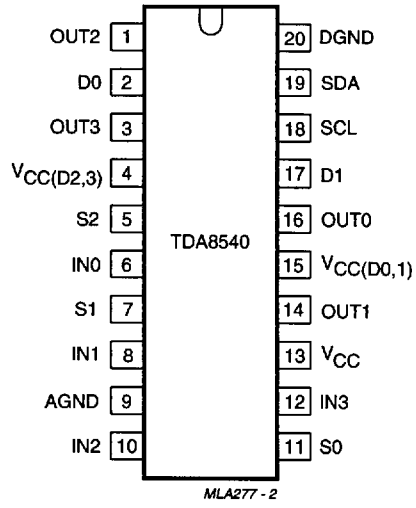


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus. 3 bits of the I²C address can be selected via the address pin, thus providing a facility for parallel connection of 7 devices.

Control options via the I²C-bus:

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 1× or 2×.
- Each of the four outputs can individually be connected to one of the four inputs.
- Each output can individually be set in a high impedance state.
- Two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18) can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses or switching to the non-I²C mode. Inputs S0 to S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

Table 1 I²C-bus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	A0
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0 and D1 are at a LOW level.

Detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

The TDA8540 is a **slave receiver** and the protocol is given in Table 2.

Table 2 The TDA8540 protocol

SEQUENCE									
S[1]	SLV[2]	A[3]	SUB	A[3]	DATA	A[3]	DATA	A[3]	P[4]

Notes

1. S = START condition.
2. Data transmission to the TDA8540 starts with the slave address (SLV).
3. A = acknowledge bit, generated by TDA8540.
4. P = STOP condition.

Table 3 Data transmission to the TDA8540 begins with SLV

A6 MSB	A5	A4	A3	A2	A1	A0	R/$\overline{W}$ LSB
1	0	0	1	A2[1]	A1[1]	A0[1]	0[2]

Notes

1. A2 to A0: pin programmable slave address bits.
2. R/$\overline{W}$ = 0; write only.

After the SLV, a second byte, SUB, is required for selecting the functions, as shown in Table 4.

Table 4 The second byte: SUB

7 MSB	6	5	4	3	2	1	0 LSB
0	0	0	0	0	0	RS1	RS0

Options for SUB:

If SUB = 00H: access to switch control (SW1)

If SUB = 01H: access to gain/clamp/data control (GCO)

If SUB = 02H: access to output enable control (OEN).

Remarks:

If more than one data byte is sent, the SUB byte will be automatically incremented.

If more than 3 data bytes are sent, the internal counter will roll over and the device will then rewrite the first register.

Data Bytes

SWI (SUB = 00H): selects which input is connected to the different outputs, as shown in Table 5.

Table 5 SWI (SUB = 00H) selection of inputs connected to outputs

7 MSB	6	5	4	3	2	1	0 LSB
S31	S30	S21	S20	S11	S10	S01	S00

Table 6 Selection of inputs

OUTPUT	Sj1 AND Sj0[1]			
	00	01	10	11
OUTj	IN0	IN1	IN2	IN3

Note

1. For j = 0 to 3.
   Example: if S21 = 0 and S20 = 1, then OUT2 is connected to IN1.

GCO (SUB = 01H):

- Selects the gain of each output.
- Selects the clamp action or mean value on inputs 0 and 1.
- Determines the value of the auxiliary outputs D1 and D0.

Table 7 GCO byte

7 MSB	6	5	4	3	2	1	0 LSB
G3[1]	G2[1]	G1[1]	G0[1]	CL1[2]	CL0[2]	D1[3]	D0[3]

Notes

1. For j = 0 to 3: if Gj = 0 (1), then output j has a gain of 2 (1).
2. If CL0 (CL1) = 0, then input signal on IN0 (IN1) is clamped.
3. For j = 0 or 1: if Dj = 0 (1), then logical output j is LOW (HIGH).

OEN (SUB = 02H): selects, for each output, if the output is active or high impedance, see Table 8.

Table 8 OEN (SUB = 02H) determines which output is active or high impedance

7 MSB	6	5	4	3	2	1	0 LSB
X(1)	X(1)	X(1)	X(1)	EN3(2)	EN2(2)	EN1(2)	EN0(2)

Notes

1. X = don't care.
2. For j = 0 to 3: if ENj = 0 (1), then OUT j is high impedance (active).

After a power-on reset:

- The outputs are set to a high impedance state; the outputs are connected to IN0; the gains are set at two and inputs IN0 and IN1 are clamped.
- Programming of the device is necessary because the outputs are in high impedance state.

Non-I²C-bus control

If the S0, S1 and S2 pins are all connected to V_{CC} the device will enter the non-I²C-bus mode.

After a power-on reset:

- Gain is set at two for all outputs.
- All inputs are clamped.
- All outputs are active.
- The matrix position is given by the SDA and SCL voltage level.

Table 9 Non-I²C-bus control

OUTPUT	SCL AND SDA			
	00	01	10	11
OUT3	IN3	IN2	IN1	IN0
OUT2	IN2	IN3	IN0	IN1
OUT1	IN1	IN0	IN3	IN2
OUT0	IN0	IN1	IN2	IN3

SCL and SDA act as normal input pins:

SCL interchanges (OUT3 and OUT2) with (OUT1 and OUT0).

SDA interchanges OUT3 with OUT2 and OUT1 with OUT0.

Remark: For use with chrominance signals, the clamp action must be overruled by external bias.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage (pin 13)		−0.3	+9.1	V
P_{tot}	total power dissipation		−	750	mW
$V_{CC(D0,1)}$, $V_{CC(D2,3)}$	driver supply voltage		−0.3	+13.8	V
IN0 to IN3	video input voltage		−0.3	+7.2	V
OUT0 to OUT3	video output voltage		−0.3	+7.2	V
D0, D1	control output voltage		−0.3	+7.2	V
SDA, SDL	I^2C input/output voltage		−0.3	+8.8	V
S0 to S2	sub-address input voltage		−0.3	+8.8	V
T_{stg}	IC storage temperature		−55	+125	°C
T_j	junction temperature		−	+150	°C
V_{es}	electrostatic handling	HBM; note 1	−1500	+1500	V
		MM; note 2	−200	+200	V

Notes

1. Human Body Model (HBM): in accordance with UZW-BO/FQ-A302.
2. Machine Model (MM): in accordance with UZW-BO/FQ-B302 (stress reference pins: AGND and DGND short-circuited and V_{CC}).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT146-1	60 (typ.)	K/W
	SOT163-1	85 (typ.)	K/W

OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage (pin 13)		7.2	−	8.8	V
T_{amb}	operating ambient temperature		0	−	70	°C
Video inputs (pins 6, 8, 10 and 12)						
C_I	external capacitor		−	100	−	nF
$V_{I(p-p)}$	C signal amplitude (peak-to-peak value)	note 1	−	−	1	V
$V_{I(p-p)}$	CVBS or Y-signal amplitude (peak-to-peak value)	note 2	−	−	1.5	V
Video drivers (pins 4 and 15)						
R_D	external collector resistor	note 3	−	25	−	Ω
C_D	external decoupling capacitor	note 4	−	22	−	µF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sub-address S0, S1 and S2 (pins 5, 7 and 11)						
V_{IH}	HIGH level input voltage		4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	1	V

Notes

1. Only for pins 6 and 8 when clamp action is not selected for these pins.
2. On all the video input pins, when non-I²C-bus control mode is selected or when clamp action is selected on pins 6 and 8 (by I²C-bus control).
3. Connected between V_{CC} and pin 4 or pin 15.
4. Connected between AGND and pin 4 or pin 15.

CHARACTERISTICS

V_{CC} = 8 V; T_{amb} = 25 °C; gain condition, clamp condition and OFF state are controlled by the I²C-bus; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_{CC}	supply current	without load	–	20	30	mA
		OFF state	–	12	–	mA
Video inputs: IN0 to IN3 when the clamp is active (see Figs 3 and 4)						
I_{LI}	input leakage current	V_I = 3 V	–	0.4	1	µA
V_{clamp}	input clamping voltage	I_I = 5 µA	–	2.2	–	V
I_{clamp}	input clamping current	V_I = 0 V	1.2	–	–	mA
Video inputs: IN0 and IN2 when the clamp is not active (see Fig.3)						
V_{bias}	DC input bias level	I_I = 0	–	2.9	–	V
R_I	input resistance		–	10	–	kΩ
Video outputs: OUT0 to OUT3 (see Fig.5)						
Z_O	output impedance	OFF state	100	–	–	kΩ
R_O	output resistance		–	5	–	Ω
ISO	isolation	OFF state; f = 5 MHz	60	–	–	dB
V_O	output top sync level; (Y or CVBS)		0.4	0.7	1	V
V_{bias}	output mean value for chrominance signals	G = 2; load = 150 Ω	1.5	1.9	2.2	V
		G = 1; without load	1	1.3	1.6	V
G_v	voltage gain	G = 1; f = 1 MHz	−1	0	+1	dB
		G = 2; f = 1 MHz	5	6	7	dB
G_{diff}	differential gain	note 1	–	0.5	3	%
φ_{diff}	differential phase	note 1	–	0.6	–	deg
NL	non linearity	note 2	–	0.5	2	%
α_{ct}	crosstalk attenuation between channels	note 3	60	70	–	dB
SVRR	supply voltage rejection	note 4	36	55	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG	maximum gain variation	100 kHz < f < 5 MHz	–	0.5	–	dB
		100 kHz < f < 8.5 MHz	–	1	–	dB
		100 kHz < f < 12 MHz	–	3	–	dB
α_{ct}	crosstalk attenuation of I²C-bus signals		60	–	–	dB
Auxiliary outputs D0 and D1 (open collector)						
I_{OH}	HIGH level output current	V_{OH} = 5.5 V	–	–	10	μA
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	–	–	0.4	V
I²C-bus inputs SCL and SDA						
I_{IH}	HIGH level input current	V_{IH} = 3.0 V	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 1.5 V	−10	–	–	μA
C_i	input capacitance		–	–	10	pF
I²C-bus output SDA						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
Sub-address S0, S1 and S2						
I_{IH}	HIGH level input current	$V_{IH} = V_{CC}$	–	–	10	μA
I_{IL}	LOW level input current	V_{IL} = 0 V	–	–	10	μA

Notes

1. Gain set at 2; R_L = 150 Ω; test signal D2 from CCIR 330.
2. Gain set at 2; R_L = 150 Ω; test signal D1 from CCIR 17.
3. Measured from any selected input to output; f = 5 MHz; R_L = 150 Ω; gain set at 2; V_I = 1.5 V (peak-to-peak value). This measurement requires an optimized board.
4. Supply voltage ripple rejection: $20 \log \frac{V_{ripple\ (supply)}}{V_{ripple\ (on\ output)}}$;
   measured at f = 1 kHz with $V_{ripple\ (supply\ max)}$ = 100 mV (peak-to-peak value).
   The supply voltage rejection ratio is >36 dB at f_{max} = 100 kHz.

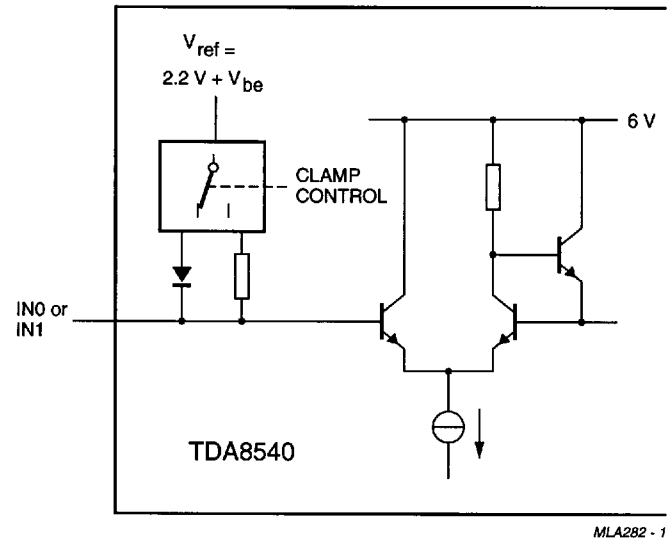


Fig.3 IN0 and IN1 inputs.

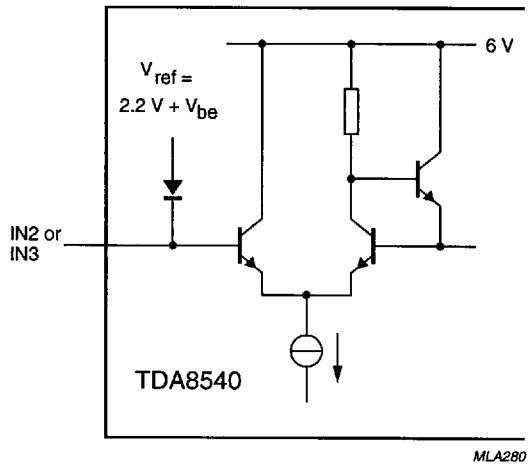


Fig.4 IN2 and IN3 inputs.

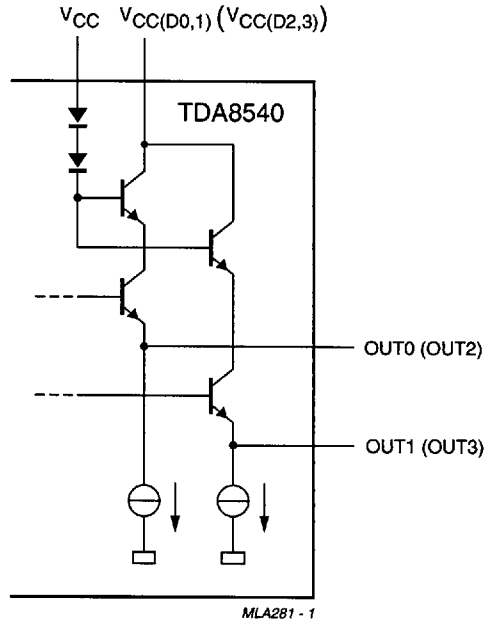
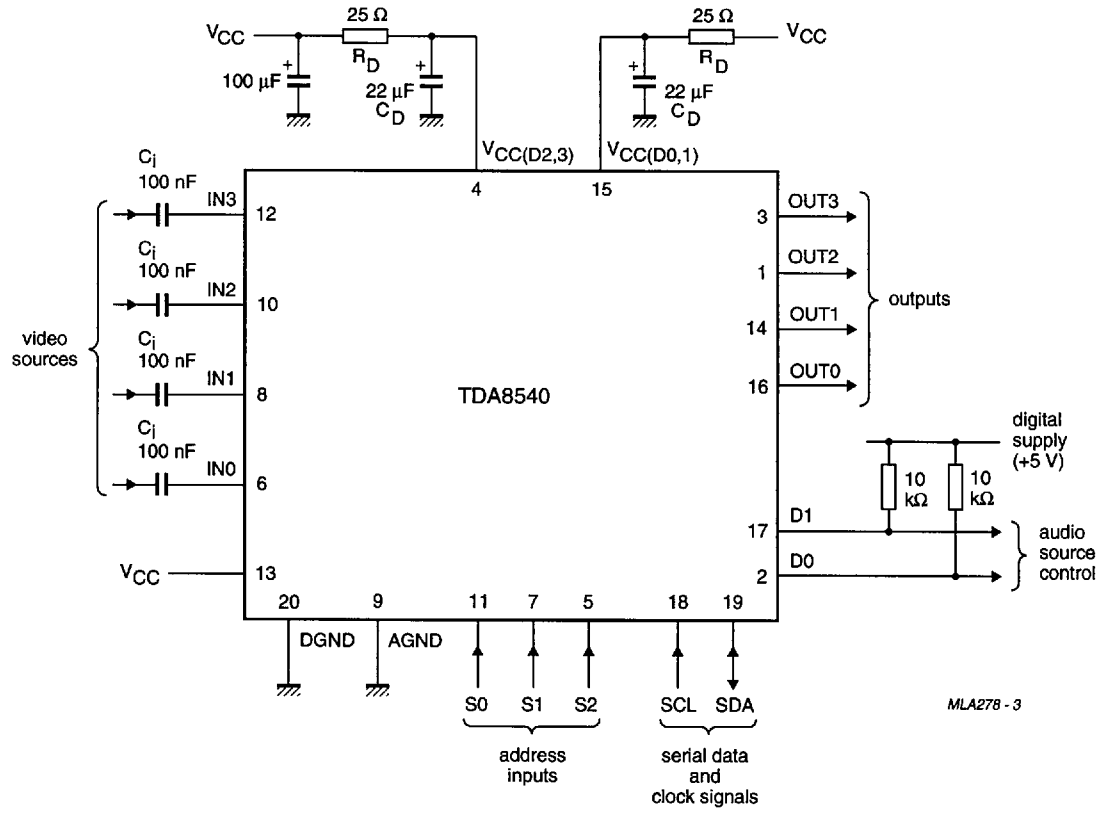


Fig.5 Driver output stage.

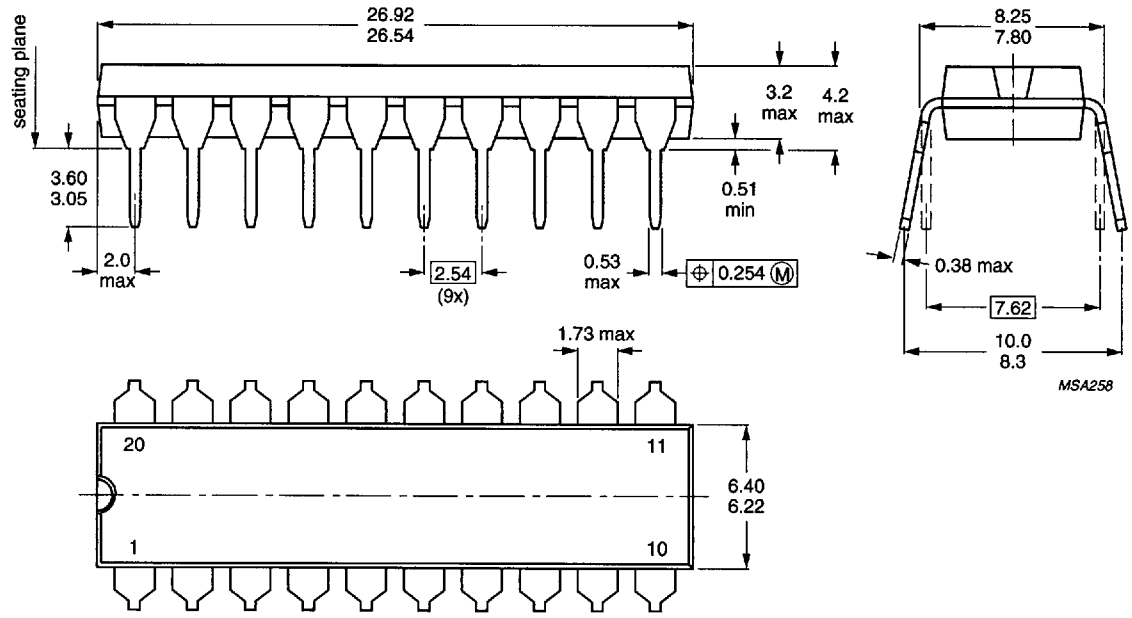
APPLICATION INFORMATION



V_{CC} = analog supply (+8 V).

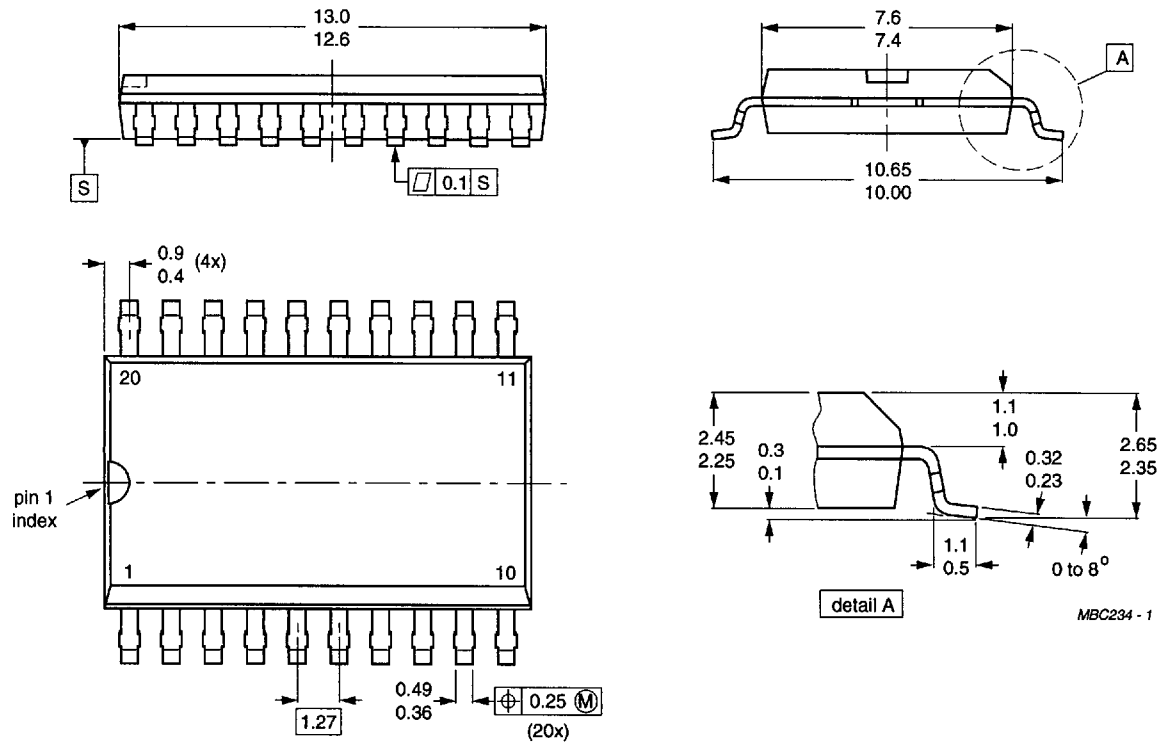
Fig.6 Application diagram.

PACKAGE OUTLINES



Dimensions in mm.

Fig.7 Plastic dual in-line package; 20 leads (300 mil); DIP20; SOT146-1.



Dimensions in mm.

Fig.8 Plastic small outline package; 20 leads; body width 7.5 mm (SO20; SOT163-1).

SOLDERING

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

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