CMOS 8–Bit Microcontrollers

TMP90C800N/TMP90C801N

TMP90C800F/TMP90C801F

1. Outline and Characteristics

The TMP90C800 is a high-speed advanced 8-bit microcontroller applicable to a variety of equipment.

With its 8-bit CPU, ROM, RAM, timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C800 allows the expansion of external memories for programs and data (up to 56K bytes). The function of TMP90C800 is exactly same as the TMP90C400 except the internal ROM/RAM size.

The TMP90C801 is the same as the TMP90C800 but without the ROM.

The TMP90C800N/801N is in a shrink Dual Inline Package (SDIP64-P-750).

The TMP90C800F/801F is in a Quad Flat package (QFP64-P-1420A)

The characteristics of the TMP90C800 include:

(1) Powerful instructions: 163 basic instructions, including Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions

(2) Minimum instruction executing time: 320ns (at 12.5MHz oscillation frequency)

(3) Internal ROM: 8K bytes (The TMP90C801 does not have a built-in ROM)

(4) Internal RAM: 256 bytes

(5) Memory expansion
External memory: 56K bytes

(6) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode

(7) 8-bit timers (4 channel): (2 external clock input)

(8) Port with zero-cross detection circuit (4 input)

(9) Input/Output ports (56 pins)
- Ports with programmable pull-up resistor (22 pins)
- Allows I/O selection on bit basis
- Multiplexer ports of address data bus

(10) Interrupt function: 7 internal interrupts and 3 external interrupts

(11) Micro Direct Memory Access (DMA) function (8 channels)

(12) Standby function (4 HALT modes)

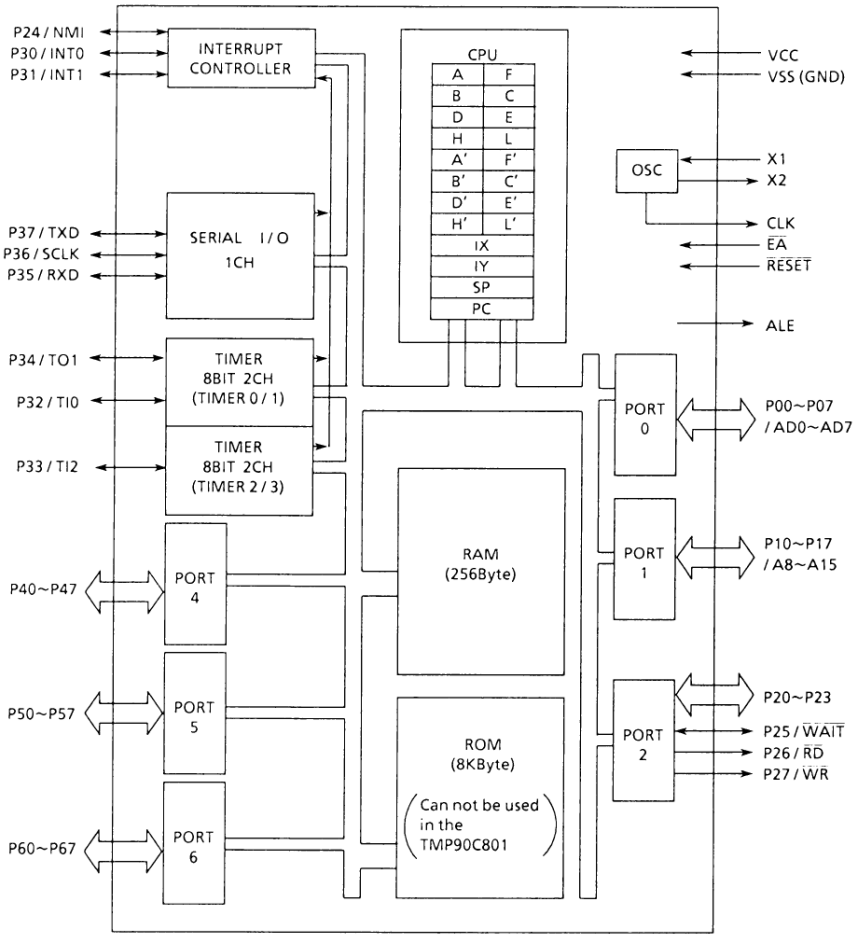


Figure 1. TMP90C800 Block Diagram

2. Pin Assignment and Functions

This section describes the assignment of input/output pins, their names and functions.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP90C800N/801N.

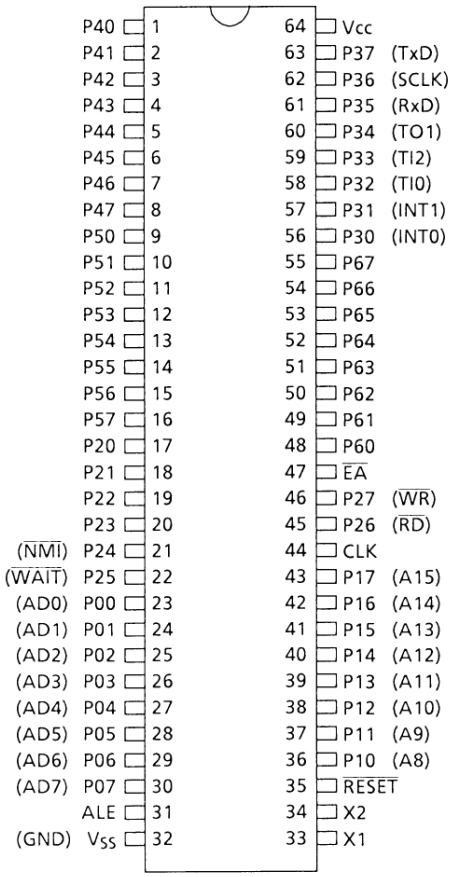


Figure 2.1 (1). Pin Assignment (Shrink Dual Inline Package)

Figure 2.1 (2) shows Pin Assignment of the TMP90C800F/ 801F.

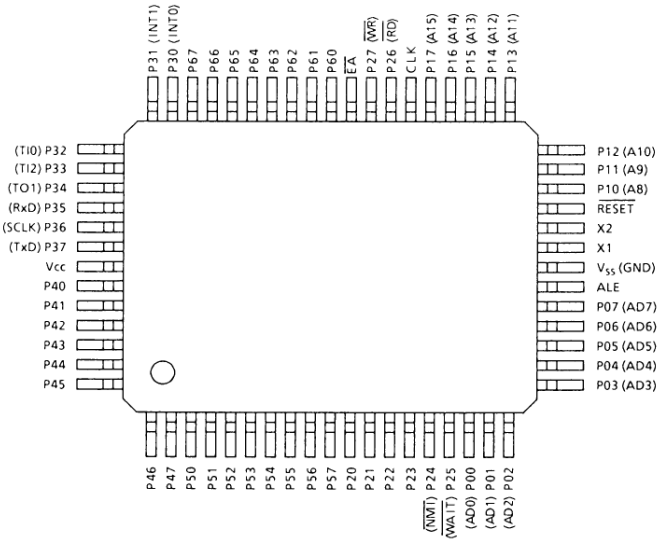


Figure 2.1 (2). Pin Assignment (Flat Package)

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00 ~ P07 /AD0 ~ AD7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Address/Data bus: Functions as 8-bit bidirectional address/data bus for external memory (For 401, fixed to address/data bus)
P10 ~ P17 /A8 ~ A15	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Address bus: Functions as address bus (upper 8 bits) by EXT1 set for external memory (For 401, fixed to address bus
P20 ~ P23	4	I.O	Port 20 ~ 23: 4-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
P24 /$\overline{\text{NMI}}$	1	I/O	Port 24: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Input	Non-maskable interrupt request pin: Falling edge interrupt register pin 
P25 /$\overline{\text{WAIT}}$	1	I/O	Port 25: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Input	Wait: Input pin for connecting slow speed memory of peripheral LSI
P26 /$\overline{\text{RD}}$	1	Output	Port 26: 1-bit output port
		Output	Read: Generates strobe signal for reading external memory (For 401, fixed to $\overline{\text{RD}}$)
P27 /$\overline{\text{WR}}$	1	Output	Port 27: 1-bit output port
		Output	Read: Generates strobe signal for writing into external memory (For 401, fixed to $\overline{\text{WR}}$)
P30 /INT0	1	I/O	Port 30: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Input	Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable) 
P31 /INT1	1	Input	Port 31: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
			Interrupt request pin 1: Rising edge interrupt request pin 
P32 /TI0	1	I/O	Port 32: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Input	Timer input 0: Counter input pin for Timer 0
P33 /TI2	1	Output	Port 33: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
			Timer input 2: Counter input pin for Timer 2

Table 2.2 Pin Names and Functions (2/2)

P35 /RxD	1	I/O	Port 35: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		I/O	Receive serial data
P36 /SCLK	1	I/O	Port 36: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Output	Serial clock output
P37 TxD	1	I/O	Port 37: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
		Output	Transmitter serial data
P40 ~ P47	8	I/O	Port 4: 8-bit I/O port that allows I/O selection on bit basis
P50 ~ P57	8	I/O	Port 5: 1-bit I/O port with a pull-up resistor that can be programmed, and allows selection of input/output on bit basis
P60 ~ P67	8	I/O	Port 6: 8-bit I/O port that allows I/O selection on bit basis
ALE	1	Output	Address latch enable signal: The negative edge ALE supplies an address latch timing on AD0 ~ A07 for external memory
$\overline{EA}$	1	Input	External access: Connects with V_{CC} pin in the TMP90C400 using internal ROM, and with GND pin in the TMP90C401 with no internal ROM
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is pulled up internally during resetting.
$\overline{RESET}$	1	Input	Reset: Initializes the TMP90C400/401 (Built-in pull-up resistor)
X1/X2	2	Input/Output	Pin for quartz crystal or ceramic resonator (1 ~ 12.5MHz)
V_{CC}	1	–	Power supply (+5V)
V_{SS}	1	–	Ground (0V)

3. Operation

This chapter describes the functions and the basic operations of the TMP90C400/401 in every block.

The function of TMP90C800 is exactly same as that of TMP90C400 except the internal ROM/RAM size. Refer to the TMP90C400 except the function which are not described this section.

3.1 CPU

The TMP90C800 includes a high performance 8-bit CPU. For the function of the CPU, see the book TLCS Series CPU Core Architecture concerning CPU operation.

3.2 Memory Map

The TMP90C800 supports a program memory of up to 56K bytes.

The program and data memory may be assigned to the address space from 0000H to FFFFH.

(1) Internal ROM

The TMP90C800 internally contains an 8K-byte ROM. The address space from 0000H to 1FFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0010H to 005FH in this internal ROM area are used for the entry area for the interrupt processing.

The TMP90C801 does not have a built-in ROM; therefore, the address space 0000H to 1FFFH is used as external memory space.

(2) Internal RAM

The TMP90C800 also contains a 256-byte RAM, which is allocated to the address space from FF80H to FF7FH. The CPU allows the access to a certain RAM area (FF00H to FF7FH, 256 bytes) by a short operation code (opcode) in a “direct addressing mode”.

The addresses from FF20H to FF5FH in this RAM area can be used as parameter area for micro DMA processing (and for any other purposes when the micro DMA function is not used).

(3) Internal I/O

The TMP90C800 provides a 32-byte address space as an internal I/O area, whose addresses range from FF80H to FF9FH. This I/O area can be accessed by the CPU using a short opcode in the “direct addressing mode”.

Figure 3.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

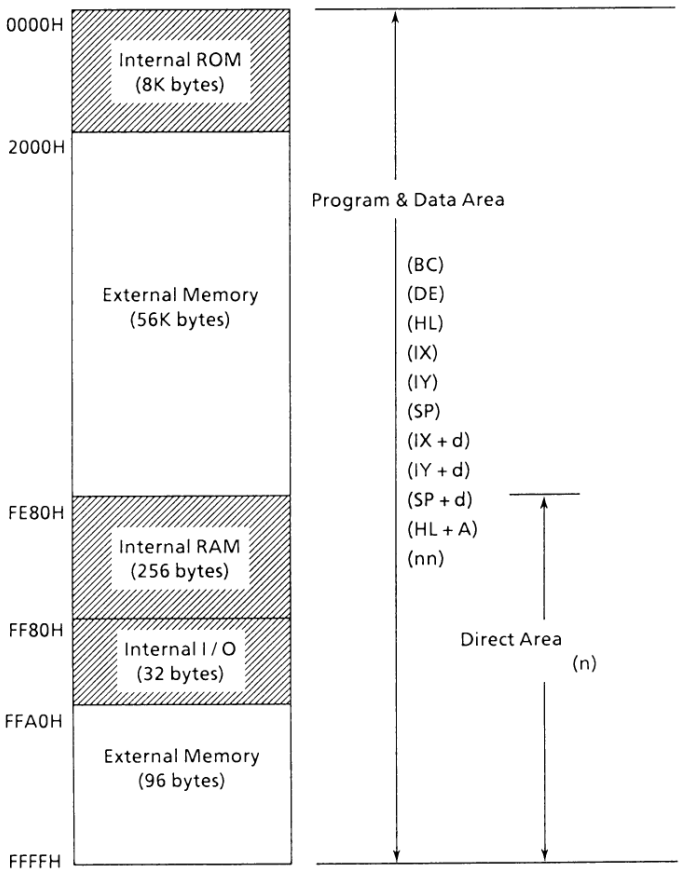


Figure 3.2 (a). Memory Map of TMP90C800

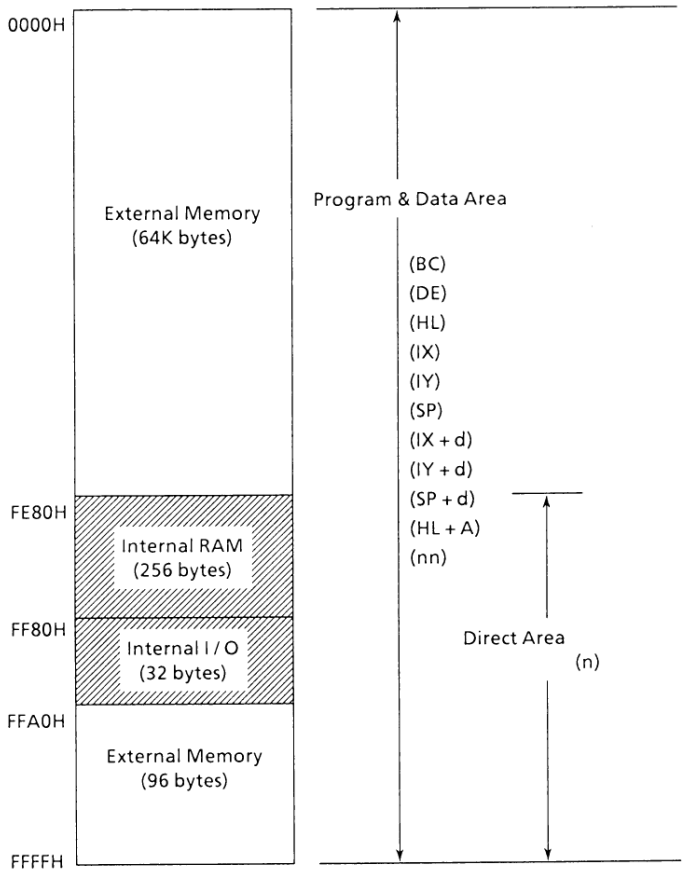


Figure 3.2 (b). Memory Map of TMP90C801

4. Electrical Characteristics (Preliminary)

TMP90C800N/TMP90C800F/
TMP90C801N/TMP90C801F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 ~ + 7	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-40 ~ 85	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P4, P5, P6	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, $\overline{NMI}$	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input High Voltage (P0)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P1, P2, P3, P4, P5, P6	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, $\overline{NMI}$	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH3}	$\overline{EA}$	V_{CC} - 0.3	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	–	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	-0.1	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 6 (Typ)	40 5 15	mA mA mA	tosc = 10MHz (25%Up @12.5MHz)
	STOP (TA = -40 ~ 85°C) STOP (TA = 0 ~ 50°C)	0.05 (Typ)	50 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP)	2 RAM BACK UP	6	V	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, $\overline{NMI}$	0.4	1.0 (Typ)	V	–

Note: I_{DAR} is guaranteed for a total of up to 8 optional ports.

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	Oscillation cycle (= x)	80	1000	100	–	80	–	ns
t_{CYC}	CLK Period	4x	4x	400	–	320	–	ns
t_{WH}	CLK High width	2x - 40	–	160	–	120	–	ns
t_{WL}	CLK Low width	2x - 40	–	160	–	120	–	ns
t_{AL}	A0 ~ 7 effective address→ALE fall	0.5x - 15	–	35	–	25	–	ns
t_{LA}	ALE fall →A0 ~ 7 hold	0.5x - 15	–	35	–	25	–	ns
t_{LL}	ALE Pulse width	x - 40	–	60	–	40	–	ns
t_{LC}	ALE fall $\overline{RD}/\overline{WR}$ fall	0.5x - 30	–	20	–	10	–	ns
t_{CL}	$\overline{RD}/\overline{WR}$ →ALE rise	0.5x - 20	–	30	–	20	–	ns
t_{ACL}	A0 ~ 7 effective address →$\overline{RD}/\overline{WR}$ fall	x - 25	–	75	–	55	–	ns
t_{ACH}	Upper effective address →$\overline{RD}/\overline{WR}$ fall	1.5x - 50	–	100	–	70	–	ns
t_{CA}	$\overline{RD}/\overline{WR}$ fall →Upper address hold	0.5x - 20	–	30	–	20	–	ns
t_{ADL}	A0 ~ 7 effective address →Effective data input	–	3.0x - 35	–	265	–	205	ns
t_{ADH}	Upper effective address →Effective data input	–	3.5x - 55	–	295	–	225	ns
t_{RD}	$\overline{RD}$ fall →Effective data input	–	2.0x - 50	–	150	–	110	ns
t_{RR}	$\overline{RD}$ Pulse width	2.0x - 40	–	160	–	120	–	ns
t_{HR}	$\overline{RD}$ rise →Data hold	0	–	0	–	0	–	ns
t_{RAE}	$\overline{RD}$ rise→ Address enable	x - 15	–	85	–	65	–	ns
t_{WW}	WR pulse width	2.0x - 40	–	160	–	120	–	ns
t_{DW}	Effective data→$\overline{WR}$ rise	2.0x - 50	–	150	–	110	–	ns
t_{WD}	WR rise→Effective data hold	0.5x - 10	–	40	–	30	–	ns
t_{ACKH}	Upper address→CLK fall	2.5x - 50	–	200	–	150	–	ns
t_{ACKL}	Lower address →CLK fall	2.0x - 50	–	150	–	110	–	ns
t_{CKHA}	CLK fall→Upper address hold	1.5x - 80	–	70	–	40	–	ns
t_{CCK}	$\overline{RD}/\overline{WR}$→CLK fall	x - 25	–	75	–	55	–	ns
t_{CKHC}	CLK fall→$\overline{RD}/\overline{WR}$ rise	x - 60	–	40	–	20	–	ns
t_{DCK}	Valid data CLK fall	x - 50	–	50	–	30	–	ns
t_{CWA}	$\overline{RD}/\overline{WR}$ fall→Valid $\overline{WAIT}$	–	x - 40	–	60	–	40	ns
t_{AWAL}	Lower address →Valid $\overline{WAIT}$	–	2.0x - 70	–	130	–	90	ns
t_{WAH}	CLK fall →Valid $\overline{WAIT}$ hold	0	–	0	–	0	–	ns
t_{AWAH}	Upper address →Valid $\overline{WAIT}$	–	2.5x - 70	–	180	–	130	ns
t_{CPW}	CLK fall →Port Data Output	–	x + 200	–	300	–	280	ns
t_{PRC}	Port Data Input →CLK fall	200	–	200	–	200	–	ns
t_{CPR}	CLK fall →Port Data hold	100	–	100	–	100	–	ns

AC Measuring Conditions

- Output level: High 2.2V/Low 0.8V, C_L = 50pF
  (However, CL = 100pF for AD0 ~ 7, A8 ~ 15, ALE, $\overline{RD}$, $\overline{WR}$)
- Input level: High 2.4V/Low 0.45V (AD0 ~ AD7)
  High 0.8V_{CC}/Low 0.2V_{CC} (excluding AD0 ~ AD7)

4.4 Zero-Cross Characteristics

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p-p
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	kHz

4.5 Serial Channel Timing-I/O Interface Mode

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
CL = 50pF TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	Serial Port Clock Cycle Time	8x	–	800	–	640	–	ns
t_{OSS}	Output Data Setup SCLK Rising Edge	6x - 150	–	450	–	330	–	ns
t_{OHS}	Output Data Hold After SCLK Rising Edge	2x - 120	–	80	–	40	–	ns
t_{HSR}	Input Data Hold After SCLK Rising Edge	0	–	0	–	0	–	ns
t_{SRD}	SCLK Rising Edge to Input DATA Valid	–	6x - 150	–	450	–	330	ns

4.6 8-bit Event Counter

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

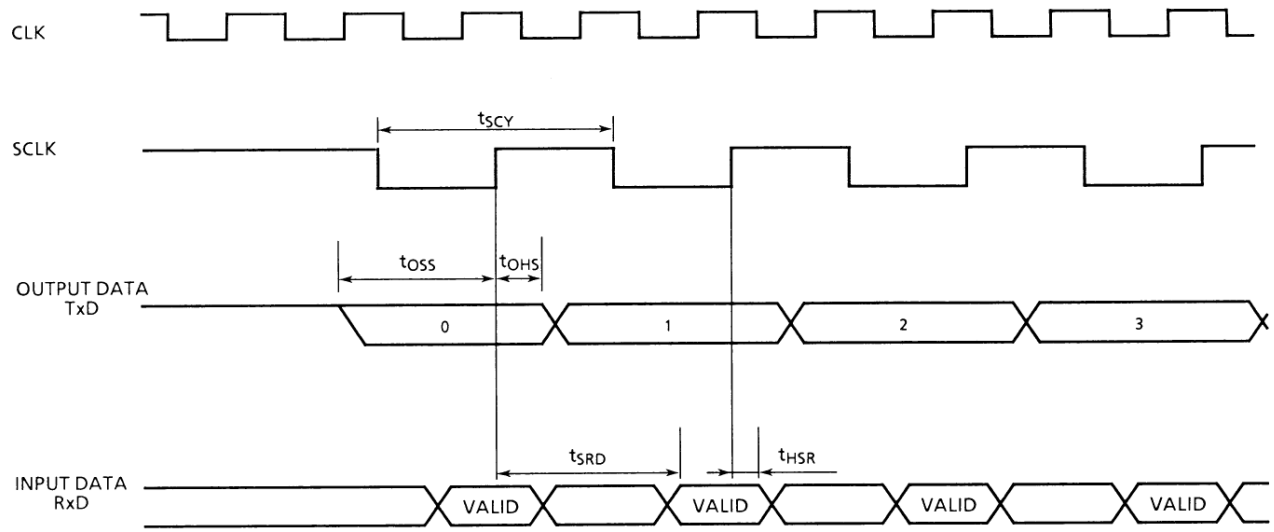
Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	TI2 clock cycle	8x + 100	–	900	–	740	–	ns
t_{VCKL}	TI2 Low clock pulse width	4x + 40	–	440	–	360	–	ns
t_{VCKH}	TI2 High clock pulse width	4x + 40	–	440	–	360	–	ns

4.7 Interrupt Operation

V_{CC} = 5V ± 10% TA = -40 ~ 85°C (1 ~ 10MHz)
TA = -20 ~ 70°C (1 ~ 12.5MHz)

Symbol	Parameter	Variable		10MHz Clock		12.5MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 Low level pulse width	4x	–	400	–	320	–	ns
t_{INTAH}	$\overline{NMI}$, INT0 High level pulse width	4x	–	400	–	320	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width	8x + 100	–	900	–	740	–	ns
t_{INTBH}	INT1, INT2 High level pulse width	8x + 100	–	900	–	740	–	ns

4.8 I/O Interface Mode Timing



4.9 Timing Chart