OPTi-386/486WB EISA Chipset

82C681/82C682/82C686/82C687 (EBC/MCC/ISP/DBC)

DATABOOK

Preliminary

Version 1.3

Disclaimer

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TABLE OF CONTENTS

1. OVERVIEW
    1.1 Introduction
    1.2 Features
    1.3 System Block Diagram

2. MEMORY/CACHE CONTROLLER (MCC)
    2.1 Features
        2.1.1 CPU Selectability
        2.1.2 Clock and Reset
        2.1.3 Cache Subsystem
        2.1.4 CPU Burst Mode Control
        2.1.5 Interleaved Cache
        2.1.6 Cache Cycle Descriptions
        2.1.7 RAM Requirements
        2.1.8 Programmable Non-Cacheable Regions
        2.1.9 RAM Subsystem
        2.1.10 System BIOS ROM
        2.1.11 Shadow RAM
        2.1.12 Refresh Logic
    2.2 MCC Pin Description
        2.2.1 Clock and Reset
        2.2.2 Address/Status
        2.2.3 Host Interface
        2.2.4 Arbiter
        2.2.5 Bus Interface
        2.2.6 I/O Decode
        2.2.7 DRAM Interface
        2.2.8 Cache Interface
        2.2.9 Data/Parity
        2.2.10 EISA Timing Signals
        2.2.11 Ground and VCC
    2.3 Register Description
    2.4 AC/DC Specifications
        2.4.1 Absolute Maximum Ratings
        2.4.2 DC Characteristics
        2.4.3 AC Specification Tables
    2.5 MCC Pinout
        2.5.1 Numerical Pin Cross Reference
        2.5.2 Alphabetical Pin Cross Reference

3. EISA BUS CONTROLLER (EBC)
- 3.1 Features
  - 3.1.1 Clock Generation
  - 3.1.2 Reset Control
  - 3.1.3 Host Bus Interface
  - 3.1.4 EISA/ISA Bus Interface
  - 3.1.5 Data/Address Control
  - 3.1.6 EISA Bus Compatibility
  - 3.1.7 Refresh
  - 3.1.8 Testability
- 3.2 EBC Pin Description
  - 3.2.1 Host Bus Interface
  - 3.2.2 Host-Bus/Numeric Interface
  - 3.2.3 ISP/MCC Interface
  - 3.2.4 ISA Bus Interface
  - 3.2.5 EISA-Bus Interface
  - 3.2.6 Clocks
  - 3.2.7 Reset Control
  - 3.2.8 Data Control
  - 3.2.9 Address Control
  - 3.2.10 Register Access
  - 3.2.11 Ground and VCC
- 3.3 Register Description
- 3.4 AC/DC Specifications
  - 3.4.1 Absolute Maximum Ratings
  - 3.4.2 DC Characteristics
  - 3.4.3 AC Specification Tables
- 3.5 EBC Pin-out
  - 3.5.1 Numerical Pin Cross Reference
  - 3.5.2 Alphabetical Pin Cross Reference

4. INTEGRATED SYSTEM PERIPHERAL (ISP)
- 4.1 Features
  - 4.1.1 Timer/Counter
  - 4.1.2 NMI/Timeout Logic
  - 4.1.3 Interrupt Controller
  - 4.1.4 DMA/Refresh Controller
  - 4.1.5 System Arbiter
  - 4.1.6 Data Buffer
  - 4.1.6 Testability
- 4.2 ISP Pin Description
  - 4.2.1 Bus Interface
  - 4.2.2 Timer
  - 4.2.3 NMI/Timeout Logic
  - 4.2.4 Interrupts
  - 4.2.5 DMA/Refresh
  - 4.2.6 I/O Decodes
  - 4.2.7 System Arbiter
  - 4.2.8 Ground and VCC
- 4.3 Register Description

4.4 AC/DC Specifications
4.4.1 Absolute Maximum Ratings
4.4.2 DC Characteristics
4.4.3 AC Specification Tables
4.5 ISP Pin-out
4.5.1 Numerical Pin Cross Reference
4.5.2 Alphabetical Pin Cross Reference

5. DATA BUS CONTROLLER (DBC)
5.1 Features
5.1.1 Data Bus Conversion
5.1.2 Parity Generation/Detection Logic
5.1.3 AEN Generation
5.1.4 Fast Warm Reset
5.1.5 I/O Decode
5.1.6 General Purpose Chip Selects
5.1.7 Configuration Non-Volatile-Memory (NVM)
5.1.8 General Purpose Single-bit I/O port
5.1.9 EISA ID Registers
5.1.10 Testability
5.2 DBC Pin Description
5.2.1 Data Bus Interface
5.2.2 Data Buffer Control
5.2.3 Parity and Control
5.2.4 I/O Address and Control
5.2.5 Fast CPU Reset Control
5.2.6 I/O Decode
5.2.7 Port Control
5.2.8 Ground and VCC
5.3 Register Description
5.4 AC/DC Specifications
5.4.1 Absolute Maximum Ratings
5.4.2 DC Characteristics
5.4.3 AC Specification Tables
5.5 DBC Pin-out
5.5.1 Numerical Pin Cross Reference
5.5.2 Alphabetical Pin Cross Reference

LIST OF FIGURES

System Block Diagram
MCC Block Diagram
EBC Block Diagram
ISP Block Diagram
DBC Block Diagram
MCC Pin-out
EBC Pin-out
ISP Pin-out
DBC Pin-out
EBB Pin-out
Mechanical Dimensions

1. OPTi EISA CHIPSET OVERVIEW

1.1 Introduction

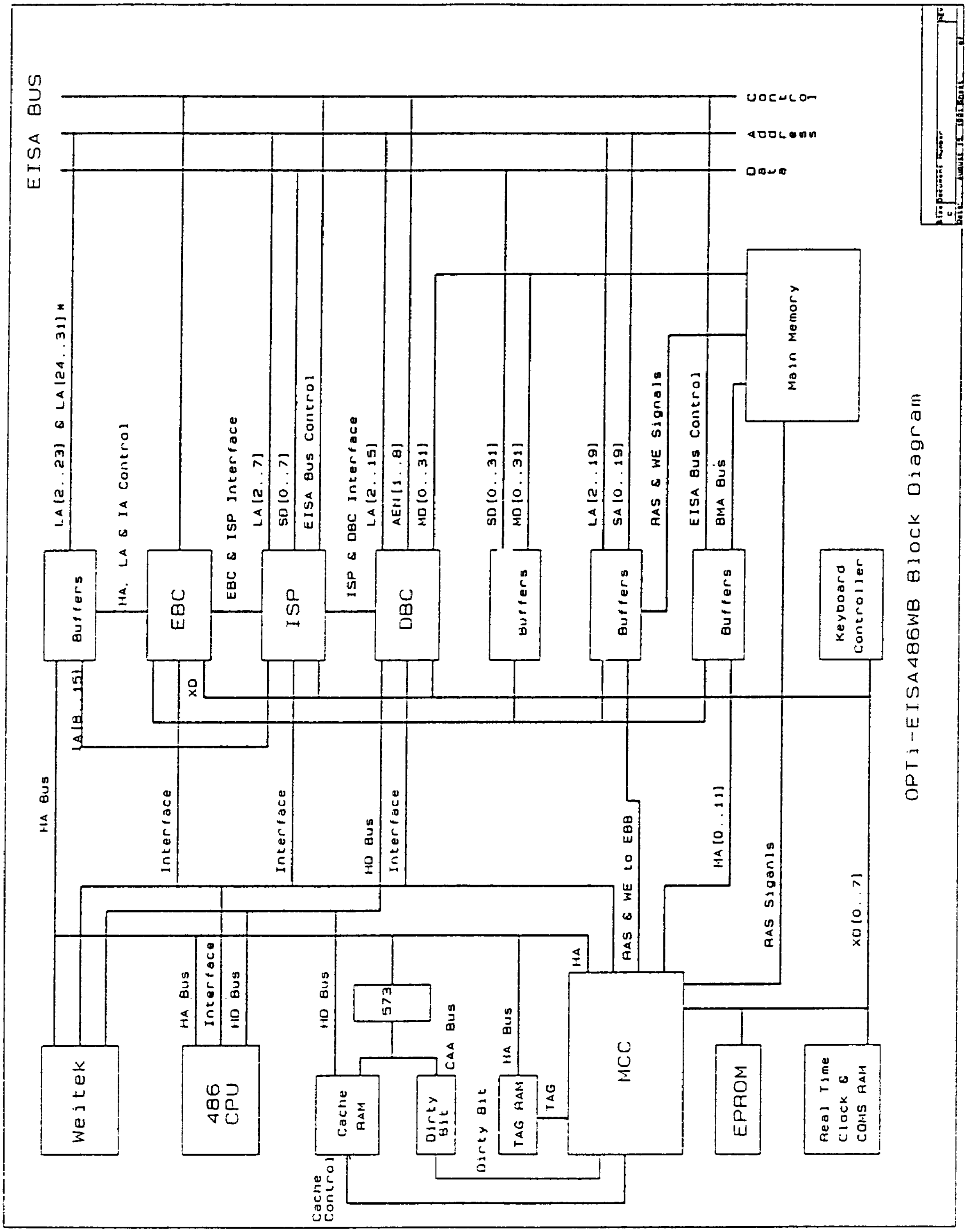
The OPTi EISA Core logic chipset consists of four 160-pin PFPs (Plastic-Flat Packages) and offers optimal performance for high-end 486/386 based EISA systems. The four chips include the Memory/Cache Controller (MCC), the EISA Bus Controller (EBC), the Integrated System Peripheral (ISP), and the Data Bus Controller (DBC). The OPTi EISA chipset is designed for systems running at 20MHz, 25MHz, 33MHz, 40MHz and 50MHz.

1.2 Features

The OPTi EISA chipset includes the following features:

* Supports 80386/80486SX/80486 CPUs
* Supports 80387/3167/4167/80487SX numeric coprocessors
* 20/25/33/40/50 MHz clock
* 64/128/256/512 KBytes of write back cache
* Supports 2-1-1-1 cache burst cycle as well as 3-1-1-1, 2-2-2-2 and 3-2-2-2 cycles
* Fast on-chip comparitor determines cache hit or miss
* Optional 0 or 1 wait state for Cache-Write-Hit
* Three programmable non-cachable-regions
* Optional caching of shadowed Video BIOS
* Supports 4 banks of local DRAM yielding systems ranging from 4MB to 256MB of host memory
* Supports shadowed RAM
* CAS# before RAS# refresh reduces power consumption
* Supports hidden refresh
* Supports Host and EISA burst modes to/from host memory
* Fast CPU warm reset and A20 control
* Glueless integration of all mandatory devices and EISA slots

1.3 System Block Diagram



2. 82C682, OPTi MEMORY/CACHE CONTROLLER (MCC)

2.1 FEATURES

The OPTi Memory/Cache Controller (MCC) is a 160-pin PFP (Plastic Flat Package) device. It controls accesses to the local memory subsystem from the 486/386 processor, EISA/ISA masters and DMA devices. The memory subsystem consists of up to 4 banks of 1M/4M/16M x36 DRAM using optional hidden refresh, and up to 512kB of write-back cache. The cache may be two-way interleaved for 486 systems

The MCC includes the following features:

* 160-pin Plastic Flat package
* Supports 486 / 486SX / and 386 CPUs
* Integrated write-back cache controller with tag comparator
* Supports cache sizes of 64kB, 128kB, 256kB, or 512kB
* 486 and EISA burst mode control
* Provides control registers for shadowing/caching memory between 640k to 1MB
* Supports 1 through 4 banks of 1Mx36, 4Mx36 or 16Mx36 DRAM.
* Provides flexible DRAM configurations from a minimum of 4MB to a maximum of 256MB
* Supports 80ns fast page mode DRAM's at 25, 33, 40 and 50 MHz
* Supports both normal and hidden refresh
* Three programmable non-cacheable regions supported.
* Internal Fast A20 mask register

2.1.1 CPU Selectability

An input strapping pin (386/486#) to the MCC determines whether it will operate in 386 mode or in 486/486sx mode. 486 type systems must tie this pin to ground and 386 systems should leave this pin unconnected (a weak pull-up resistor will keep this input high when left unconnected).

2.1.2 Clock and Reset

The MCC has two high frequency clock inputs, CLK and CLK2. CLK2 is used for internal cache timing control. CLK is a master single-phase clock which is used to drive all host CPU synchronous signals and the MCC's internal state machine. The motherboard signal RST# is driven by the EBC to reset the MCC.

2.1.3 Cache Subsystem

An integrated write-back cache controller boosts the local memory subsystem's overall performance by caching writes as well as reads. Cache sizes of 64kB, 128kB, 256kB, and 512kB are all supported. The MCC operates in non-pipeline mode with a 16-byte line size (optimized to match a 486 burst fill cycle) in order to simplify the motherboard design without increasing cost or degrading performance. For 486 systems, this secondary cache operates independently and in addition to the CPU's internal cache.

A built-in tag comparator reduces board real estate and maintains high cache performance. The comparator internally detects a cache hit by comparing the addressed memory location high order address with the tag bits of the current cache entry. When a match is detected, and the location is cacheable, a cache-hit cycle takes place. If the comparator does not detect a match or a non-cacheable location is accessed (based on the internal non-cacheable region registers or the shadow control registers), the current cycle is a cache-miss.

A "dirty bit" corresponds to each tag entry to indicate whether the data in the cache has been modified since it was loaded from memory. This allows the MCC to determine whether the data in memory is "stale" and needs to be updated before a new memory location overwrites the currently indexed cache entry. The writeback cycle causes an entire cache line (16 bytes) to be written back to memory followed by a line burst from the new memory location into the cache and CPU.

2.1.4 CPU Burst Mode Control

The cache/DRAM controller in the MCC insures that data is burst into the CPU whenever the 486 requests an internal cache line fill (read cycles to cacheable memory not currently in the internal cache). The secondary cache provides data on read-hits and the DRAM provides data during read-misses. For secondary cache read-hits, the MCC asserts BRDY# (Burst Ready) in the middle of the first T2 state when zero wait states are required and at the middle of the second T2 state when one wait state is required. BRDY# is asserted after the cache memory is updated for secondary cache read-misses. Once asserted, BRDY# stays active until BLAST# (Burst Last) is detected. BRDY# is never active during DMA and EISA master cycles.

The MCC also supports bursting across the EISA bus to/from main memory by other bus masters by sampling the MSBURST# input from the bus.

2.1.5 Interleaved Cache:

In 486 systems, the MCC allows the cache SRAMs to be interleaved in order to improve burst performance without having to use faster SRAMs. This interleaving is automatically selected whenever two banks of SRAMs are installed (64kB and 256kB systems).

2.1.6 Cache Cycle Descriptions:

The following cache cycles are possible with the MCC:

Cache-Read-Hit:

CPU

The cache memory provides data to the CPU. For 486 systems, the MCC follows the CPU's burst protocol in order fill the processor's internal cache line.

EISA/ISA/DMA

The cache memory provides the data.

Cache-Read-Miss (Dirty bit negated):

CPU

The MCC does not need to update DRAM with the cache's current data because that data is unmodified. The cache controller asserts TAGWE#, causing the tag SRAMs to update their address information and asserts CAWE#, causing the data SRAMs to store new information from memory. This new data is presented to the CPU (following burst protocol for 486 systems).

EISA/ISA/DMA

DRAM provides the data, the cache is bypassed.

Cache-Read-Miss (Dirty bit asserted)

CPU

The cache controller must first update memory with data from the cache location that is going to be overwritten. The controller writes the 16-byte line from cache memory to the DRAM, then reads the new line from DRAM into cache memory and deasserts the DIRTY bit. The MCC asserts TAGWE#, CAWE#[3:0] and DIRTYWE#.

EISA/ISA/DMA

DRAM provides the data, the cache is bypassed.

Cache-Write-Hit.

CPU

Because this is a write-back cache , the cache controller does not need to update the slower DRAM memory. Instead, the controller updates the cache memory and sets the DIRTY bit. (DIRTY may already be set, but that does not affect this cycle). The ability to cache write-hit cycles boosts performance over write-through caches, especially on a string of consecutive write-hits, because each write cycle completes as fast as the SRAM can respond without having to wait for a slower DRAM cycle to complete.

EISA/ISA/DMA

Data is written to BOTH the cache and DRAM. EADS# is asserted to the 486 to invalidate its internal cache line in order to maintain cache coherency. The dirty bit is unchanged.

Cache-Write-Miss

CPU

The cache controller bypasses the cache entirely and writes the line directly into DRAM. DIRTY is unchanged.

EISA/ISA/DMA

The cache controller bypasses the cache entirely and writes the line directly into DRAM. DIRTY is unchanged.

2.1.7 SRAM requirements

The following table summarizes the cache SRAM requirements of the MCC:

Cache Size	Inter-leaved	DIRTY bit	Tag Field Address/ Tag RAM size	Cache RAM Address /Cache RAMs	Cachable Main Memory
64kB	Yes	4kx1	A24 - A16 4Kx9	A15 - A4 8 - 8Kx8	32MB
128kB	No	8kx1	A25 - A17 8Kx9	A16 - A4 4 - 32Kx8	64MB
256kB	Yes	16kx1	A26 - A18 16Kx9	A17 - A4 8 - 32Kx8	128MB
512kB	No	32kx1	A27 - A19 32Kx9	A18 - A4 4 - 128Kx8	256MB

2.1.8 Programmable Non-Cacheable regions

Up to three independent areas of memory can be defined as non-cacheable by the MCC. This is accomplished by programming the Non-Cacheable-Area index registers (NCA0, NCA1, NCA2) with a starting address and block size for each region selected. Allowable block sizes range from 64kB to 512kB.

2.1.9 DRAM Subsystem

The MCC supports up to 4 banks of page-mode local memory. 1M, 4M, or 16M DRAM devices may be used. Note that 16M memory can't mix with 4M/1M memory. The memory configuration is programmable through two memory configuration registers in the MCC (C33h and C34h). The following table illustrates the configurations supported.

Bank 0	Bank 1	Bank 2	Bank 3	Total
1M	X	X	X	4M
1M	1M	X	X	8M
1M	1M	1M	X	12M
1M	1M	1M	1M	16M
4M	X	X	X	16M
1M	4M	X	X	20M
1M	1M	4M	X	24M
1M	4M	1M	X	24M
1M	1M	4M	1M	28M
1M	4M	1M	1M	28M
4M	4M	X	X	32M
1M	4M	4M	X	36M
4M	4M	1M	X	36M
1M	1M	4M	4M	40M
1M	4M	4M	1M	40M
4M	4M	1M	1M	40M
4M	4M	4M	X	48M
1M	4M	4M	4M	52M
4M	4M	4M	1M	52M
4M	4M	4M	4M	64M
16M	X	X	X	64M
16M	16M	X	X	128M
16M	16M	16M	X	192M
16M	16M	16M	16M	256M

2.1.10 System BIOS ROM

To reduce the system chip count and form factor, the MCC supports 8-bit ROM cycles so that a single EPROM can be used for the system BIOS. This EPROM resides on the XD bus and is controlled by ROMCS0#. The system BIOS is typically shadowed or cached so that there is no performance penalty associated with 8-bit ROM cycles.

A second ROM chip select exists (ROMCS1#) which can be programmed according to the values defined in the Shadow RAM/ROM configuration registers.

2.1.11 Shadow RAM/ROM

Because DRAM accesses are much faster then EPROM accesses, the MCC provides shadow RAM capability to enhance system performance. Data is read from EPROM, then write-protected, into a dedicated area in DRAM. Accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h to FFFFFh. 16kB granularity is provided for the address range C0000h to EFFFFh while the 64kB range from F0000h - FFFFFh (the location of system BIOS) is shadowable as an entire segment.. Shadow control is provided by internal index registers in the MCC.

Additionally, these registers can selectively set the video and system BIOS areas as cacheable.

2.1.12 Refresh Logic

Refresh cycles occur on both the EISA bus and the local memory bus. The MCC implements refresh cycles to the local DRAMs using CAS before RAS timing. This provides the advantage of eliminating the refresh counter in the MCC while allowing the EISA bus refresh address to be decoupled from the local memory refresh address. Additionally, CAS before RAS has a lower power consumption than RAS only refresh which is important when dealing with large memory arrays. CAS before RAS timing is used for both normal and hidden refresh to local memory.

The MCC supports both normal and hidden refresh. "Normal" refers to the classical refresh implementation that places the CPU in hold while a refresh cycle takes place to both the local DRAM and any EISA bus memory. This is the default condition at power-up (and is useful for debugging purposes). However, hidden refresh is superior, and recommended over normal refresh, because it does not suffer from the performance restriction of forcing the CPU into its hold state. Instead, when a hidden refresh cycle takes place, the EISA bus is decoupled from the CPU. Similarly, the MCC will perform a refresh cycle to the DRAMs independently of the CPU. The CPU continues to execute instructions during this time. As long as the CPU does not try to access local memory or the EISA bus during a hidden refresh cycle, refresh is transparent to the CPU. ie: The CPU can continue to execute out of its internal and secondary caches as well as perform internal instructions during hidden refresh without any loss in performance due to refresh arbitration. In the event that a local memory or an EISA bus access is required during hidden refresh, the CPU cycle will have wait states added until the resource becomes available.

2.1.13 Fast A20 Mask

The MCC provides an internal software index register to speed up the implementation of the A20 Mask output. This internal Fast A20 mask bit (Reg C30h<0>) is internally OR'd with the keyboard controller's GATEA20 input to generate A20M#. A20M# is used directly by the 486 because of its internal cache. 386 systems require external A20 masking which is accomplished by connecting this output to the A20M# input of the EBC.

2.1.14 Testability

I/O configuration register C30h<3:2> contains a 2-bit read only value that indicates the revision level of the MCC. This allows the revision level of the MCC to be verified by software.

The MCC includes a tristate test mode to enhance board level testability/manufacturability. When this test mode is entered, all outputs and bidirectional pins become tristated, allowing electrical isolation between the MCC and signals on the PCB.

At the trailing edge of the reset signal (RST#) the MCC samples two pins to determine whether the tristate test mode should be entered. GT1M#/TMOD# must be low and GATEA20/TSEL must be high *at this sample point* to guarantee entering this test state.

The following table illustrates the test function options at the RST# sample point.:

GT1M#/ TMOD#	GATEA20/ TSEL	Function
Low	Low	Reserved
Low	High	Tristate Test Mode
High	X	Normal Operation

2.2 MCC PIN DESCRIPTION

2.2.1 Clock and Reset

Pin Name	Type	Pin No.	Description
CLK	I	21	***Clock.*** Master single-phase CPU clock driven from an external clock-generator circuit. In 486 based systems, it is the same signal that the CPU receives. In 386 systems, it is the single-phase version (half the frequency) of the CPU clock.
CLK2	I	29	***Clock2.*** This input is driven from an external oscillator circuit without any external division. In systems at or below 33MHz, this clock signal input is twice the CPU's rated frequency. This is the same clock signal that drives the CPU in 386 systems. CLK2 is used for CAWE[3:0]# generation if the cache's Early Write Enable feature is turned on (Reg C31h<0> is set).
RST#	I	11	***Reset.*** RST# is an input from the EBC that resets the MCC (this same reset signal is also connected to the ISP, DBC, and 8042). The EBC asserts this signal based on powergood and reset switch functions.

2.2.2 Address/Status

Pin Name	Type	Pin No.	Description
HA[31:2]	I	76-71, 69-62, 60-51, 49-44	***Host Address Bus.*** Connected to the Host CPU A[31:2] bus. The MCC uses these 30 address lines for internal memory decoding and to generate the memory address bus (MA[11:0]).and the low order cache addresses (CAA3_[1:0], CAA2). The HA[31:2] bus is also used to determine all MCC internal register decodes.
GATEA20/ TSEL	I	27	***GATEA20 or Test Mode Select.*** This input pin serves two functions. Normally, it serves as the GATEA20 input from the keyboard controller (Output P21 of the 8042). This input , along with the internal Fast GATEA20 register (Reg C30h<0>), is used to generate A20M#. The second function of this pin is to allow the MCC to enter its Tristate test mode. The MCC will enter this test mode when GATEA20/TSEL is sampled High AND GT1M#/TMOD# is sampled low at the trailing edge of RST#.
A20M#	O	39	***A20 Mask.*** This output determines whether Host Address A20 should be forced low (to emulate the address wraparound at 1MB on the 8086). 486 based systems receive this signal directly (because of their internal cache). 386 systems require the masking to take place externally, so for these systems, A20M# is connected to the A20M# input of the EBC.
HBE[3:0]#	I	38-35	***Host Byte Enables [3:0].*** Connected to Host CPU BE[3:0]#. These signals determine valid bytes during DRAM/cache writes and MCC internal register accesses.
HM/IO#	I	42	***Host Memory / IO#.*** Connected to Host CPU M/IO#. This is sampled at the same time as HA[31:2]. This signal is not used by ISA Masters.
HD/C#	I	34	***Host Data / Control#.*** Connected to Host CPU D/C#. This is sampled at the same time as HA[31:2].
HW/R#	I	41	***Host Write / Read#.*** Connected to ISP & Host CPU W/R#. This is sampled at the same time as HBE[3:0]# except for ISA masters, when it is not used.

2.2.3 Host Interface

Pin Name	Type	Pin No.	Description
386/486#	I	155	***CPU Select.*** Hardware strapping pin to distinguish between 386 and 486 systems. Tie low to indicate a 486 and leave floating (a weak internal pull-up is provided) to indicate a 386.
HADS#	I	43	***Host Address Status.*** Connected to Host CPU ADS#. This is sampled at the rising edge of CLK, and when active, indicates valid address/status on the host address bus.
BLAST#/ EBCRDY#	I	77	***Burst Last or EBC 386Ready.*** The function of this pin is determined by the processor type. For 486 systems, this is the BLAST# signal from the CPU and is sampled on the rising edge of CLK except in T1 and the first T2. In 386 systems, this is connected to the HRDY0# signal from the EBC. The MCC internally OR's this signal along with any coprocessor ready signal to produce the BRDY# output, which is fed to the 386 CPU.
RDYI#/ 387RDY1#	I	7	***486 Ready In or 387 Ready1.*** The function of this pin is determined by the processor type. It is directly connected to the RDY# pin of the CPU for 486 systems and is used by other devices to indicate the end of the current cycle. In most 386 systems, RDYO# from the 387/3167 must be cascaded through the MCC. In this case, 387RDY1# is connected to READYO# from the numeric coprocessor. In all other 386 systems, this pin is left floating (a weak internal pull-up is provided).
387RDY2#	B	33	***387 Ready2.*** This pin is unused and should be tied high in 486 systems. In most 386 systems, RDYO# from the 387/3167 is cascaded through the MCC via 387RDY1#. In this case, 387RDY2# should be pulled high. In the special case where the 387/3167 READYO# is OR'D externally with the MCC's BRDY#, the READYO# from the coprocessor should be connected to 387RDY2# and 387RDY1# should be left unconnected. This second case is not recommended above 25MHz.
BRDY#	B	78	***Burst Ready.*** This signal is connected to the BRDY input of the 486 or to the READY# input of the 386. The MCC drives this line active (low) to indicate the end of a host CPU to local memory cycle. After being active, it is driven high (inactive) for one clock and then tristated. In 386 systems, it is also driven low for a CLK after EBCRDY# or 387RDY# is sampled active.

2.2.4 Arbiter

Pin Name	Type	Pin No.	Description
HHLDA	I	18	***Host Hold Acknowledge.*** Connected to HHLDA from the host CPU. This indicates an EISA/ISA/DMA/Refresh access.
EMSTR16#	I	19	***ISA Master.*** This input, from the ISP, indicates that an ISA master is in control of the Host/EISA bus.
MCCRDY	O	5	***MCC Ready.*** This normally active (high) signal goes inactive (low) when a hidden refresh cycle is pending and returns active when the refresh cycle is over. It is connected to the EBC MCCRDY input.

2.2.5 Bus Interface

Pin Name	Type	Pin No.	Description
BCLK	I	2	***EISA BCLK.*** EISA system clock. Connected from BCLK of the EISA connectors.
START#	I	13	***Start.*** This input indicates the beginning of an EISA/DMA/Refresh access and is connected to START# of the EISA connectors.
CMD#	I	14	***Command.*** Provides timing control within an EISA cycle. Connected to CMD# of the EISA connectors.
MSBURST#	I	15	***Master Burst.*** This input is sampled at the rising edge of BCLK and indicates that an EISA burst mode transfer should be carried out. It is connected to MSBURST# of the EISA connectors.
REFRESH#	I	8	***Refresh.*** Connected to REFRESH# of the EISA connectors. The leading edge of MRDC# is interpreted as a request to perform hidden refresh when this signal is active.
MRDC#	I	16	***Memory Read Command.*** The MCC uses this input to indicate a DRAM/Cache read from a master device (EMSTR16# active). Also, when REFRESH# is active, the leading edge of MRDC# is interpreted as a request to perform hidden refresh. Connected to MRDC# of the EISA connectors
MWTC#	I	17	***Memory Write Command.*** When EMSTR16# is active, the leading edge of MWTC# is used to start a DRAM/cache write. Connected to MWTC# of the EISA connectors.

2.2.6 Decode

Pin Name	Type	Pin No.	Description
HKEN#	O	79	***Host cache enable.*** Connected to the KEN# of the 486. It is based on a decode of HA[31:17] and will be active for cacheable regions of memory. This signal is forced active from the end of a CPU cycle to the end of the first T1.
HLOCM#	O	4	***Host Local Memory.*** Inhibits EISA/ISA cycle if active during a local Host master cycle. Connected to HLOCM# of the EBC.
GT1M#/ TMOD#	B	3	***Greater than 1MB or Test Mode.*** This pin serves two functions. This signal uses HA[31:20] and A20M# to decode memory accesses above 1MB (inactive for accesses in the 000XXXXXh range). It is connected to GT1M# of the EBC. The second function of this pin is to force the MCC into test mode. The MCC will enter its test mode when this pin is sampled low on the trailing edge of RST#. GATEA20/TSEL must be high at this sample point for the Tristate test mode to be entered.. A weak internal pull-up keeps GT1M#/TMOD high during RST# if no outside source/tester is driving it.
ROMCS0#	O	31	***ROM Chip Select 0.*** During normal operation, it goes active when FFFFXXXXh or FXXXXh is decoded from HA[31:16]. It is connected to CS# of the BIOS ROM.
ROMCS1#	O	32	***ROM Chip Select 1.*** ROMCS1# decodes a 16K/32K/64K block in the range C0000h thru EFFFFh based on the value programmed into the MCC's ROM/Shadow RAM index registers (C36h-C3Fh).

2.2.7 DRAM Interface

Pin Name	Type	Pin No.	Description
MA[11:0]	O	141-144 146-149 151-154	***Multiplexed DRAM addresses.*** This bus provides row and column address information to the DRAMs. External buffering is typically required (EBB or discrete). Note that for EISA master accesses, the HA bus should drive the MA through transparent latches (or use the EBB).
RAS#[3:0]	O	157-160	***Row Address Strobes.*** Each RAS output corresponds to one DRAM bank of four bytes.
CAS3#[3:0] CAS2#[3:0] CAS1#[3:0] CAS0#[3:0]	O	121,126, 131,136 122,127, 132,137 123,128, 133,138 124,129, 134,139	***Column Address Strobes.*** CAS0#_[3:0] connects to byte lanes 3 thru 0 of DRAM bank-0. Similarly, each set of four CAS lines corresponds to a particular 4-byte bank. To guarantee EISA memory access timing, these CAS signals should be connected directly (without external buffering) to the local memory DRAMs.
WE#	O	156	***Write Enable.*** This signal is externally buffered (EBB or discrete) to drive the WE# input of the DRAM's. WE# transitions with similar timing to RAS[3:0]#.

2.2.8 Cache Interface

Pin Name	Type	Pin No.	Description
TAG27/18 TAG26/17 TAG25/16 TAG[24:19]	B	103,104, 105, 96-99, 101,102	***Cache Tag Data Bus.*** Connected to the tag SRAM data bus. The tag number corresponds to the Host address line that it will be compared against. The tag bus is always 9 bits wide. For CPU accesses, the tag bits are sampled at the falling edge of CLK in the first T2. For EISA/DMA, they are sampled at the rising edge of BCLK30. For ISA masters, they are sampled at the leading edge of MRDC# or MWTC#.
TAGWE#	O	95	***Tag Write Enable.*** Connected to tag SRAM WE#. This signal is active during CPU read-miss cycles when the cache gets updated.
DIRTY	B	87	***Dirty bit.*** The dirty bit indicates whether the data in the cache has been modified. It is sampled on the rising edge of CLK on the first T2 of a CPU read miss cycle. It is connected to the data pin of the dirty-bit SRAM.
DIRTYWE#	O	88	***Dirty bit Write Enable.*** This signal goes active when the host CPU writes into the cache. It is connected to the WE# pin of dirty-bit SRAM.
XCA30E#	O	82	***External Cache address 3 Output Enable.*** Allows the CPU address lines HA2 and HA3 to drive the cache SRAM. Connected to the OE# of the buffer between HA2, HA3 and CAA3[1:0], and CAA2.
CAA31	O	83	***Cache Altered Address 3 (odd).*** Connected to cache bank-1 A3 for the 486 and to A3 of the entire cache for the 386.
CAA30	O	84	***Cache Altered Address 3 (even).*** Connected to cache bank-0 A3 for 486 systems.
CAA2		89	***Cache Altered Address 2.*** Connected to the cache address line A2.

HACALE	O	80	***HA bus to CA bus Latch Enable.*** This output provides the proper control timing to the latches that create the cache address bus CA[18:4] from the HA bus. This normally active signal goes inactive at the end of a host write or EISA/DMA access to provide sufficient hold time on the CA bus.
CACS#[1:0]	O	85,86	***Cache Memory Chip Selects.*** Connected to cache-memory CS# for odd & even banks respectively. These outputs are dependent upon the DRAM size, shadow -control, and cache mode bits. When the cache is interleaved (486), these normally active signals go inactive when there is a cache write to the opposite bank of cache.
CAOE#	O	106	***Early Cache Output Enable.*** This signal functions as an output enable for the cache SRAMs with slightly earlier timing than CDOE# and with fewer decoding restrictions. It is typically unused.
CAWE[3:0]#	O	107-109,111	***Cache Write Enables.*** Connected to cache-memory WE# pins for byte lanes 3 thru 0. These signals are derived from CLK2 if the MCC's Early Write Enable feature is set (Reg C31<0> = 1).

2.2.9 Data/Parity

Pin Name	Type	Pin No.	Description
CDOE[1:0]#	O	91,92	***Cache Data Output Enable.*** Used to enable data from the cache SRAM onto the local HD bus. For 486 systems, CDOE0# is always controls the low cache data SRAM bank and CDOE1# is used for the upper bank only when cache interleaving is selected (64k/256k cache size). For 386 systems, either signal can be used. In both cases, CDOE# will go high when HA31 is high.
XD[3:0]	B	23-26	***X-Data Bus.*** The MCC uses the low order nibble of the XD bus to provide the programming data for its internal registers. The upper four bits are ignored during I/O programming cycles to the MCC.
MDHDOE#	O	118	***Memory to Host Data Output Enable.*** This control signal enables instructs the DBC to enable data from the MD onto the HD bus for CPU DRAM reads. It is connected to MDHDOE0# of the DBC
MDHDCLK	O	117	***MD/HD Clock.*** This normally high signal is the clock used by the DBC's internal master-slave flip-flop between MD and HD busses. It is similarly used to clock the MP bits for parity checking. This signal should be connected to MDHDCLK of the DBC
HDMDLE#	O	116	***HD/MD Latch Enable.*** This normally active signal goes inactive during cache write-back cycles for one CLK when CAS# goes active. It is connected to HDMDLE# of the DBC.
HDMDOE#	O	115	***HD/MD Output Enable.*** This signal enables the HD bus onto the MD bus and is active for all CPU memory writes except cache hit cycles. It is connected to HDMDOE# of the DBC
PAREN#	O	119	***Parity Enable.*** PAREN# provides a timing pulse to the DBC after valid DRAM data has been read into the DBC. This pulse is used as the timing strobe to check for parity errors. It is connected to PAREN# of the DBC.

2.2.10 EISA-Timing Signals

Pin Name	Type	Pin No.	Description
BCLK15	I	6	***BCLK-15.*** 15ns delayed version of BCLK from the external delay line.
BCLK30	I	9	***BCLK-30.*** 30ns delayed version of BCLK from the external delay line.

2.2.11 Ground and VCC

Pin Name	Type	Pin No.	Description
VDD	I	20,30,61,100,110,140	+5V
VSS	I	1,10,40,50,70,81,90,114,120,125, 130,135,145,150	VSS or Ground
NC	N/A	12,22,28,93,94,112,113	No Connect. Reserved.

2.3 MCC Register Description

Revision/Refresh/Status Register
Index:C30h

BIT	FUNCTION	DEFAULT
3-2	The MCC revision number (read only)	00
1	Hidden refresh 0 = Disable, 1 = Enable	0
0	Fast A20 mask. This bit is internally OR'd with the GATEA20 input to generate A20M#.	0

Cache Configuration Register 0
Index:C31h

BIT	FUNCTION	DEFAULT
3,2	Cache burst wait-state control: 00 = 3-1-1-1 cycles 01 = 2-1-1-1 cycles 10 = 3-2-2-2 cycles 11 = 2-2-2-2 cycles	00
1	0 wait-state cache write 0 = disable 1 = enable	0
0	Early cache write enable 0 = disable 1 = enable	0

Cache Configuration Register 1
Index: C32h

BIT	FUNCTION	DEFAULT
3-2	Cache Size and Max. cachable DRAM <u>3 2</u> <u>Cache Size</u> <u>Cachable DRAM</u> 0 0 64K 32M 0 1 128K 64M 1 0 256K 128M 1 1 512K 256M	00
1-0	Cache mode select: 00 Enable Enables normal cache operation. 01 Disable (Default) Disable cache. DRAM reads will invalidate the tag and clear the dirty bit. Flush by reading a block of memory equal to the cache size. 10 Test-1 All accesses go to DRAM. Upon a DRAM read, the tag and dirty-bit is written with the values defined in I/O registers C4Dh thru C4Fh. 11 Test-2 All accesses go to DRAM. Upon a read miss, the tag and dirty-bit is read into I/O registers C4Dh thru C4Fh	01

DRAM Configuration Register 0
Index: C33h

BIT	FUNCTION	DEFAULT
3	Control CAS# pulse width for ISA master 0 : 1 CPU clock 1 : 2 CPU clock	0
2-0	Bank[1:0] DRAM Configuration. 16M DRAM can't mix with 4M/1M memory 2 1 0 Bank0 Bank1 0 0 0 1M -- 0 0 1 1M 1M 0 1 0 1M 4M 0 1 1 -- -- 1 0 0 4M -- 1 0 1 4M 4M 1 1 0 16M -- 1 1 1 16M 16M	000

DRAM Configuration Register 1
Index:C34h

BIT	FUNCTION	DEFAULT
3	Unused	X
2-0	Bank[3:2] DRAM Configuration 2 1 0 Bank2 Bank3 0 0 0 1M -- 0 0 1 1M 1M 0 1 0 -- -- 0 1 1 4M 1M 1 0 0 4M -- 1 0 1 4M 4M 1 1 0 16M -- 1 1 1 16M 16M	000

DRAM Wait-State Control Register
Index:C35h

BIT	FUNCTION	DEFAULT
3-2	Wait states for CPU-DRAM read cycles 3 2 Wait State 0 0 0 wait state 0 1 1 wait state 1 0 2 wait states 1 1 3 wait states	11
1	Wait states for CPU-DRAM write cycles 0 - 0 wait state 1 - 1 wait state	1
0	Unused	X

Shadow RAM Control Registers
Index:C36h,C37h,C38h,C39h,C3Ah,C3Bh,C3Ch,C3Dh,C3Eh,C3Fh

Each 16K block between C0000h to DFFFFh can be individually shadowed. Each 16k block between C0000h to C7FFFh can also be made cachable for host CPU only. The MCC will not respond in this area for EISA/DMA/ISA accesses. Each 64K segment between E0000h to FFFFFh can also be controlled in the same fashion (E0000h-EFFFFh is shadowable and F0000h-FFFFFh is shadowable and cacheable)..

The general purpose ROMCS1# pin can be made active selectively for each of the 10 memory areas defined below by writing the appropriate value into bits [3:0] of the Shadow RAM Control Registers. The meaning of each bit is explained below:

Bit-0: RE: 1 enables CPU read from DRAM if bit 3 is 0
Bit-1: WE: 1 enables CPU write from DRAM
Bit-2: CE: 1 makes Cachable if DRAM selected
Bit-3: ROM: 1 enables decode of ROM chip select and inhibits DRAM read

INDEX	START ADDRESS	BLOCK SIZE	BIT 3 2 1 0	DEFAULT
C36h	C0000h	4000h	ROM CE WE RE	0000
C37h	C4000h	4000h	ROM CE WE RE	0000
C38h	C8000h	4000h	ROM WE RE	0X00
C39h	CC000h	4000h	ROM WE RE	0X00
C3Ah	D0000h	4000h	ROM WE RE	0X00
C3Bh	D4000h	4000h	ROM WE RE	0X00
C3Ch	D8000h	4000h	ROM WE RE	0X00
C3Dh	DC000h	4000h	ROM WE RE	0X00
C3Eh	E0000h	10000h	ROM WE RE	0X00
C3Fh	F0000h	10000h	ROM CE WE RE	1000

Upper-Bound-Cachable-Region Register
Index: C40h

BIT	FUNCTION	DEFAULT
3-0	Define the upper bound of cachable memory region <u>3210</u> <u>Upper Bound Cachable Region</u> 0000 64M 0001 4M 0010 8M 0011 12M 0100 16M 0101 20M 0110 24M 0111 28M 1000 32M 1001 36M 1010 40M 1011 44M 1100 48M 1101 52M 1110 128M 1111 256M	0000

NCA0-Block-Size Register
Index: C41h

BIT	FUNCTION	DEFAULT
3	Unused	X
2-0	Define the size of non-cachable block NCA0. <u>2 1 0</u> <u>Block size</u> 0 0 0 64K 0 0 1 128K 0 1 0 256K 0 1 1 512K 1 0 0 invalid 1 0 1 invalid 1 1 0 invalid 1 1 1 disable non-cachable block 0	000

NCA0-Start-Address Register 0
Index:C42h

BIT	FUNCTION	DEFAULT
3	Address bit 27 of NCA0	0
2	Address bit 26 of NCA0	0
1	Address bit 25 of NCA0	0
0	Address bit 24 of NCA0	0

NCA0-Start-Address Register 1
Index:C43

BIT	FUNCTION	DEFAULT
3	Address bit 23 of NCA0	0
2	Address bit 22 of NCA0	0
1	Address bit 21 of NCA0	0
0	Address bit 20 of NCA0	0

NCA0-Start-Address Register 2
Index:C44h

BIT	FUNCTION	DEFAULT
3	Address bit 19 of NCA0	0
2	Address bit 18 of NCA0	0
1	Address bit 17 of NCA0	0
0	Address bit 16 of NCA0	0

NCA1-Block-Size Register
Index: C45h

BIT	FUNCTION	DEFAULT
3	Unused	0
2-0	Define the size of non-cachable block NCA1. 2 1 0 Block size 0 0 0 64K 0 0 1 128K 0 1 0 256K 0 1 1 512K 1 0 0 invalid 1 0 1 invalid 1 1 0 invalid 1 1 1 disable non-cachable block 1	000

NCA1-Start-Address Register 0
Index:C46h

BIT	FUNCTION	DEFAULT
3	Address bit 27 of NCA1	0
2	Address bit 26 of NCA1	0
1	Address bit 25 of NCA1	0
0	Address bit 24 of NCA1	0

NCA1-Start-Address Register 1
Index:C47h

BIT	FUNCTION	DEFAULT
3	Address bit 23 of NCA1	0
2	Address bit 22 of NCA1	0
1	Address bit 21 of NCA1	0
0	Address bit 20 of NCA1	0

NCA1-Start-Address Register 2
Index:C48h

BIT	FUNCTION	DEFAULT
3	Address bit 19 of NCA1	0
2	Address bit 18 of NCA1	0
1	Address bit 17 of NCA1	0
0	Address bit 16 of NCA1	0

NCA2-Block-Size Register
Index: C49h

BIT	FUNCTION	DEFAULT
3	Unused	0
2-0	Define the size of non-cachable block NCA2. 2 1 0 Block size 0 0 0 64K 0 0 1 128K 0 1 0 256K 0 1 1 512K 1 0 0 invalid 1 0 1 invalid 1 1 0 invalid 1 1 1 disable non-cachable block 2	000

NCA2-Start-Address Register 0
Index:C4Ah

BIT	FUNCTION	DEFAULT
3	Address bit 27 of NCA2	0
2	Address bit 26 of NCA2	0
1	Address bit 25 of NCA2	0
0	Address bit 24 of NCA2	0

NCA2-Start-Address Register 1
Index : C4Bh

BIT	FUNCTION	DEFAULT
3	Address bit 23 of NCA2	0
2	Address bit 22 of NCA2	0
1	Address bit 21 of NCA2	0
0	Address bit 20 of NCA2	0

NCA2-Start-Address Register 2
Index : C4Ch

BIT	FUNCTION	DEFAULT
3	Address bit 19 of NCA2	0
2	Address bit 18 of NCA2	0
1	Address bit 17 of NCA2	0
0	Address bit 16 of NCA2	0

Tag-Bit-Test-Mode-Register 0
Index : C4Dh

BIT	FUNCTION	DEFAULT
3	TAG19	0
2	TAG18	0
1	TAG26/17	0
0	TAG25/16	0

Tag-Bit-Test-Mode-Register 0
Index : C4Eh

BIT	FUNCTION	DEFAULT
3	TAG23	0
2	TAG22	0
1	TAG21	0
0	TAG20	0

Tag-Bit-Test-Mode-Register 0
Index : C4Fh

BIT	FUNCTION	DEFAULT
3	TAG24	0
2	Unused	
1	Unused	
0	Dirty bit	0

2.4 AC/DC SPECIFICATIONS

2.4.1 82C682 (MCC) Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	70	C
Tstg	Storage Temperature	-40	125	C

Note: Permanent device damage may occur if Absolute maximum Ratings are exceeded.

2.4.2 82C682 (MCC) DC Characteristics

Temperature: 0C to 70C, Vcc: 5V +/- 5%

Sym	Description	Min	Max	Units
VIL	Input Low Voltage		0.8	V
VIH	Input High Voltage		2.0	V
VOL	Output Low Voltage (IOL = 4.0 mA)		0.4	V
VOH	Output High Voltage (IOH = -1.6mA)	2.4		V
IIL	Input Leakage Current, VIN = Vcc		10	uA
IOZ	Tristate Leakage Current		10	uA
CIN	Input Capacitance		20	pF
COUT	Output Capacitance		20	pF
ICC	Power Supply Current			mA

2.4.3 82C682(MCC) A.C. Specification Tables

Sym	Description	Min	Typ	Max
t101	CLK period	30		
t102	CLK high time	13		17
t103	CLK low time	13		17
t104	CLK fall time			2
t105	CLK rise time			2
t106	CLK2 period	15		
t107	CLK2 high time	6		8
t108	CLK2 low time	6		8
t109	CLK2 fall time			2
t110	CLK2 rise time			2
t111	CLK2 to CLK delay	0		8
t201	RESET setup to CLK^	5		
t202	RESET hold from CLK^	5		
t203	RESET pulse width in CLKs	16		
t301	TAG assert delay from CLK^			
t302	TAG negate delay from CLK^			
t303	TAG setup from CLK^			
t304	TAG hold from CLK^			
t305	TAGWE# assert delay from CLK^			18
t306	TAGWE# negate delay from CLK^			18
t307	DIRTY assert delay from CLK^			
t308	DIRTY assert delay from CLK^			
t309	DIRTY setup from CLK^			
t310	DIRTY hold from CLK^			
t311	DIRTYWE# assert delay from CLK^			17
t312	DIRTYWE# negate delay from CLK^			17
t313	XCA30E# assert delay from CLK^			
t314	XCA30E# negate delay from CLK^			
t315	CAA31 valid from HADDRESS valid			19
t316	CAA31 negate from CLK^			19
t317	CAA30 valid from HADDRESS valid			19
t318	CAA30 negate from CLK^			19
t319	CAA2 assert delay from CLK^			
t320	CAA2 negate delay from CLK^			
t321	HACALE assert from HADS# assert			12
t322	HACALE negate from HADS# negate			20
t323	CACS[1:0] assert delay from address valid			18
t324	CACS[1:0] negate delay from address valid			18
t325	CAOE# assert delay from address valid			18
t326	CAOE# negate delay from address invalid			18
t327	CAWE# assert delay from CLK^			18
t328	CAWE# negate delay fro CLK^			18
t329	CDOE0# assert delay from address valid			19
t330	CDOE0# negate delay from CLK^			18
t331	CDOE1# assert delay from CLK^			18

2.4.3 82C682(MCC) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t332	CDOE1# negate delay from CLK^			18
t333	CAWE# assert from CLK2^			18
t334	CAWE# negate from CLK2^			17
t335	DRTYWE# assert from CLK2^			18
t336	DRTYWE# negate from CLK2^			17
t501	MA[10:0] assert delay from CLK^	8		16
t502	MA[10:0] negate delay from CLK^	8		16
t503	RAS# assert delay from CLK^			20
t504	RAS# negate delay from CLK^			16
t505	CAS# assert delay from CLK^			16
t506	CAS# negate delay from CLK^			18
t507	WE# assert delay from CLK^	11		18
t508	WE# negate delay from CLK^	8		16
t509	MDHDOE# assert delay from CLK^			24
t510	MDHDOE# negate delay from CLK^			13
t511	MDHDCLK assert delay from CLK^			25
t512	MDHDCLK negate delay from CLK^			25
t513	HDMDLE# assert delay from CLK^			15
t514	HDMDLE# negate delay from CLK^			20
t515	HDMDOE# assert delay from CLK^			21
t516	HDMDOE# negate delay from CLK^			15
t517	PAREN# assert delay from CLK^			21
t518	PAREN# negate delay from CLK^			18
t701	ROMCS# assert delay from CLK^			23
t702	ROMCS# negate delay from CLK^			
t801	BCLK period	120		250
t802	BCLK high time	55		
t803	BCLK low time	55		
t804	BCLK rise time			
t805	BCLK fall time			
t806	START setup from BCLK	25		
t807	START hold from BCLK	45		
t808	CMD# active to read data valid			
t809	CMD# setup from BCLK	20		
t810	CMD# hold from BCLK			
t811	MSBURST# setup to BLCK	20		
t812	MSBURST# hold from BCLK			
t813	REFRESH setup to BCLK	20		
t814	REFRESH hold from BCLK			
t815	MRDC# setup to BCLK			
t816	MRDC# hold from BCLK			
t817	MWTC# setup to BCLK			
t818	MWTC# hold from BCLK			
t819	HLOCM# assert delay from CLK^			
t820	HLOCM# negate delay from CLK^			
t821	RAS# active from HLOCM# active			

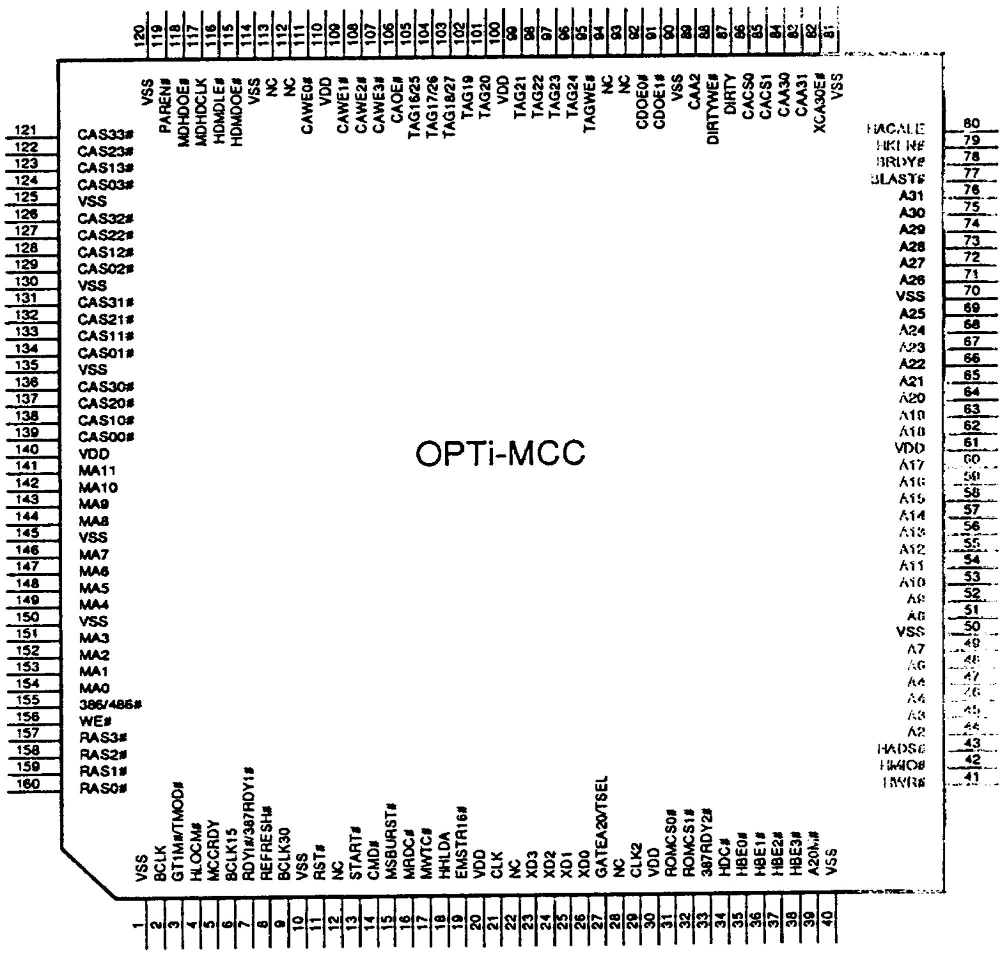
2.4.3 82C682(MCC) A.C. Specification Tables (Continued)

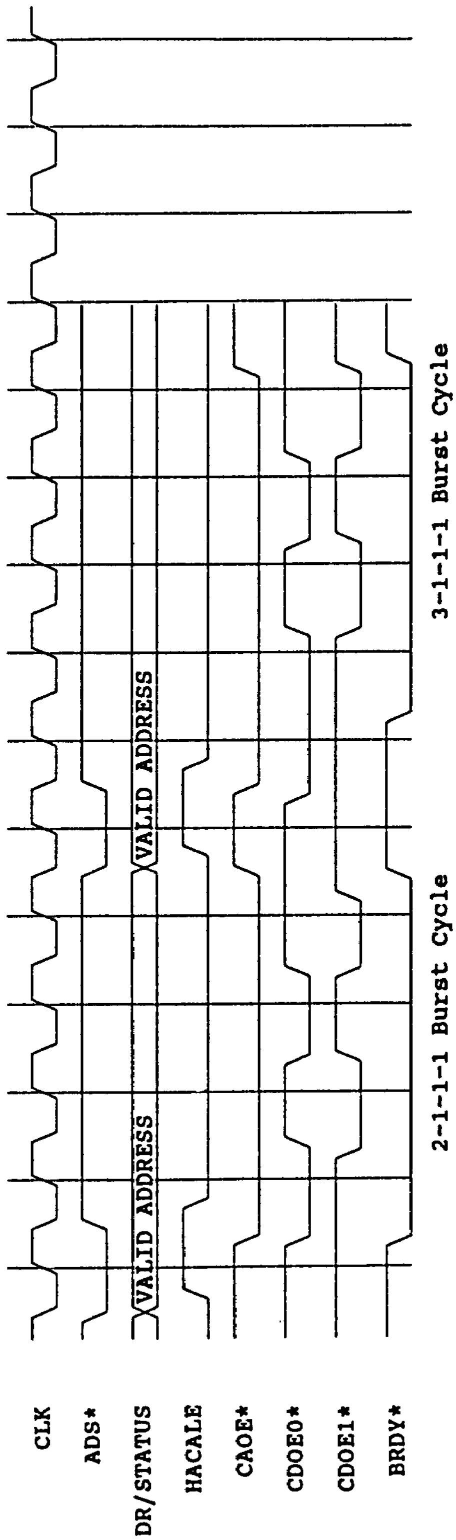
Sym	Description	Min	Typ	Max
t901	MCCRDY# assert delay from CLK^			
t902	MCCRDY# negate delay from CLK^			
t903	BRDY# assert delay from CLK^			17
t904	BRDY# negate delay from CLK^			17
t905	HKEN# assert delay from CLK^			25
t906	HKEN# negate delay from CLK^			20
t907	READY# assert delay from CLK^			17
t908	READY# negate delay from CLK^			18
t909	GT1M#/TMOD# assert delay from CLK^			
t910	GT1M#/TMOD# negate delay from CLK^			
t911	RDY#/387RDY1# setup to CLK^			
t912	RDY#/387RDY1# hold from CLK^			

Note:

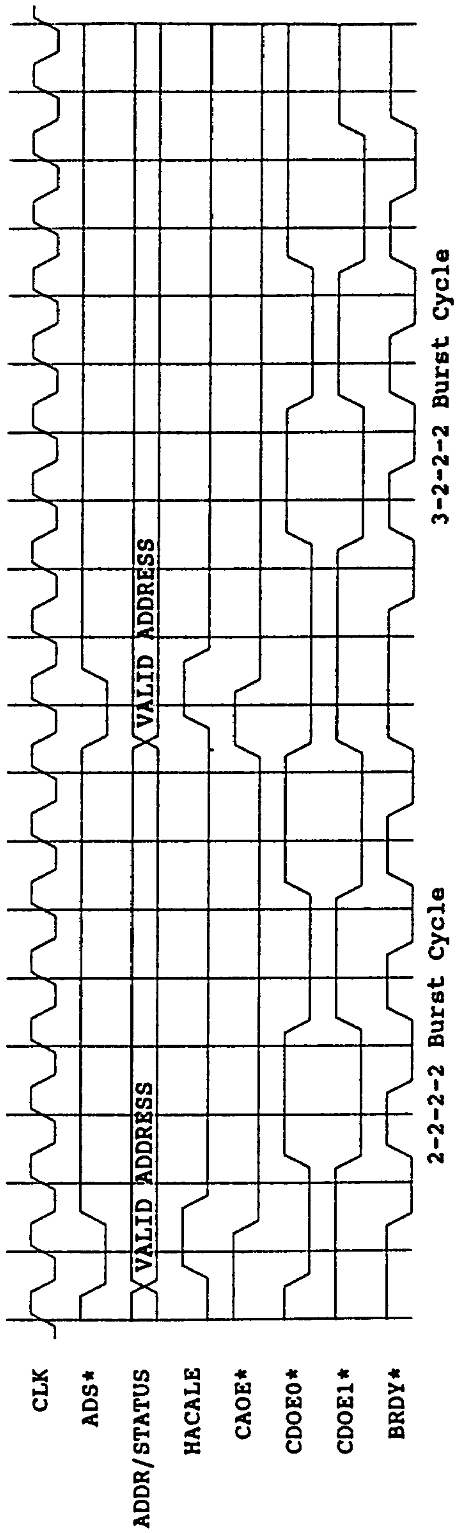
T1^	Rising edge of T1
T1	Falling edge of T1
T2^	Rising edge of T2
T2	Falling edge of T2
BCLK^	Rising edge of BCLK
BCLK	Falling edge of BCLK
CLK^	Rising edge of CLK
CLK	Falling edge of CLK
CLK2^	Rising edge of CLK2
CLK2	Falling edge of CLK2

2.5 82C682 (MCC) PIN-OUT

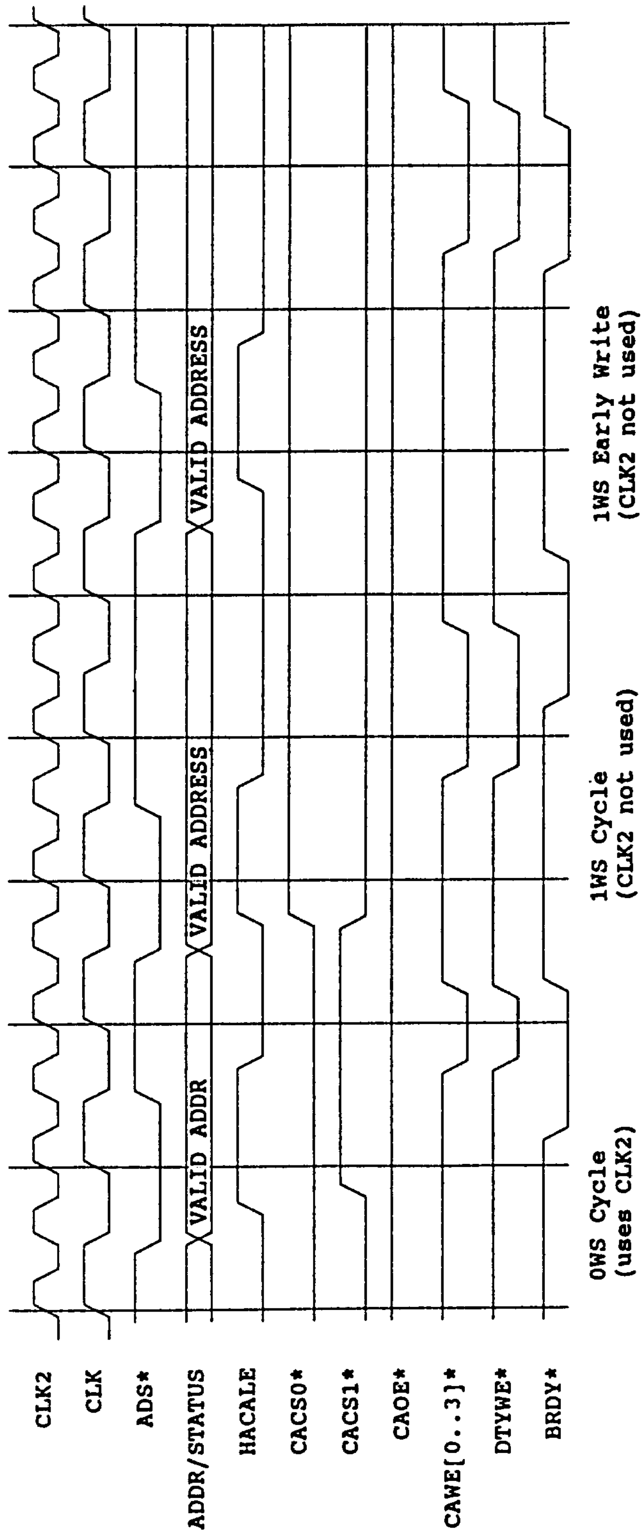




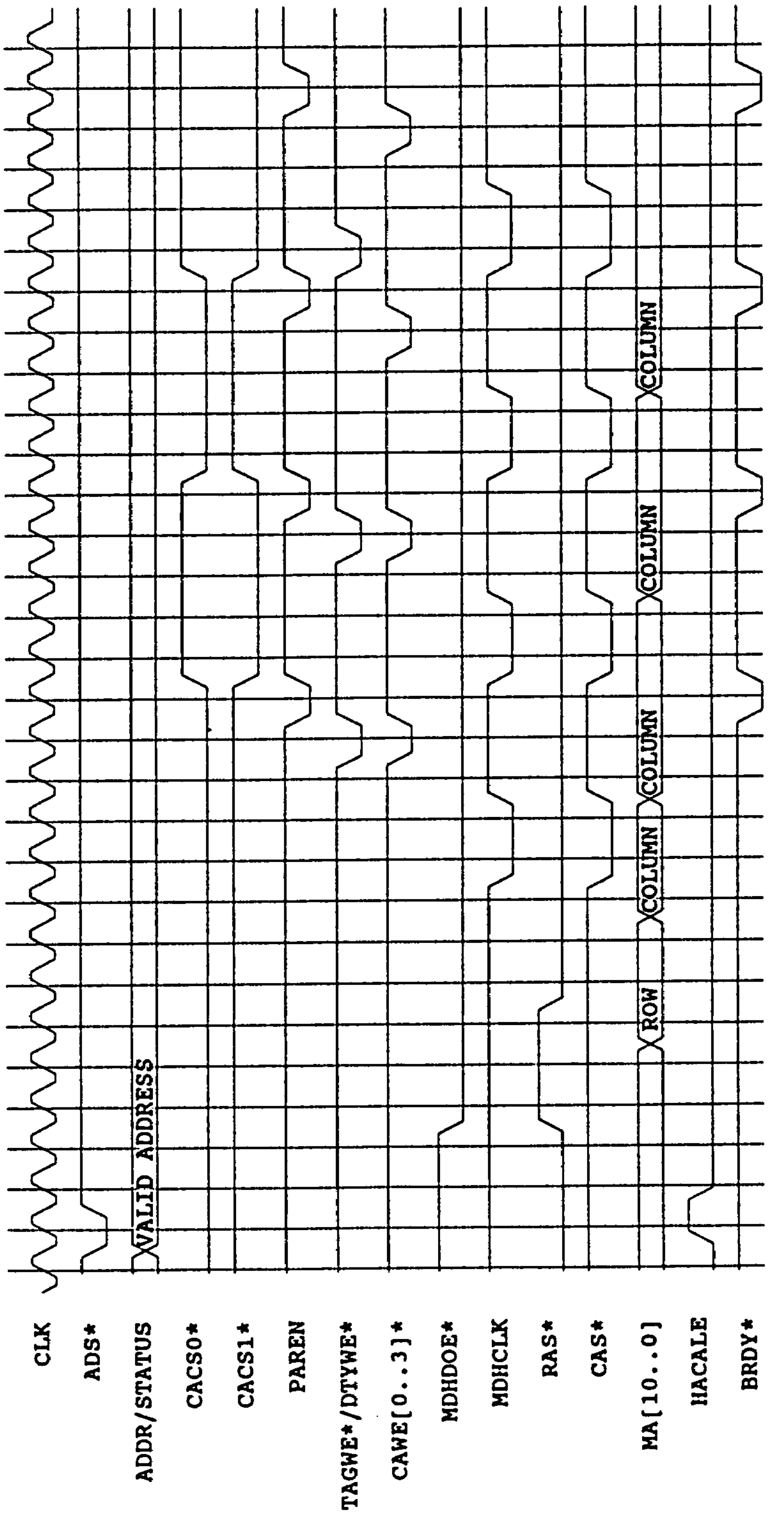
486 SECONDARY CACHE READ HIT



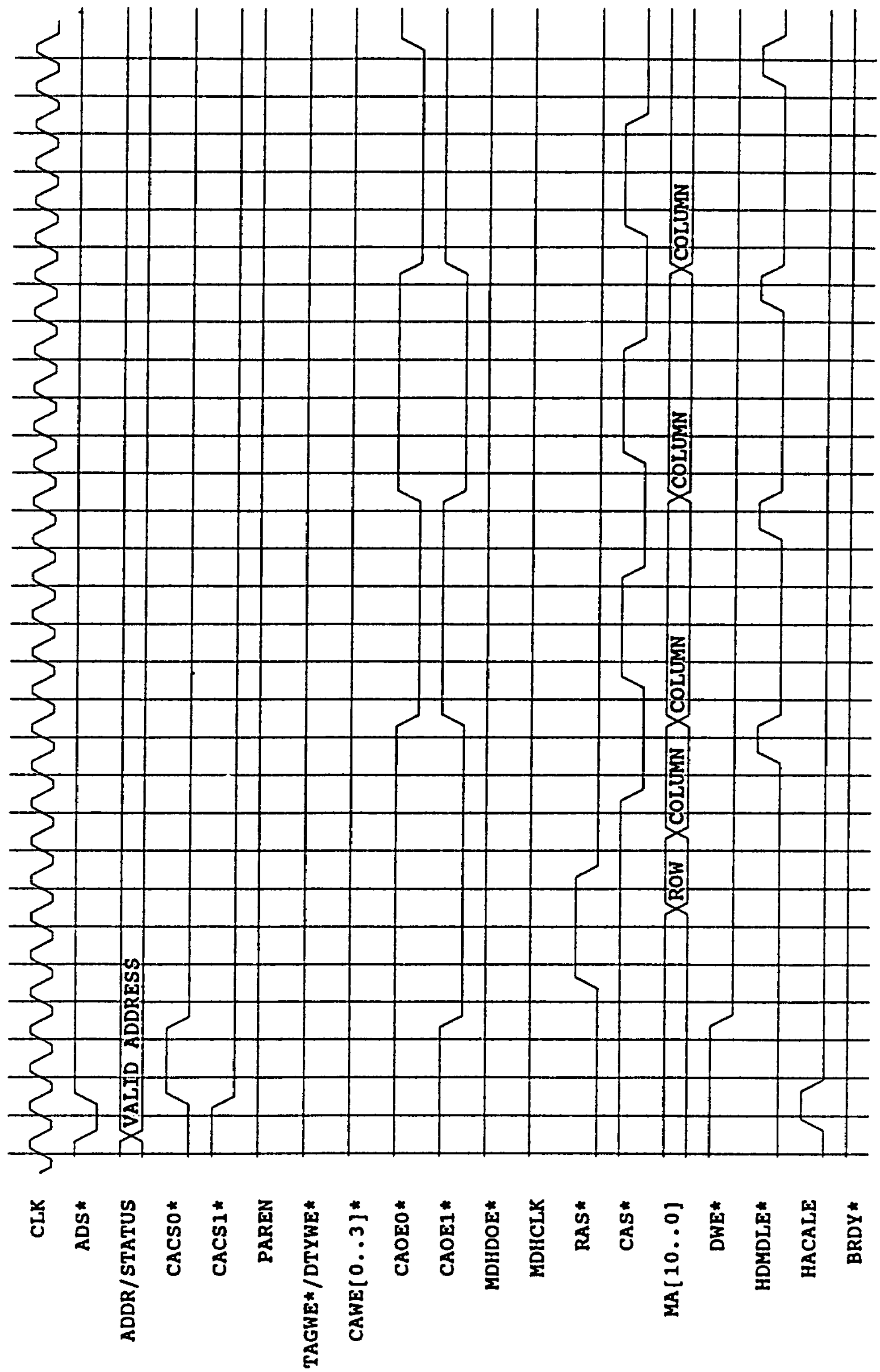
486 SECONDARY CACHE READ HIT



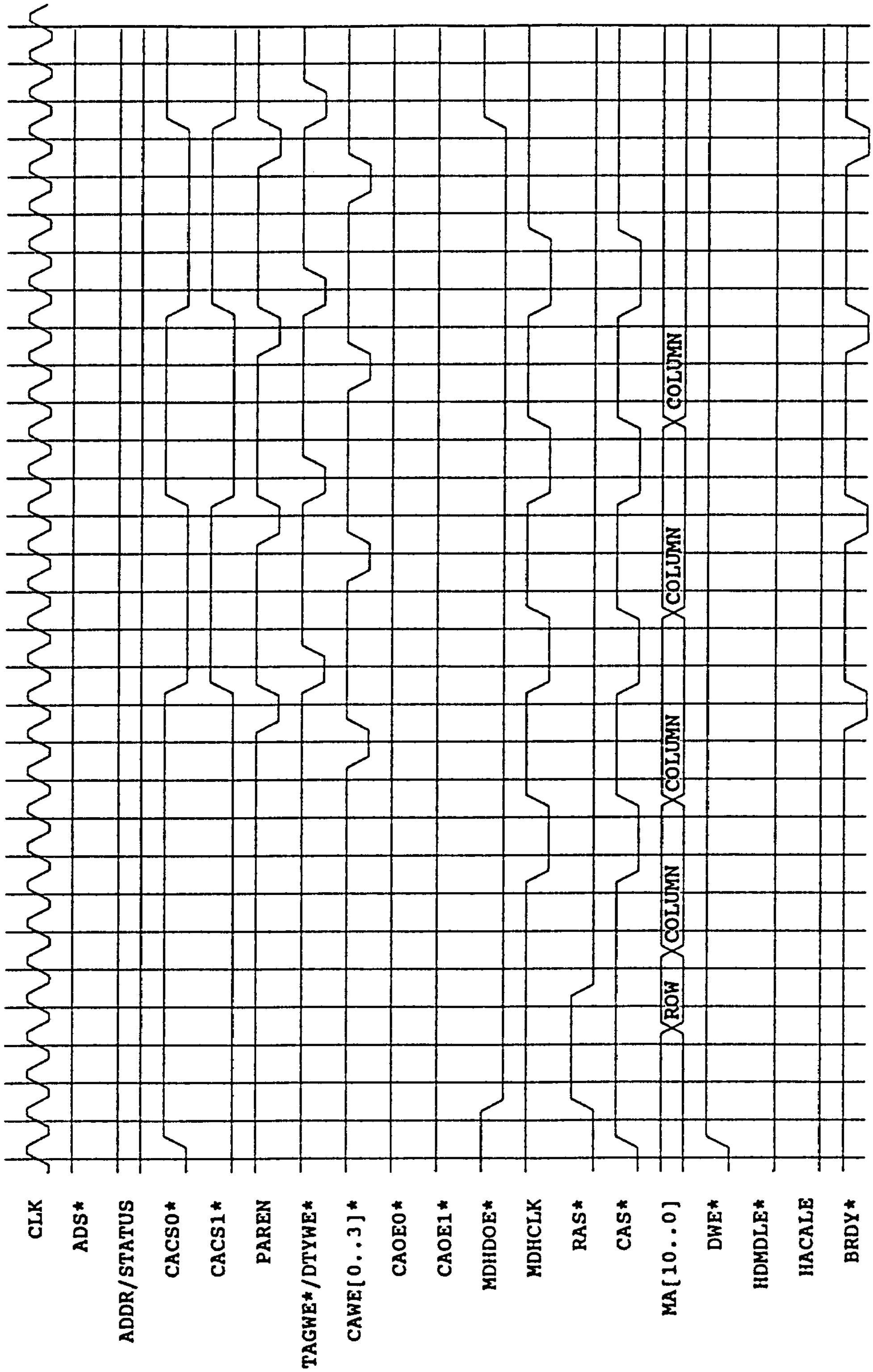
496 Secondary Cache Write Hit Cycle



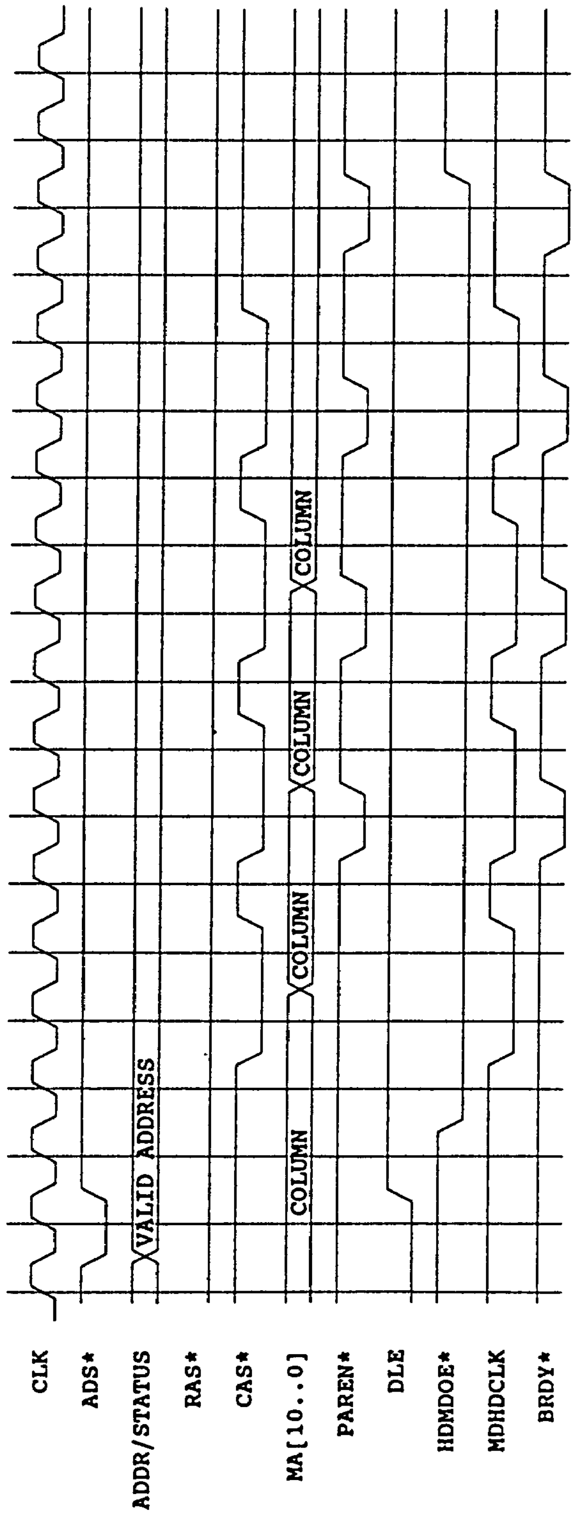
DRAM READ MISS CYCLE NOT DIRTY 1WS



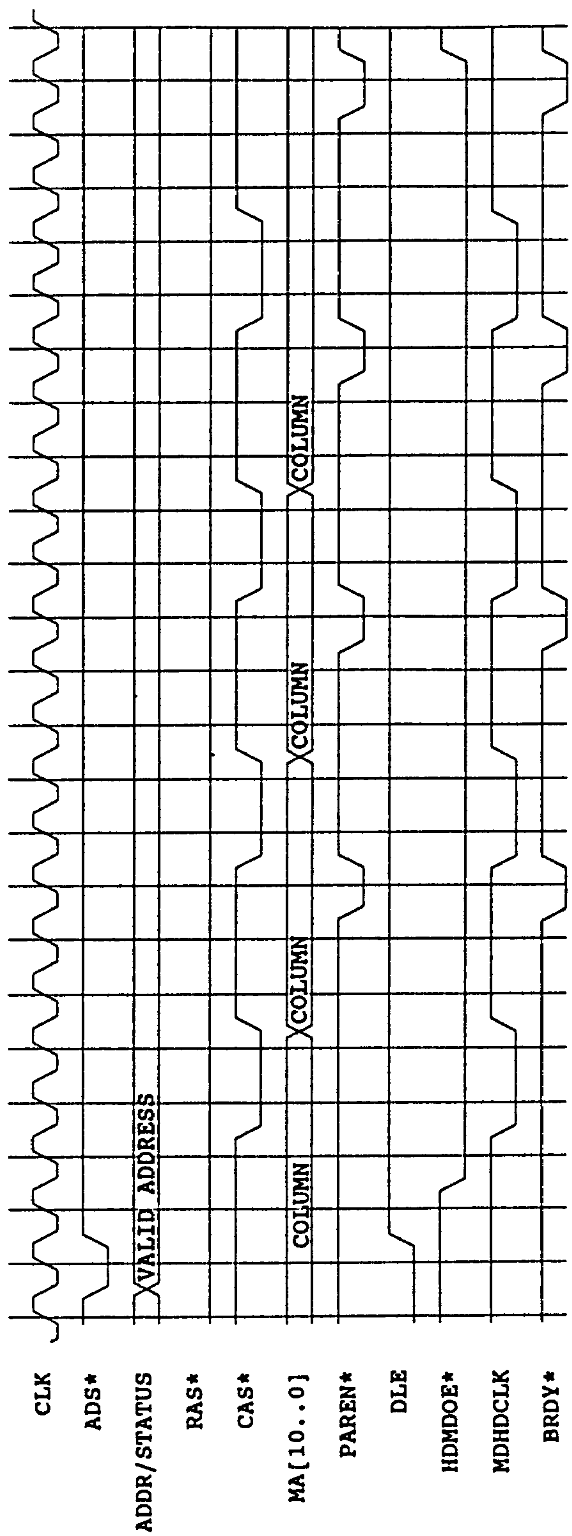
READ MISS DIRTY CYCLE 1WS



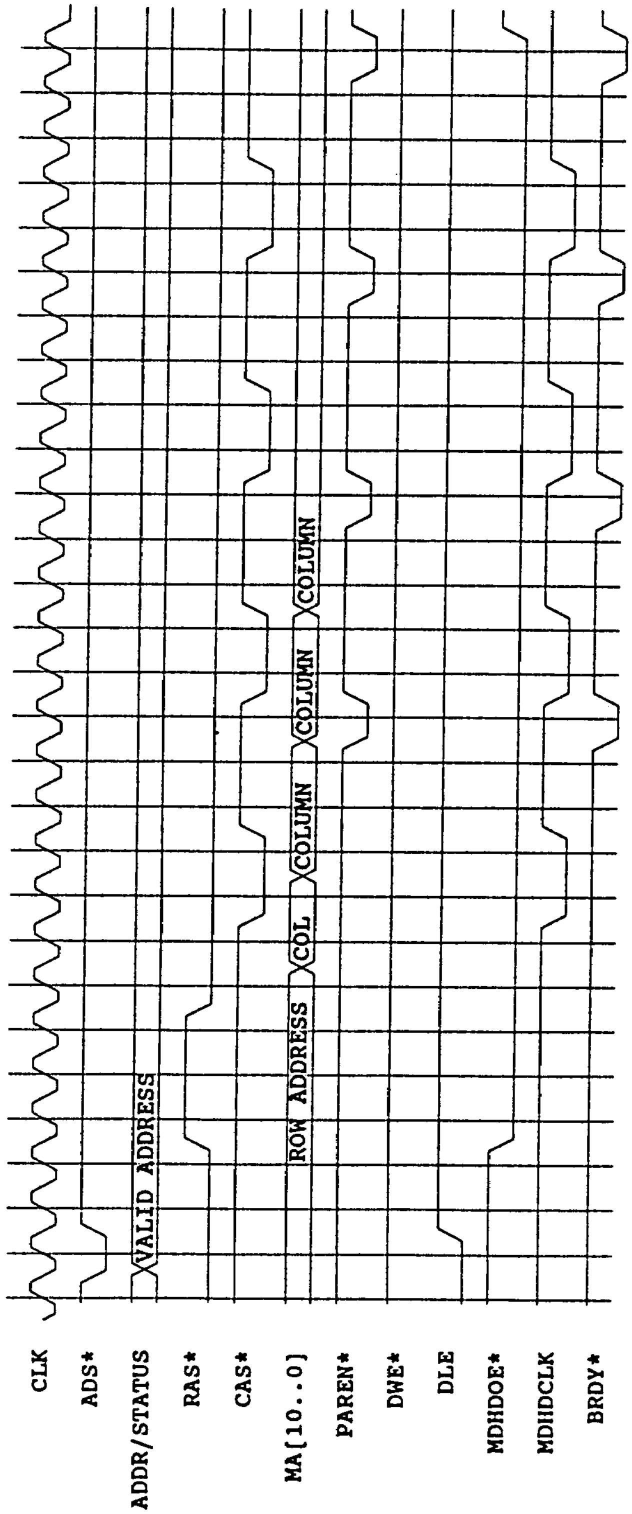
READ MISS DIRTY CYCLE 1WS



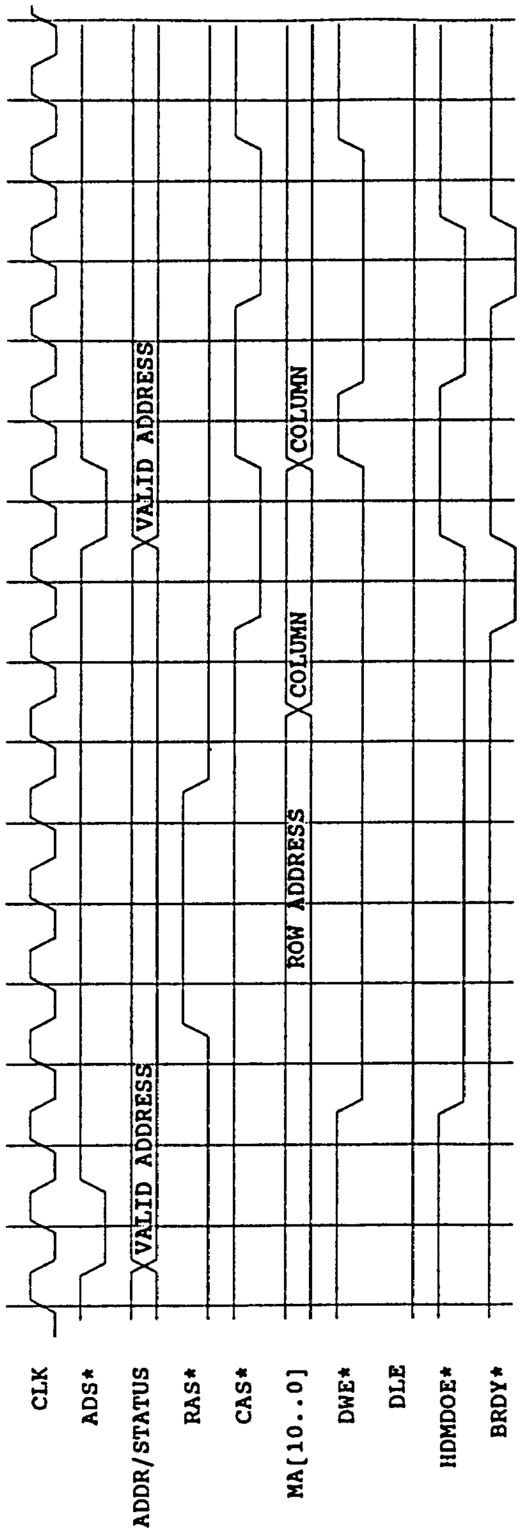
DRAM READ PAGE HIT 0WS



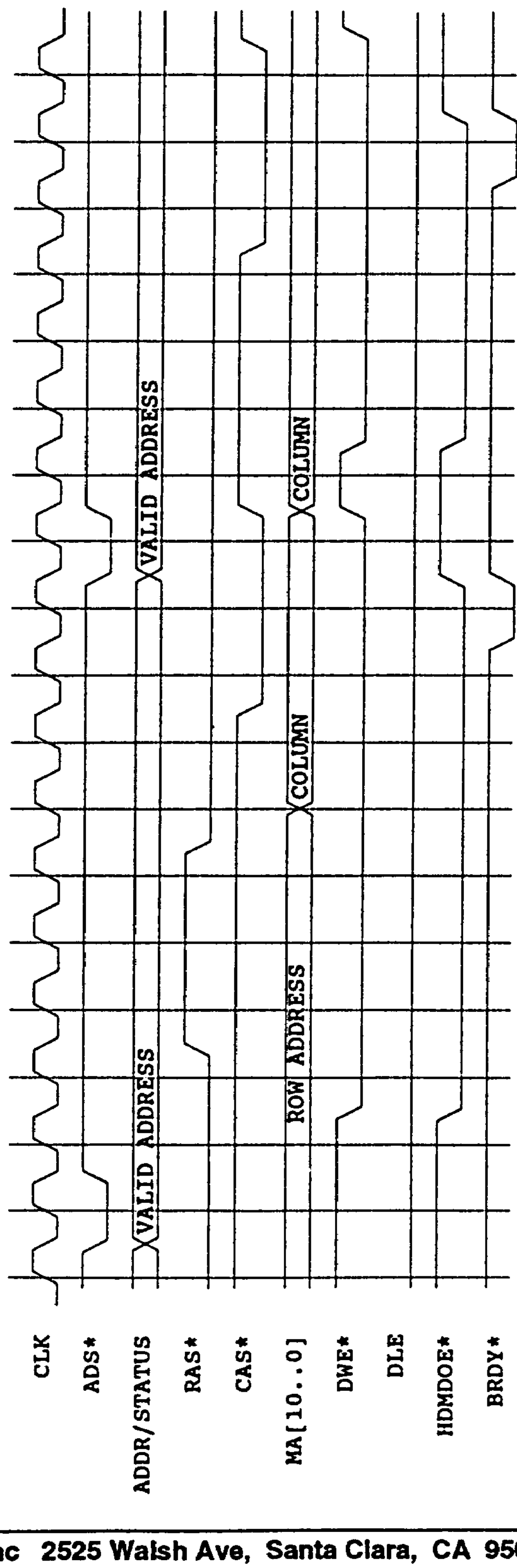
DRAM READ PAGE HIT 1WS



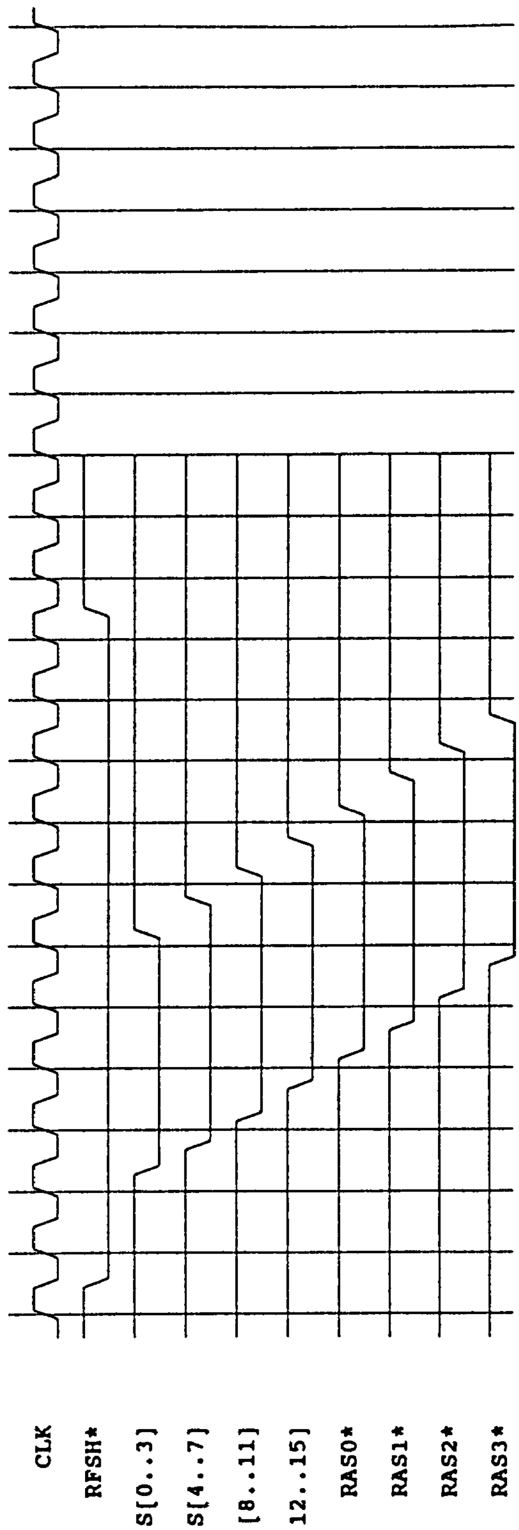
DRAM READ PAGE MISS 1WS



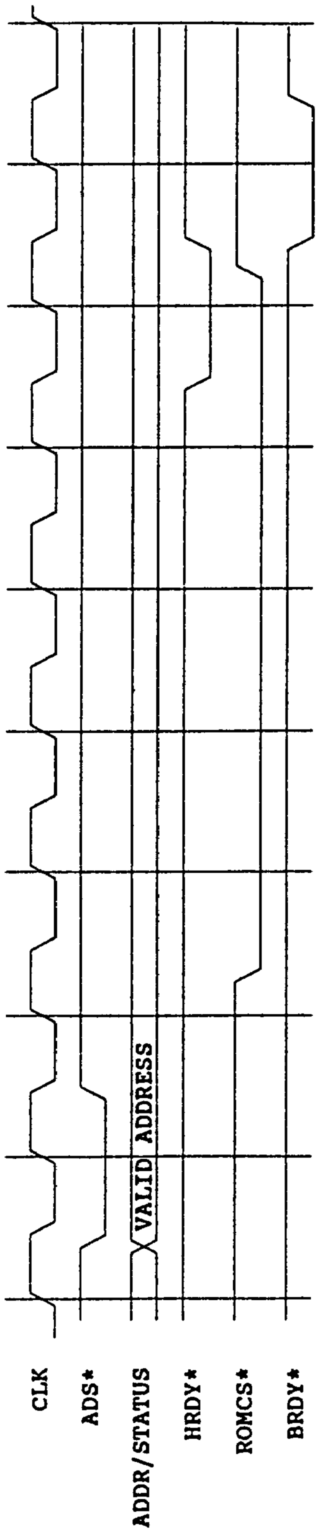
DRAM WRITE PAGE MISS 0WS PAGE HIT 0WS



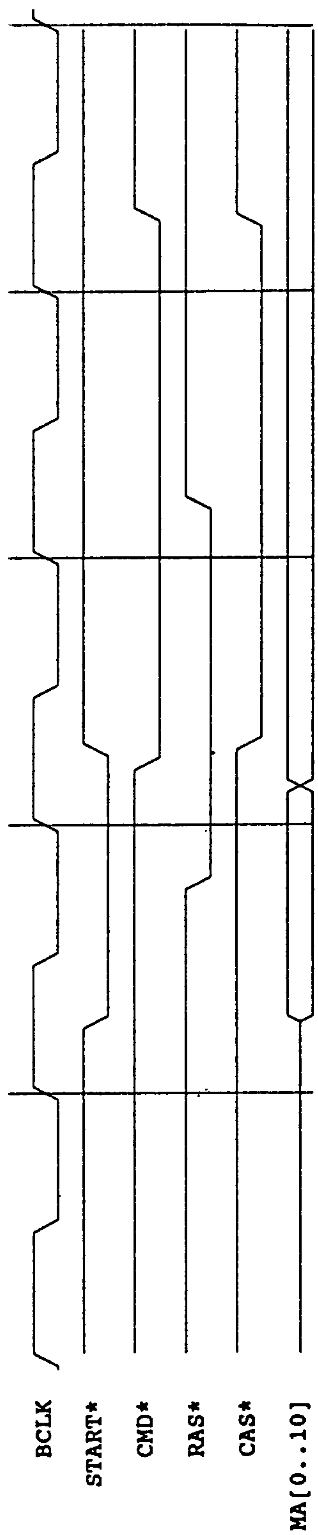
DRAM WRITE PAGE MISS 1WS PAGE HIT 1WS



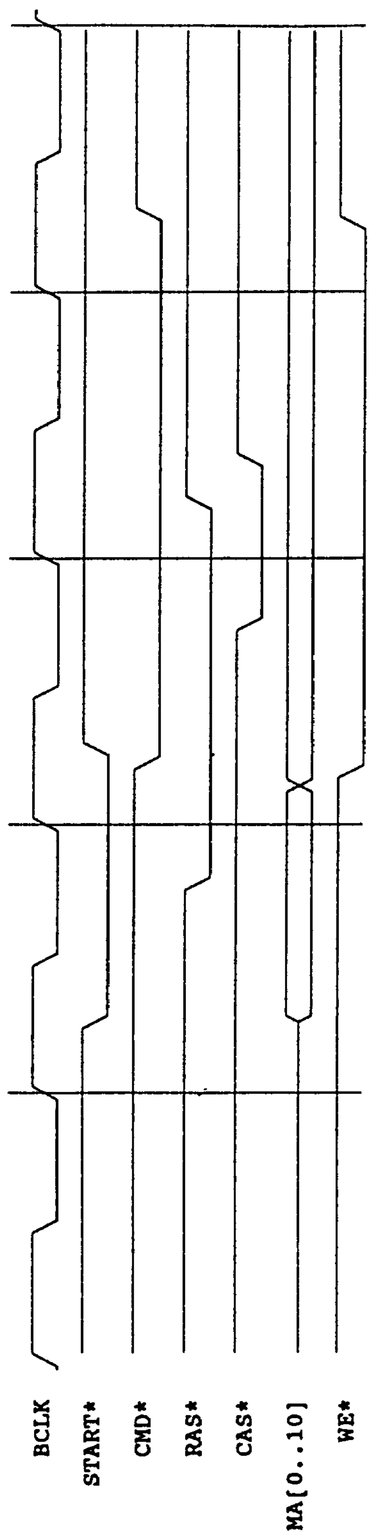
NORMAL REFRESH, NORMAL SPEED



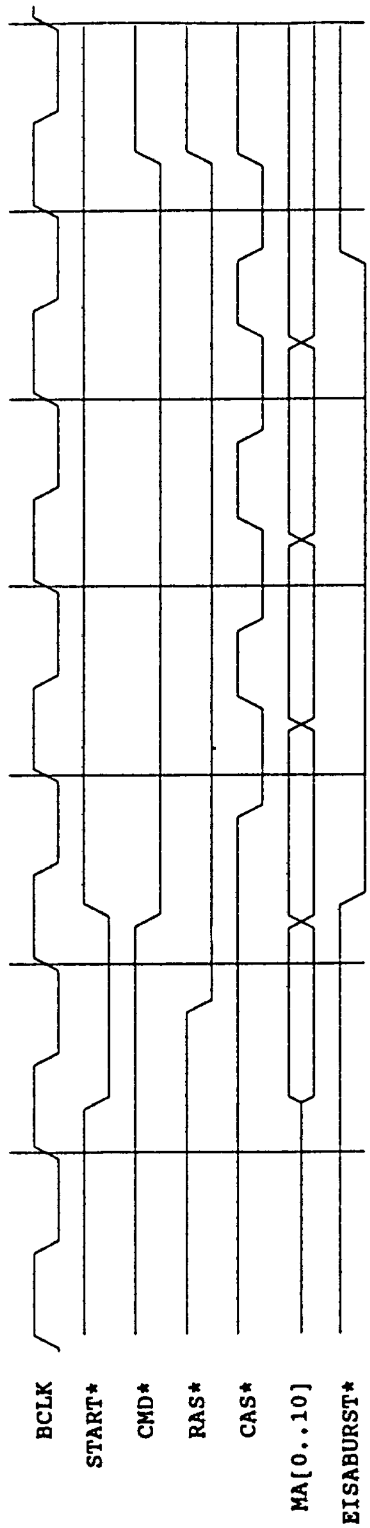
ROM CYCLE



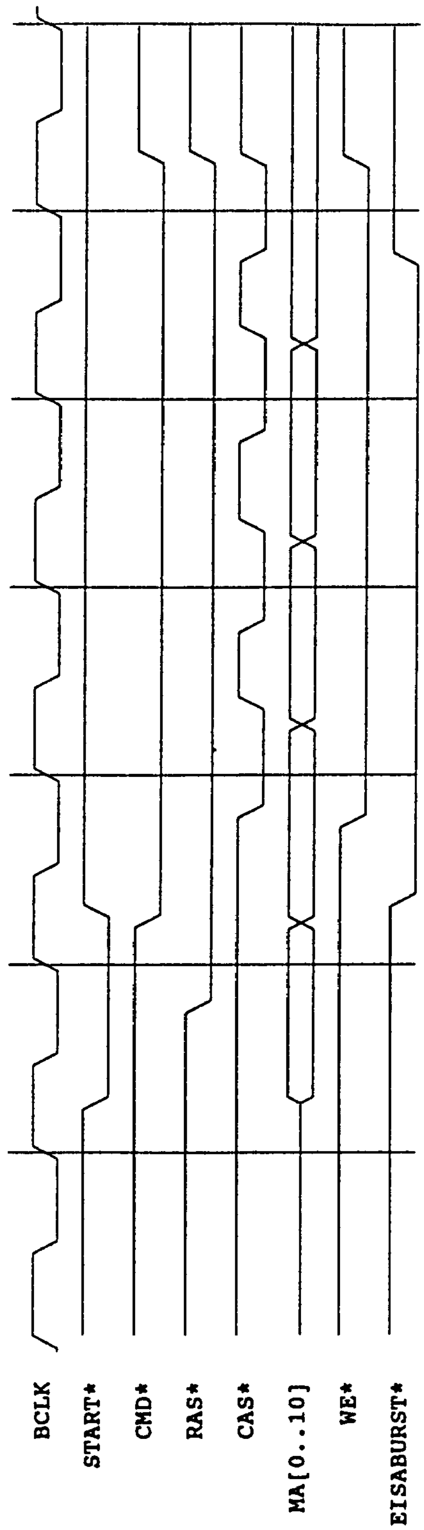
EISA READ



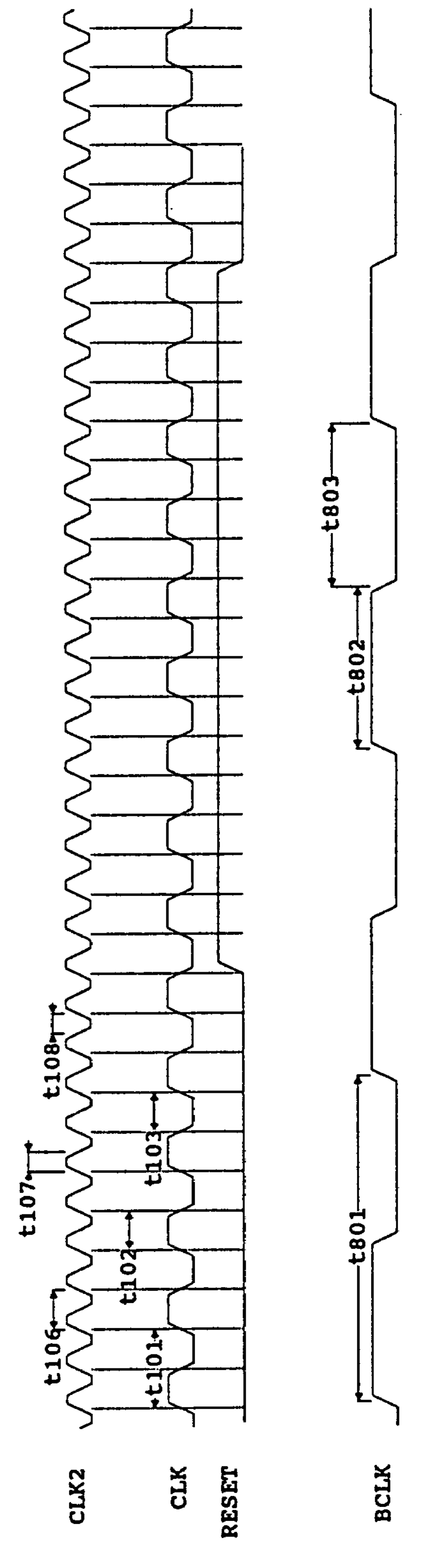
EISA WRITE



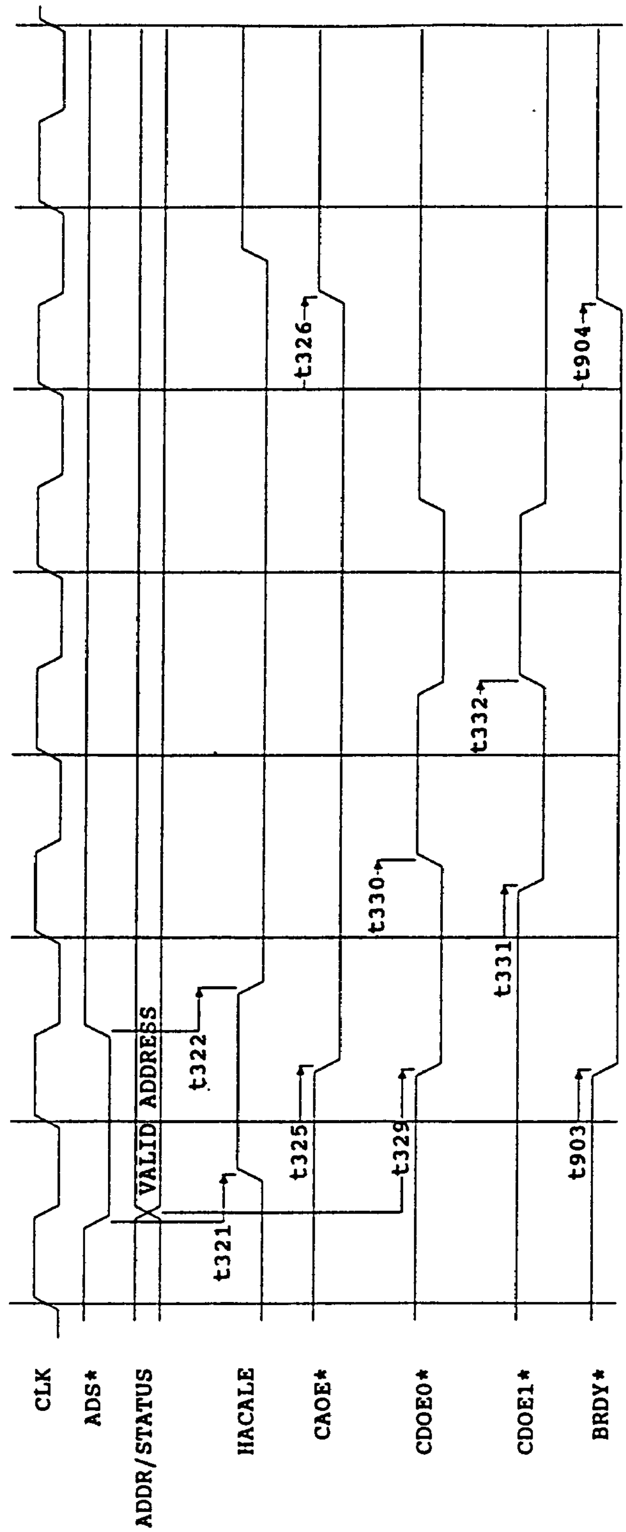
EISA BURST READ



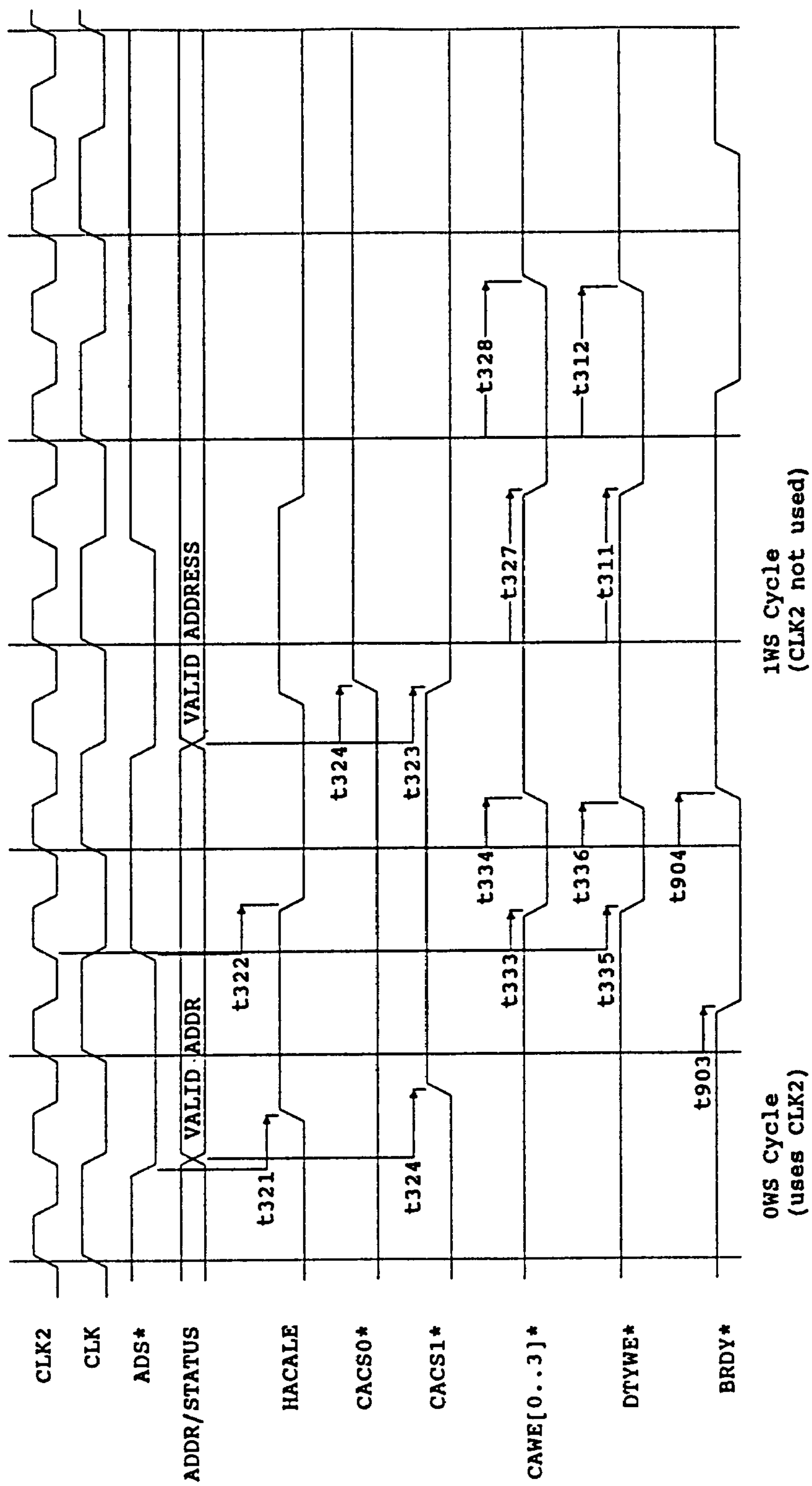
EISA BURST WRITE



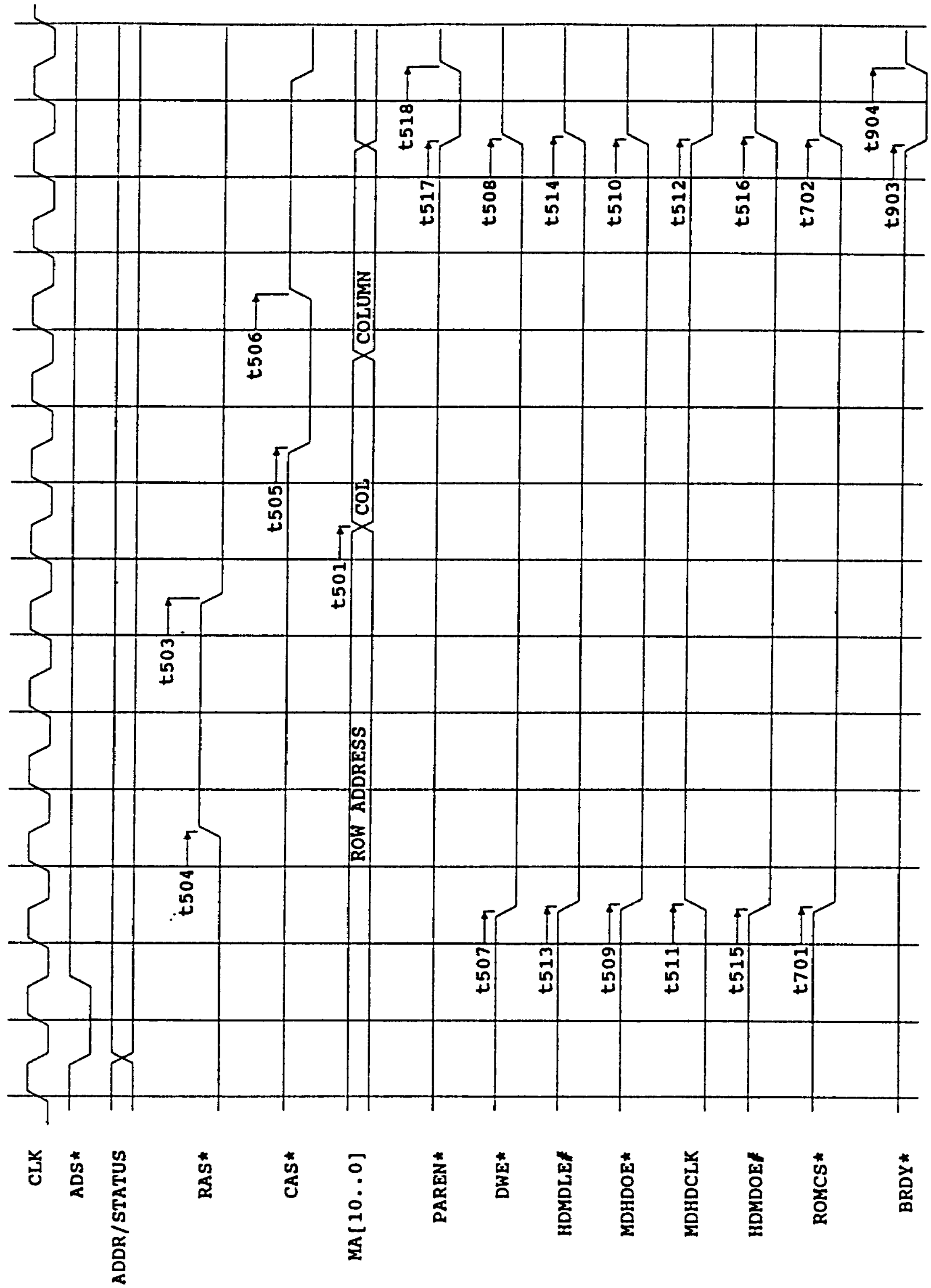
CLOCK TIMING AND RESET



Cache Read Timing



Cache Write Timing


CLK
ADS*
ADDR/STATUS
RAS*
CAS*
MA[10..0]
PAREN*
DWE*
HDMDLE#
MDHDOE*
MDHDCLK
HDMDOE#
ROMCS*
BRDY*
ROW ADDRESS
COL
COLUMN
t504
t503
t505
t506
t501
t507
t513
t509
t511
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t701
t517
t518
t508
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t510
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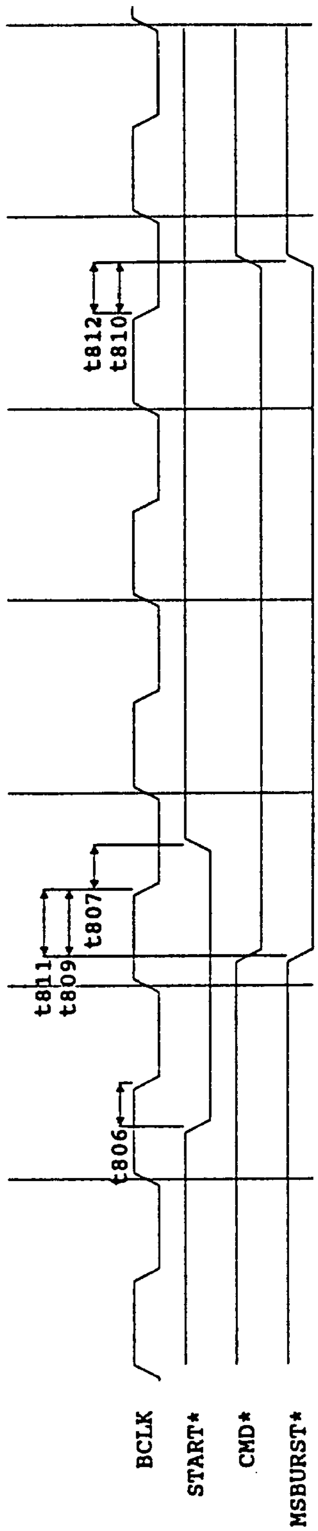
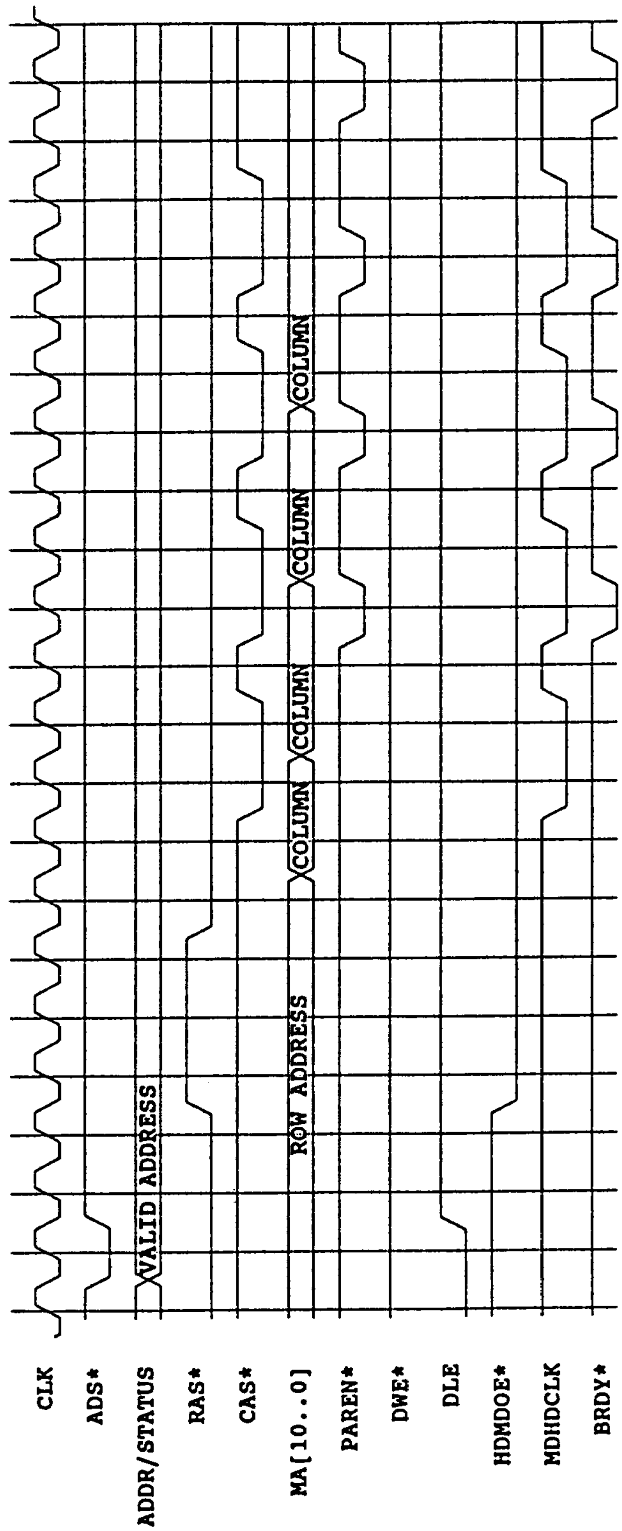
t702
t903
t904

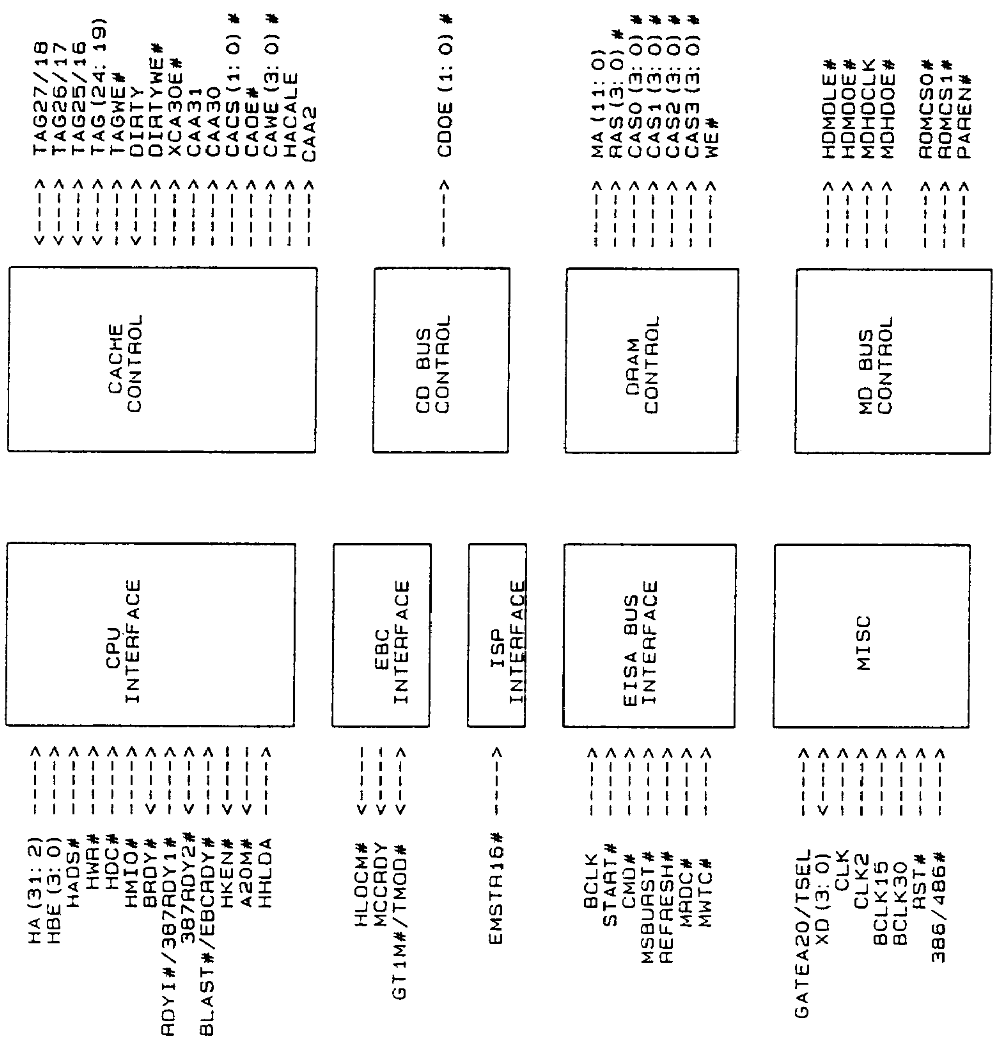
DRAM TIMING



EISA TIMING



DRAM READ PAGE MISS OWS



MCC BLOCK DIAGRAM

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2.5.1 82C682, MCC Numerical Pin Cross Reference

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	Vss	41	HWR#	81	Vss	121	CAS33#
2	BCLK	42	HM/IO#	82	XCA30E#	122	CAS23#
3	GT1M#/TMOD#	43	HADS#	83	CAA31	123	CAS13#
4	HLOCM#	44	A2	84	CAA30	124	CAS03#
5	MCCRDY	45	A3	85	CACS1	125	Vss
6	BCLK15	46	A4	86	CACS0	126	CAS32#
7	RDYI#/387RDY1#	47	A5	87	DIRTY	127	CAS22#
8	REFRESH#	48	A6	88	DIRTYWE#	128	CAS21#
9	BCLK30	49	A7	89	CAA2	129	CAS20#
10	Vss	50	Vss	90	Vss	130	Vss
11	RST#	51	A8	91	CDOE1#	131	CAS31#
12	NC	52	A9	92	CDOE0#	132	CAS21#
13	START#	53	A10	93	NC	133	CAS11#
14	CMD#	54	A11	94	NC	134	CAS01#
15	MSBURST#	55	A12	95	TAGWE	135	Vss
16	MRDC#	56	A13	96	TAG24	136	CAS30#
17	MWTC#	57	A14	97	TAG23	137	CAS20#
18	HHLDA	58	A15	98	TAG22	138	CAS10#
19	EMSTR16#	59	A16	99	TAG21	139	CAS00#
20	VDD	60	A17	100	VDD	140	VDD
21	CLK	61	VDD	101	TAG20	141	MA11
22	NC	62	A18	102	TAG19	142	MA10
23	XD3	63	A19	103	TAG18/27	143	MA9
24	XD2	64	A20	104	TAG17/26	144	MA8
25	XD1	65	A21	105	TAG16/25	145	Vss
26	XD0	66	A22	106	CAOE#	146	MA7
27	GATEA20/TSEL	67	A23	107	CAWE3#	147	MA6
28	NC	68	A24	108	CAWE2#	148	MA5
29	CLK2	69	A25	109	CAWE1#	149	MA4
30	VDD	70	Vss	110	VDD	150	Vss
31	ROMCS0#	71	A26	111	CAWE0#	151	MA3
32	ROMCS1#	72	A27	112	NC	152	MA2
33	387RDY2#	73	A28	113	NC	153	MA1
34	HDC#	74	A29	114	Vss	154	MA0
35	HBE0#	75	A30	115	HDMDOE#	155	386/486#
36	HBE1#	76	A31	116	HDMDLE#	156	WE#
37	HBE2#	77	BLAST#	117	MDHDCLK	157	RAS3#
38	HBE3#	78	BRDY#	118	MDHDOE#	158	RAS2#
39	A20M#	79	HKEN#	119	PAREN#	159	RAS1#
40	Vss	80	HACALE	120	Vss	160	RAS0#

2.5.2 82C682, MCC Alphabetical Pin Cross-Reference

Name	Pin	Name	Pin	Name	Pin	Name	Pin
386/486#	155	CAA31	83	HDC#	34	ROMCS0#	31
387RDY2#	33	CACS0	86	HDMDLE#	116	ROMCS1#	32
A10	53	CACS1	85	HDMDOE#	115	RST#	11
A11	54	CAOE#	106	HHLDA	18	START#	13
A12	55	CAS00#	139	HKEN#	79	TAG16/25	105
A13	56	CAS01#	134	HLOCM#	4	TAG17/26	104
A14	57	CAS02#	129	HM/IO#	42	TAG18/27	103
A15	58	CAS03#	124	HWR#	41	TAG19	102
A16	59	CAS10#	138	MA0	154	TAG20	101
A17	60	CAS11#	133	MA1	153	TAG21	99
A18	62	CAS12#	128	MA10	142	TAG22	98
A19	63	CAS13#	123	MA11	141	TAG23	97
A2	44	CAS20#	137	MA2	152	TAG24	96
A20	64	CAS21#	132	MA3	151	TAGWE	95
A20M#	39	CAS22#	127	MA4	149	VDD	20
A21	65	CAS23#	122	MA5	148	VDD	30
A22	66	CAS30#	136	MA6	147	VDD	61
A23	67	CAS31#	131	MA7	146	VDD	100
A24	68	CAS32#	126	MA8	144	VDD	110
A25	69	CAS33#	121	MA9	143	VDD	140
A26	71	CAWE0#	111	MCCRDY	5	Vss	1
A27	72	CAWE1#	109	MDHDCLK	117	Vss	10
A28	73	CAWE2#	108	MDHDOE#	118	Vss	40
A29	74	CAWE3#	107	MRDC#	16	Vss	50
A3	45	CDOE0#	92	MSBURST#	15	Vss	70
A30	75	CDOE1#	91	MWTC#	17	Vss	81
A31	76	CLK	21	NC	12	Vss	90
A4	46	CLK2	29	NC	22	Vss	114
A5	47	CMD#	14	NC	28	Vss	120
A6	48	DIRTY	87	NC	93	Vss	125
A7	49	DIRTYWE#	88	NC	94	Vss	130
A8	51	EMSTR16#	19	NC	112	Vss	135
A9	52	GATEA20/TSEL	27	NC	113	Vss	145
BCLK	2	GT1M#/TMOD#	3	PAREN#	119	Vss	150
BCLK15	6	HACALE	80	RAS0#	160	WE#	156
BCLK30	9	HADS#	43	RAS1#	159	XCA30E#	82
BLAST#	77	HBE0#	35	RAS2#	158	XD0	26
BRDY#	78	HBE1#	36	RAS3#	157	XD1	25
CAA2	89	HBE2#	37	RDYI#/387RDY1#	7	XD2	24
CAA30	84	HBE3#	38	REFRESH#	8	XD3	23

3. 82C681, OPTi EISA BUS CONTROLLER (EBC)

3.1 FEATURES

The EISA Bus Controller (EBC) is a 160-pin PFP (Plastic Flat Package) device capable of operation in both 386 and 486 mode. It generates the EISA bus clock (BCLK) as well as the keyboard clock while also providing board level and CPU/Coprocessor reset signals. In addition, the EBC controls the interface between the EISA bus and the Host bus and arbitrates between Host/ EISA/ISA Masters, DMA controllers, and Refresh requests for the EISA bus. It directs the steering logic of the DBC and the ISP and provides latch/buffer controls for address/data byte lane translation/swapping. Additionally, it provides the address translation between masters and slaves for addresses A20 and A[1:0]. Some of the features of the EBC include:

* 160-pin PFP (Plastic Flat Package)
* Clock generator logic for EISA bus clock and keyboard clock
* Reset control including Fast CPU warm reset
* Supports 486DX, 486SX and 386DX processors
* Supports 80387/3167/4167/487SX numeric coprocessors
* Provides interface between Host and EISA/ISA bus
* Supports EISA bus Arbitration controls from the ISP
* Provides control signals for EISA Bus Buffers/Latches (EBB)
* Provides EISA/ISA bus cycle compatibility including Burst mode
* Supports 32-bit, 16-bit and 8-bit DMA cycles - Type A, B or C (Burst)
* Provides EISA/ISA bus translation between master, slave or DMA devices for 32-bit, 16-bit, and 8-bit cycles
* Supports Host/EISA Refresh cycles (including hidden refresh)
* Built-in tristate test mode enhances manufacturability

3.1.1 Clock generation

The single-phase version of the host CPU clock drives the EBC's CLKIN input. This is the same frequency as an installed 486 CPU and half the frequency of a 386 host CPU. An external clock generator controls the buffering and skew of this clock so that it is in phase with the CPU and the MCC.

The EBC generates approximately an 8 MHz EISA bus clock signal BCLKOUT. The EBC divides the CLKIN signal by an appropriate amount, (based on the external speed strapping pins SPEED1# and SPEED0#) to produce this BCLKOUT signal. BCLKOUT is buffered externally (typically by an EBB) to provide the required drive of the EISA bus. The EBC samples the actual EISA bus clock, BCLK, through its BCLKIN input in order to internally synchronize and drive EISA bus logic. This mechanism allows the EBC to always sample the actual EISA bus clock even if the EBC is not the source. The signals BCLK15 and BCLK30 are derived via an external delay element and are used by the EBC (and the MCC) to help relax EISA bus timing requirements.

The EBC also generates the keyboard clock for the 8042/8742 (CLKKB and CLKKB#) in order to eliminate an external clock source.

The following table illustrates the relationship between CLKIN and BCLKOUT:

CLKIN	SPEED[1:0]#	BCLKOUT	BCLKIN
20 MHz	11	6.67 MHz*	8-10 MHz*
25 MHz	11	8.33 MHz	8.33 MHz
33 MHz	10	8.25 MHz	8.25 MHz
40 MHz	01	8.0 MHz	8.0 MHz
50 MHz	00	8.33 MHz	8.33 MHz

* At 20 MHz, an external clock source may be used for BCLK in order to boost the EISA bus frequency to 8-10 MHz as shown.

3.1.2 Reset Control

The reset control logic generates three output control signals based on the following input stimuli:

1. RST#: This is the board level reset output that is used to drive the RST# inputs of the EBC, ISP, MCC, DBC and the keyboard controller. It is asserted whenever the power good signal (PWRGD) signal is low (power-on/off) and whenever the external reset switch is depressed (RESETSW# active). This reset synchronizes the host devices on the motherboard. RST# is buffered in the ISP to provide the EISA bus reset signal.

2. RSTCPU: This signal resets the host CPU and is usually referred to as the "warm reset". RSTCPU is always active along with the system reset signal RST#. In addition, there are two other cases that cause RSTCPU to occur. The first is during CPU shutdown cycles, decoded from the CPU status/control lines and the byte enables. The second is from warm resets initiated by I/O writes to the keyboard controller's reset port. The OPTi EISA chipset greatly speeds up this process by emulating the reset function in the keyboard controller. The MCC intercepts reset instructions to the 8042 and responds by generating the ARMRC# signal to the EBC. The EBC will then issue the RSTCPU instruction upon execution of the next HLT instruction (typically the instruction immediately following the I/O instruction). This "fast CPU warm reset" boosts performance of programs that switch in and out of protected mode.

3. RST387: This reset is used by a host 80387 coprocessor. This signal goes active with RST# as well as during I/O writes to port F1h.

3.1.3 Host bus Interface

The EBC interfaces directly with the local CPU (386, 486 or 486SX) on the Host bus. This interface is used to track host bus cycles when the CPU or other local device is the current master on the host bus. When a host cycle is initiated, the EBC checks to see whether any local slave is responding. If a local device is not the target of the cycle, then the EBC will activate the EISA/ISA interface logic to complete the instruction. The EBC waits until the completion of the EISA/ISA portion of the cycle before terminating the cycle on the host bus.

The EBC also contains the glue logic required to interface the host CPU with a numeric coprocessor. The EBC supports the 80387 and 80487SX, as well as the Weitek 3167 and 4167 coprocessors. Interrupt, busy, error and coprocessor detection logic that is typically included in external PALs has been integrated into the EBC.

3.1.4 EISA/ISA Bus Interface

The EISA/ISA interface monitors cycles initiated by EISA or ISA masters and watches their corresponding busses to detect a slave response. The correct cycle will then be generated on the responding slave's bus (EISA or ISA). The EISA/ISA interface accepts cycles from the host interface and will run the appropriate cycles on the EISA or ISA bus. If necessary, the EISA/ISA interface will perform multiple cycles (assembly/disassembly) for every host cycle. When this translation is completed, the host interface is informed to terminate the cycle on the local bus. The EISA/ISA interface will also inform the host interface when the host can change the address for the next cycle.

3.1.5 Data/Address Control

The EBC controls the data buffers between the host bus and the EISA data bus. MDLE#, MDHDOE1#, LDMDOE#, MDSDOE#, and SDOE# provide the latching clocks and output enables used by the steering logic in the DBC and the ISP

The control lines CPY01#, CPY02#, CPY03#, CPY13#, and CPYUP are used in the data bus assembly/disassembly logic when a master and slave are different widths. These signals connect directly to an EBB or to external transceivers.

The LA/SA, and LA/HA address steering is done with either an EBB or with external buffers and latches. The EBC provides the control signals to direct this address logic.

3.1.6 EISA bus compatibility

The EBC is responsible for generating EISA bus compatible cycles including bursting to and from the EISA bus. Bus cycle compatibility is maintained by controlling bus translations and address/data latching for the following cases as well as any cycle involving mismatched source and destination sizes:

- Host master to an EISA/ISA/ISP slave
- EISA master to an SA/ISP slave
- 32-bit EISA master to a 16-bit EISA slave
- ISA master to an EISA slave
- DMA from EISA/ISA memory
- Refresh to EISA/ISA memory
- EISA/ISA/DMA accesses to a Host slave

3.1.7 Refresh

The EBC supports two types of refresh protocols, classical AT refresh and hidden refresh. Classical AT refresh is performed by placing the host processor in hold while the refresh controller completes the EISA bus refresh. This method maintains compatibility with older AT architectures, but has the performance disadvantage of losing processor bandwidth when the CPU is put into hold.

Superior performance is gained when hidden refresh is enabled. This method allows refresh cycles to take place on the EISA bus while the host CPU continues to execute instructions. As long as the host does not try to access the EISA bus, the refresh operation remains transparent to the CPU. If the CPU does try to gain access to the bus during a hidden refresh, the host cycle is simply delayed until the completion of the refresh. The effectiveness of hidden refresh varies with each application (EISA bus intensive programs will benefit less than host bus intensive programs), however hidden refresh always yields better performance than classical AT refresh because the Hold/Hold Acknowledge latency is eliminated.

3.1.8 Testability

I/O configuration register C13h <3:0> contains a 4-bit read only value that indicates the revision level of the EBC. This allows the revision level of the EBC to be verified by software.

The EBC includes a tristate test mode to enhance board level testability/manufacturability. When this test mode is entered, all outputs and bidirectional pins become tristated, allowing electrical isolation between the EBC and signals on the PCB.

At the trailing edge of the motherboard reset (RST#), the EBC samples two pins to determine whether the tristate test mode should be entered. CPUMISS#/TMOD# must be low and IO16#/TSEL must be high at this sample point to guarantee entering this test state. The following table illustrates this:

CPUMISS#/ TMOD#	IO16#/ TSEL	Function
Low	Low	Reserved
Low	High	Tristate Test Mode
High	X	Normal Operation

3.2 EBC PIN DESCRIPTION

3.2.1 Host Bus Interface

Name	Type	Pin No	Description
386/486#	I	79	***CPU Select.*** Hardware strapping pin to distinguish between 386 and 486 Host CPUs. Tied high for a 386 Host and low for a 486 Host.
HADS#	I	119	***Host Address Strobe.*** A host initiated bus cycle is started from the EBC after HADS# has been sampled low and then high. Connected to ADS# from the host CPU.
HD/C#	B	132	***Host Data / Control.*** The CPU drives this signal during host originated cycles and the EBC decodes HD/C# (along with HW/R# and HM/IO#) to determine the type of cycle in process. The EBC drives this line high during EISA/ISA/DMA master cycles. HD/C# is connected to the Host CPU D/C# pin.
HW/R#	B	122	***Host Write / Read.*** The EBC treats this signal as an input during Host CPU and DMA cycles and decodes it (along with HD/C# and HW/R#) to determine the cycle type in process. HW/R# becomes an output during master cycles based on SW/R# for EISA masters and on MWTC# or IOWC# for ISA master cycles. This signal is connected to the ISP HW/R# pin and the CPU W/R# pin.
HM/IO#	B	120	***Host Memory / IO.*** The CPU drives this signal during host originated cycles and the EBC decodes HM/IO# (along with HW/R# and HD/C#) to determine the type of cycle in process. The EBC drives line this during master cycles based on SM/IO# for EISA masters and based on IORC# or IOWC# for ISA masters. This signal is driven high during DMA cycles. HM/IO# is connected to the Host CPU's M/IO# pin.
HHOLD	O	111	***Host Hold.*** This signal is driven active when synchronized DHOLD or SLOWH# are active. It is also driven high during normal refresh cycles when Hidden Refresh is disabled (Reg C11h<0>=0 or C30h<1>=0). HHOLD is connected to the Host CPU's HOLD input.
HHLDA	I	133	***Host Hold Acknowledge.*** This is the acknowledgement from the CPU that it has given up the Host bus in response to HHOLD. The EBC uses this signal to generate RDHLDA to the ISP and the DBC. It is connected to the Host CPU's HLDA pin.
WCS#	I	83	***Weitek Chip Select.*** Typically used to decode a local coprocessor such as the Weitek 3167or 4167. If sampled active, the EBC assumes a local bus cycle is in process and inhibits the generation of EISA/ISA cycles. It is only sampled during Host initiated cycles. Typically connected to MCS# from the 3167/4167.
HLOCM#	I	135	***Host Local Memory.*** This input tells the EBC that the accessed memory is local to the Host. During Host initiated memory access, this signal is sampled with the same timing as WCS# for 20/25/33 MHz systems and one CLKIN later otherwise. If active, the EBC inhibits the generation of an EISA/ISA memory cycle. During non Host initiated memory cycles, if HM/IO# is high, it is sampled at the same time as EX32# and the EBC assumes a 32-bit EISA memory access to the Host bus. HLOCM# is connected to the HLOCM# output of the MCC.

HLOCDEV#	I	103	***Host Local Device.*** Local devices on the Host bus must drive this signal to inform the EBC that they are claiming the cycle in progress. During Host initiated cycles, this signal is sampled at the same time as HLOCM#. If active, the EBC assumes a local cycle and inhibits the generation of an EISA/ISA cycle. During all other memory or I/O cycles, HLOCDEV# is sampled at the same time as EX32# and if active, the EBC assumes a 32-bit EISA device on the Host data bus. It is connected to the decoding logic of any local device.
NPRDY#	I	89	***Numeric Processor Ready.*** This input samples the numeric coprocessor's ready output pin and is tied directly to the 387/3167/4167/487SX READYO# pin.
LOCRDY#	I	2	***Host Local Ready.*** An additional ready input for local devices in 486 mode. This pin has a weak internal pull-up and may be left unconnected. Its timing is similar to NPRDY#.
HRDYO#	O	115	***Host Ready Out.*** For 486 systems, this pin is connected to the CPU's ready input. For 386 systems, this pin is connected to the MCC's ready input (BLAST#/EBCRDY#). The EBC drives this line low for one CLKIN at the end of all host-CPU cycles unless HLOCM#, WCS# or HLOCDEV# indicate a host-bus device. The EBC will also drive HRDYO# active (low) after NPRDY is sampled active as well as during 387 cycles when the coprocessor is not present. After driving HRDYO# low, the EBC will drive this signal high for one CLKIN cycle before tristating it to help the external pull-up resistor guarantee proper voltage levels to the CPU.
DELRDY	I	80	***Delayed Ready.*** When tied low, it indicates standard HRDYO# timing. When tied high it indicates that HRDYO# is delayed by one CLKIN.
HLOCK#	I	112	***Host Bus Lock.*** The CPU drives this pin to indicate that the current bus cycle is locked. This is used to generate SLOCK# for the EISA bus. HLOCK# is connected to the MCC HLOCK# pin and the CPU LOCK# output.

3.2.2 Host-Bus/Numeric Processor Interface

Pin Name	Type	Pin No.	Description
BREQ/HA31	I	113	***486 Bus Request or 386 Host Address A31.*** The function of this pin is determined by the CPU installed. For 486 systems, it indicates that the 486 is requesting control of the Host bus. The EBC uses this signal to generate CPUMISS#. In 386 systems, HA31 allows the EBC to decode 387 accesses at the top of I/O space. This signal is connected directly to the corresponding pin of the appropriate CPU.
HKEN#/ NPBUSY#	I	104	***Host Cache Enable or Numeric Coprocessor Busy.*** The function of this pin is determined by the CPU installed. For 486 systems, HKEN# is connected to the 486 KEN# pin and is sampled to override HBE[3:0]# during 486 reads. For 386 systems, NPBUSY# is connected directly from the coprocessor and is used to generate 386BUSY#, 386PEREQ and NPINT. Connected to 486 KEN# or 387 BUSY#.

NPERR#	I	88	***Numeric Coprocessor Error.*** For 486 systems, it is connected to the 486 or 487SX FERR# output and is used to generate IGERR# and NPINT. For 386 systems, this signal is connected the 387 ERROR# output and is used along with NPBUSY# to generate 386BUSY#, 386PEREQ and NPINT. It is also used to detect the presence of a 387 while the RSTCPU signal is active. This information is passed on to the processor via the 386ERR# signal.
WINT/ NPPEREQ	I	87	***Weitek Interrupt or Numeric Coprocessor Extension Request.*** In all 486 systems, and in those 386 systems with a 3167or 4167 numeric coprocessor installed, this input is connected to the numeric coprocessor's interrupt signal (INTR). The EBC uses WINT in the logic that generates the numeric processor interrupt output (NPINT). In 386 systems with a 387 numeric coprocessor installed, the numeric coprocessor extension request signal (PEREQ) is connected to this pin on the EBC. NPPEREQ is used by by the EBC to help generate the 386 processor extension request output (386PEREQ).
EADS#	O	117	***External Address Status.*** EADS# is used by the 486 to monitor whether any external device has driven its address onto the Host bus. The CPU then will invalidate the corresponding internal cache line in order to maintain coherency. The EBC drives EADS# active for one CLKIN cycle, when the HA bus is stable, for every memory write by an EISA/ISA/DMA master. EADS# is not driven for read cycles. This output is connected to the 486 EADS# input and is not used for 386 systems.
386PEREQ	O	106	**386 Processor Extension Request.** This signal instructs the 386 that the 387 has operands ready to transfer. It is connected directly to the PEREQ input of the 386 and it is not used by 486 systems.
IGERR#/ 386ERR#	O	114	***Ignore Numeric Processor Error or 386 Error.*** In 486 systems, IGERR# goes active when NPCS#and IOWC# are low and SA0 is high (write to port 0F1h) and stays active as long as NPERR# is active. It is connected to the IGNNE# input of the 486. For 386 systems this line reflects the 387 ERROR# status and is also used by the CPU to detect the presence of a 387. If a 387 is installed, this line will be driven low from the leading edge of RSTCPU until the first bus cycle. It is connected to the ERROR# input of the 386.
386BUSY#	O	118	***386 Busy.*** This output is only used in 386 systems. 386BUSY# is active whenever the 387 is busy or when a coprocessor error condition has occurred. 386 BUSY# is also It is connected to the 386 BUSY# input.
NPINT	O	78	***Numeric Coprocessor Interrupt.*** This output is connected to IRQ13 of the ISP. It goes active on coprocessor errors (NPERR#) and inactive when reset by an I/O write to port F0h (NPCS#, IOWC# and SA0 all low).

3.2.3 ISP/MCC Interface

Pin Name	Type	Pin No.	Description
DHOLD	I	73	***Delayed Hold Request.*** This is a request for the Host and EISA bus, generated when the ISP wants to transfer control to an EISA/ISA/DMA master. DHOLD is used to generate HHOLD and will never be active at the same time as refresh request (REFRQ). It is connected to DHOLD from the ISP.
REFRQ	I	72	***Refresh Request.*** It is never active along with DHOLD. If hidden refresh is disabled (Reg C11h<1>=0 (default) or RegC30h<1>=0 (default)), this input is used in the same way as DHOLD to request control of the Host and EISA busses during a refresh cycle. However, if Hidden refresh is enabled (Reg C11h<1>=1 AND C30h<1>=1) then the EBC generates RDHLDA at the end of any ongoing CPU cycle. Hidden refresh to the EISA bus will then be performed in parallel with ongoing CPU activity and any new CPU cycle to the EISA bus will be kept waiting until the bus refresh is over. This input is connected to REFRQ from the ISP.
SLOWH#	I	54	***Slowdown Hold Request.*** This is one of several inputs that cause the EBC to generate HHOLD. Since 486 systems are intolerant of frequency changes, this signal provides an alternate method of making the CPU appear to slow down. SLOWH# is generated by the ISP in order to reduce the CPU bandwidth so that it is compatible with older software. SLOWH# will toggle on and off depending on the rate that the ISP chooses to slow down the system. The method also works with 386 systems. This input is connected to the SLOWH# output of the ISP.
MCCRDY	I	134	***MCC Ready.*** This input indicates that the MCC is ready to accept a new cycle. This normally active (high) input goes inactive (low) when a hidden refresh cycle is pending and returns active when the refresh cycle is over. RDHLDA is not allowed to make low to high transitions while MCCRDY is inactive. It is connected to the MCCRDY output of the MCC.
RDHLDA	O	96	***Refresh or Delayed Hold Acknowledge.*** RDHLDA is driven active in response HHLDA from the CPU based on either DHOLD or REFRQ if hidden refresh is disabled. It remains active as long as DHOLD is active. Also, when hidden refresh is enabled, (RegC11h<1>=1 AND RegC30h<1>=1), REFRQ will cause this output to go active as soon as any pending cycle to the EISA bus is completed. In this case, RDHLDA will remain active as long as REFRQ is active. This output is connected to RDHLDA of the ISP and the DBC
CPUMISS#/ TMOD#	B	75	***CPU Miss or Test Mode.*** This pin serves two functions. Normally, CPUMISS# indicates that a host access (HLOCDEV#, WCS# and HLOCM# are inactive) to the EISA bus is pending during a hidden refresh cycle. It is only driven active during RDHLDA. It is also active in response to HHOLD or BREQ and is connected to the CPUMISS# input of the ISP. The second function of this pin is to force the EBC into test mode. The EBC will enter its tristate test mode when this pin is sampled low on the trailing edge of PWRGD or RESETSW# AND IO16#/TSEL is high. CPUMISS#/TMOD# is tristated when PWRGD or RESETSW# is low and a weak internal pull-up keeps it high when no outside source is driving it.

ST[3:0]	B	64,65, 66,67	***Inter-Chip Status bus.*** Inter-chip communication bus between the EBC and the ISP to reflect EISA/ISA/DMA control information. Connected to ST[3:0] of the ISP.
DRDY	B	68	***Delayed Ready.*** DRDY is active during DMA or refresh cycles. It works in conjunction with ST[3:0] and is connected to DRDY of the ISP.
EXMASTER#	I	76	***EISA Master.*** This indicates that an *EISA* master is in control of the bus. Connected to EXMASTER# from the ISP.
EMSTR16#	I	62	***ISA Master.*** This indicates that an *ISA* master is in control the bus. Connected to EMSTR16# from the ISP.

3.2.4 ISA Bus Interface

Pin Name	Type	Pin no.	Description
BALE	0	25	***Buffered Address Latch Enable.*** Externally buffered ('244 or EBB) to drive BALE of the EISA connectors and the latch enable signal for the SA[19:17] latch. It is driven high during the second half of START# for Host/EISA master cycles and is always high during DMA/ISA/Refresh cycles.
CHRDY CHRDYA	B T	9 10	***EISA Channel Ready.*** Connected to CHRDY of the EISA connectors. The EBC pulls this line low for ISA master I/O cycle or access to EISA memory with the leading edge of ISACMD (MRDC#, MWTC#, IORC# or IOWC#).
GT16M#	I	74	***Greater than 16 MB.*** The ISP drives this line active for DMA addresses greater than 16 MB. For compatible DMA cycles, the ISA memory commands are inhibited if an EISA memory resource responds when GT16M# is active. It is inactive during refresh and is connected to the GT16M# output from the ISP.
M16# M16A#	B T	18 19	***ISA 16-bit Memory Capability.*** The EBC pulls both M16# and M16A# low during ISA master cycles based on HLOCM#, EX16# or EX32#. It samples this line during Host/EISA/DMA access to ISA memory to determine the data width and default cycle time. These pins are connected M16# on the EISA connectors.
IO16#/TSEL	I	30	***ISA 16-bit I/O.*** This pin serves two functions. Normally, the EBC samples this line during Host/EISA accesses to ISA I/O in order to determine the data-width and default cycle time. It is connected to IO16# of the EISA connectors. The second function of IO16#/TSEL is to force the EBC into test mode. The EBC will enter its tristate test mode when this pin is sampled high on the trailing edge of PWRGD or RESETSW# AND CPUMISS#/TMOD# is low.
NOWS#	I	21	***No Wait State.*** The EBC samples this for Host/EISA(DMA) cycles to ISA-slaves (memories) on the falling edge of BCLKIN to shorten default cycles if CHRDY is high. It is connected to NOWS# of the EISA connectors.

MRDC#	B	43	***Memory Read Command***. This is an output of the EBC during Host/EISA/DMA and refresh cycles. This signal is driven active for all these memory reads except during Burst DMA reads or when EX16# or EX32# are sampled active. The EBC also drives MRDC# active during all Compatible DMA reads when GT16M# is inactive. MRDC# is an input during ISA master cycles. It is connected to MRDC# of the EISA connectors through a 74F245 transceiver (or EBB).
MWTC#	B	45	***Memory Write Command.*** This is an output fo the EBC during Host/EISA/DMA and refresh cycles. It drives this signal active for all memory writes except Burst DMA or when EX16# or EX32# are sampled active. The EBC also drives MWTC# active during all Compatible DMA writes when HGT16M# is inactive. MWTC# is an input during ISA master cycles. It is connected to MWTC# of the EISA connectors through a 74F245 transceiver (or EBB).
IORC#	B	46	***I/O Read Command.*** This signal is an output during Host/EISA/DMA/Refresh master cycles and is driven active during I/O reads. It is an input for ISA master cycles. IORC# is connected to IORC# of the EISA connectors through a 74F245 transceiver (or EBB).
IOWC#	B	47	***I/O Write Command.*** This signal is an output during Host/EISA/DMA/Refresh master cycles and is driven active during I/O writes. It is an input for ISA master cycles. IOWC# is connected to IOWC# of the EISA connectors through a 74F245 transceiver (or EBB).
GT1M#	I	136	***Greater than 1MB***. GT1M# goes active for addresses greater than 1MB. This signal is used to generate SMEMR# and SMEMW#. It is connected to GT1M# from the MCC.
SMEMR#	O	24	***System Board Memory Read***. Goes active for memory reads to addresses below 1MB (GT1M# is inactive) when MRDC# is active or REFRESH# is active. Buffered (EBB) to drive SMEMR# of the EISA connectors.
SMEMW#	O	23	***System Board Memory Write***. Goes active for memory writes to addresses below 1MB (GT1M# is inactive) when MRDC# is active or REFRESH# is active. Buffered (EBB) to drive SMEMW# of the EISA connectors.
REFRESH#	I	55	***Refresh***. It indicates that a refresh cycle is in progress. Connected to REFRESH# of the EISA connectors and to the ISP.
MASTER16#	I	5	***16-bit Master***. It indicates that a 16-bit EISA/ISA master is in control of the bus. For EISA masters, if it is sampled low at the BCLKIN rising edge where command goes active (after being sampled high one BCLKIN earlier), the EBC assumes a downshifting master and aborts all copying and assembly / disassembly for 16-bit burst slaves. It is connected to MASTER16# of the EISA connectors.

3.2.5 EISA-Bus Interface

Pin Name	Type	Pin No.	Description
SM/IO# SM/IOA#	B T	148 149	***System Memory / IO.*** The EBC drives these lines during Host master cycles (based on HM/IO#), ISA master cycles (based on IORC# or IOWC#) and DMA /Refresh (always high). They are connected to M/IO# of the EISA connectors.
SW/R# SW/RA#	B T	8 7	***System Write / Read.*** The EBC drives these lines during Host/DMA master cycles (based on HW/R#), ISA master cycles (based on MWTC# or IOWC#) and Refresh (always low). They are connected to W/R# of the EISA connectors.
SLOCK# SLOCKA#	B T	35 36	***Bus Lock.*** The host or bus master asserts LOCK# to guarantee exclusive memory access during the time LOCK# is asserted. This is an output from the EBC during host master cycles. It is driven active from the BCLKIN falling edge during START# to the BCLKIN falling edge after CMD# going inactive during Host cycles for which HLOCK# is asserted. It is connected to LOCK# of the EISA connectors.
START# STARTA#	B T	95 94	***Cycle Start.*** START is an output for Host/ISA/DMA/Refresh masters. It is driven active to indicate the beginning of an EISA cycle for all these cases except for Host master cycles when HLOCM#, WCS# or HLOCDEV# has indicated a host-bus device has been decoded on the local bus. It is also an output for assembly/disassembly cycles of an EISA master and is driven active to indicate the beginning of such cycles. For host generated back-to-back I/O cycles (or INTA) to ISA devices (including assembly/disassembly cycles), extra delay is inserted between the trailing edge of the last IORC#/IOWC# and the leading edge of the next START#. The EBC's I/O delay register (C12h<3:0>) determines the number of BCLK delays to be inserted between such cycles. Delays are programmed based on 8-bit and 16-bit accesses. START# and START#A are connected to START# of the EISA connectors.
CMD#	O	22	***Command.*** CMD# provides timing control within a cycle. It is driven active from the BCLKIN rising edge when START# is low to the BCLKIN rising edge when MSBURST# is sampled high after EXRDY is sampled high. CMD# may be wider during DMA cycles and the trailing edge occurs with the BCLKIN falling edge for DMA reads. It is buffered (EBB) to drive CMD# of the EISA connectors.
EXRDY EXRDYA	B T	16 17	***EISA Bus Ready.*** It is sampled on the falling edge of BCLKIN when CMD# is active if EX16# or EX32# is also active and used to insert wait-states. Connected to EXRDY of the EISA onnectors.
MSBURST# MSBURSTA#	B T	152 151	***Master Burst Capability.*** This is an output for Host master cycles to indicate to the slave device that the CPU can provide burst cycles. For DMA cycles, this signal is asserted if SLBURST# is active (ie: the EBC will burst if the slave supports it). MSBURST# becomes an input and is sampled by the EBC to terminate EISA CMD# at the end of Burst EISA transfers. Connected to MSBURST# of the EISA Connectors.
SLBURST# SLBURSTA#	B T	11 12	***Slave Burst Capability.*** SLBURST# is sampled during DMA (burst) master cycles. It is driven active for EISA/DMA cycles if HLOCM# is active (ie: local memory can burst to the EISA bus). Connected to SLBURST# of the EISA connectors.

EX32# EX32A#	B T	15 14	***32-bit EISA Capability*.** . The EBC samples EX32# to determine whether a slave supports 32-bit transfers for Host EISA cycles. The EBC drives EX32# low during EISA master cycles based on HLOCM# (ie: local memory supports 32-bit transfers across the EISA bus). Connected to EX32# of the EISA connectors
EX16# EX16A#	B T	29 28	***16-bit EISA Capability*.** The EBC samples EX16# to determine whether a slave supports 16-bit transfers for Host EISA cycles. The EBC drives this line low on the BCLKIN falling edge at the end of assembly/disassembly cycles for 16-bit EISA masters. Connected to EX16# of the EISA connectors.

3.2.6 Clocks

Pin Name	Type	Pin No.	Description
CLKIN	I	108	***Clock Input*.** Master single-phase CPU clock driven from an external clock-generator circuit. For 486 systems, this is the same as the CPU clock. For 386 systems, this is the single-phase version of the CPU CLK2 (half the frequency of the CPU clock).
SPEED[1:0]#	I	82,81	***CPU Speed*.** These two pins indicate the CPU frequency as follows: SPEED[1:0]# FREQUENCY 11 20, 25 MHz 10 33 MHz 01 40 MHz 00 50 MHz
BCLKOUT	O	27	***Bus Clock Output*.** This BCLK output of the EBC is connected to an external buffer (TTL or EBB) which drives the EISA connectors, ISP and MCC for non-20 MHz systems (20 MHz systems require an external, asynchronous BCLKOUT). The EBC derives this signal by appropriately dividing CLKIN based on the SPEED[1:0] strapping inputs to generate a frequency of approximately 8 MHz. BCLKOUT can be stretched at the beginning of Host Master cycles when START# is asserted by enabling the Asynchronous BCLK stretch option in Reg C11h<2>.
BCLKIN	I	31	***EISA Bus Clock Input*.** This input directly samples BCLK from the EISA bus connectors and is used to internally sample and drive all EISA/ISA synchronous signals.
BCLK15	I	131	***Bus Clock delayed by 15ns*.** Delayed version of BCLKIN from the external delay line.
BCLK30	I	129	***Bus Clock delayed by 30ns*.** Delayed version of BCLKIN from the external delay line.
CLKKB	O	69	***Keyboard Clock X1*.** Drives the 8042/8742 XTAL1. Unstretched 8/10 MHz signal generated by dividing CLKIN.
CLKKB#	O	71	***Keyboard Clock X2*.** Drives the 8042/8742 XTAL2. Unstretched 8/10 MHz signal generated by dividing CLKIN.

3.2.7 Reset Control

Pin Name	Type	Pin No.	Description
PWRGD	I	160	***Power Good.*** Connected to PWRGD from the Power Supply. This is used to indicate that the supply voltage has stabilized at an acceptable level and when low, it forces RST#, RSTCPU and RST387 active.
RESETSW#	I	121	***Reset Switch.*** Connected to an external reset switch. This is used to force RST#, RSTCPU and RST387 active.
ARMRC#	I	139	***Arm the Reset CPU Logic.*** This is used by the EBC to arm the logic that generates the RSTCPU signal upon the detection of the next halt cycle. Connected to ARMRC# from the DBC.
RST#	O	97	***System Reset.*** Drives the reset signal, RST#, to the ISP, MCC, DSC and 8042. It is asserted whenever PWRGD or RESETSW# go low and is de-asserted at the same time as RSTCPU.
RSTCPU	O	110	***CPU Reset.*** The EBC drives a reset signal to the host CPU for the following conditions: when RST# is active, when a host master shutdown cycle is decoded, or when ARMRC# was previously asserted and a halt cycle is decoded. RSTCPU is active for a minimum of 64 CLKINs and its trailing edge is synchronized with CLKIN's falling edge.
RST387	O	92	***387 Reset.*** This signal goes active with RST# as well as when NPCS# , IOWC# and SA0 are asserted (I/O write to port F1). It is connected to the reset input of the 80387.

3.2.8 Data Control

Pin Name	Type	Pin No.	Description
MDLE[2:0]#	O	145,144, 142	***Memory Data Latch Enable.*** These signals are normally inactive. For Host/EISA/DMA master reads, MDLE[2:0]# are active at the same time as CMD#. For EISA/DMA master writes to host devices, MDLE[2:0]# are active from the BCLKIN falling edge during START# until the BCLKIN falling edge after CMD# goes inactive. For ISA master writes, these signals remain active for the duration of MWTC# or from the time IOWC# goes active until the the BCLKIN falling edge following IOWC# inactive. In all these cases, MDLE[2:0] are selectively disabled depending upon the master data width, the byte accessed (based on SBE[3:0]#, SA[1:0] or SBHE#), and whether it is a local slave. Connected MDLE[2:0]# of the DBC.
MDHDOE1#	O	141	***Memory Data to Host Data Output Enable.*** This normally inactive signal, goes active as soon as a Host master read cycle from an EISA/ISA slave is detected, and remains active until the end of the cycle (determined by HRDYO# and DRDY). Connected to MDHDOE1# of the DBC.
LDMDOE#	O	146	***Local Data to Memory Data Output Enable.*** This is a normally inactive signal. For EISA/DMA read assembly cycles, it goes active on the BCLK30 rising edge after the last CMD# goes inactive. For EISA/DMA write disassembly cycles, it goes active at the BCLK15 rising edge and remains active until the BCLKIN falling edge after the last CMD# goes inactive. Connected to LDMDOE# of the DBC.

MDSDOE2# MDSDOE1# MDSDOE0#	O	154 156 159	***Memory Data to System Data Output Enables.*** MDSDOE2# controls SD[31:16], MDSDOE1# controls SD[15:8] and MDSDOE0# controls SD[7:0]. Connected to T/R# input of the transceivers (or EBB) between the SD and MD busses.
SDOE[2:0]	O	153,155, 158	***System Data Output Enables.*** SDOE2# controls SD[31:16], SDOE1# controls SD[15:8] and SDOE0# controls SD[7:0]. Connected to OE# of the transceivers (or EBB) between the SD and MD busses.
CPYO1#	O	38	***Copy 01.*** This is enabled for 8-bit ISA slaves if SA0 is 1 for 16-bit masters or if SA[1:0] is 01b for 32-bit masters. It is also enabled for 8-bit non-compatible DMA if SA0 is 1 for 16-bit memory or if SA[1:0] is 01b for 32-bit memory. Connected to OE# of the transceiver (or EBB) between SD[7:0] & SD[15:8].
CPY02#	O	39	***Copy 02.*** This is enabled for 8/16-bit slaves accessed by 32 bit masters if SA[1:0] is 10b. It is also enabled for 32-bit slave access by 16-bit masters or 8-bit non-compatible DMA when SA[1:0] is 10b. Connected to OE# of the transceiver (or EBB) between SD[7:0] & SD[23:16].
CPY03#	O	41	***Copy 03.*** This is enabled for 8-bit ISA slave access by 32-bit masters and for 32-bit EISA slave access by 8-bit non-compatible DMA when SA[1:0] is 11b. Connected to OE# of the transceiver (or EBB) between SD[7:0] & SD[31:24].
CPY13#	O	4	***Copy 13.*** This is enabled for 16-bit slaves accessed by 32 bit masters when SA1,SBHE# is 10b. It is also enabled for 32-bit slave accesses from 16-bit masters when SA1,SBHE# is 10b. Connected to OE# of the transceiver (or EBB) between SD[15:8] & SD[31:16].
CPYUP	O	3	***Copy Up.*** This normally high signal goes low during reads when the master (I/O for DMA) width is less than the slave width and during writes when the master (I/O for DMA) width is greater than the slave width. Connected to the direction control of the SD transceivers (or EBB).

3.2.9 Address Control

Pin Name	Type	Pin No.	Description
ISAMSTR#	O	51	***ISA Master.*** This is active during EMSTR16# or REFRESH. Connected to OE# of the buffer (or EBB) driving LA[16:2] from SA[16:2].
ISAMSTR	O	49	***ISA Master.*** Connected to OE# of the latch (or EBB) driving SA[19:2] from LA[19:2]. This is the active high version of ISAMSTR#. ISAMSTR and ISAMSTR# are also used to control the T/R# of the transceiver (or EBB) that drives MRDC#, MWTC#, IORC#, IOWC#, SA[1:0] and SBHE#.
HALAOE#	O	52	***HA bus to LA bus Output Enable.*** This normally active signal is inactive when REFRESH# is active. It is also inactive when DHOLD is inactive and HHLDA is active. Connected to OE# of the F640/F245 transceivers (or EBB) between LA[31:2] and HA[15:2].
LAHARD	O	53	***LA bus to HA bus Read.*** This signal sets the direction between the LA bus and the HA bus. Connected to DIR of the F640/F245 transceivers (or EBB) between HA[31:21,19:16] and LA[31:24]#, LA[23:21,19:16].

LASALE#	O	61	***LA Synchronous Address Latch Enable*** This signal is the active low version of BALE. It is connected to the corresponding pin of the DBC and LE# of the latch (or EBB) driving SA[16:2] from LA[16:2].
AENLE#	O	147	***AEN Latch Enable.*** For Host /EISA masters, this normally active signal goes high for accesses to ISA I/O at the BCLKIN rising edge when CMD# goes active. It is connected to AENLE# of the DBC.
HBE[3:0]	B	125,126, 127,128	***Host Byte Enables.*** The EBC drives these signals during EISA/ISA/DMA master cycles (from SBE[3:0]#) and ISA master cycles from SA[1:0] and SBHE#). They are inputs during Host master cycles and are connected to Host CPU BE[3:0]#.
SBE[3:0]# SBE[3:0]A#	B T	84,98, 90,102 85,99, 91,101	***System Byte Enables.*** The EBC drives these signals during Host master cycles (based on HBE[3:0]# and HKEN#), during ISA master cycles (from SA[1:0] and SBHE#) and from an internal counter during assembly/disassembly cycles. Connected to BE[3:0]# of the EISA connectors.
SA[1:0]	B	40,42	***System Address 0 and 1.*** The EBC drives these lines for Host master cycles (based on HBE[3:0]# and HKEN#), for EISA/DMA/Refresh master cycles (based on SBE[3:0]# and from an internal counter for assembly/disassembly cycles). They are connected to SA[1:0] of the EISA connectors through a 74F245 transceiver (or EBB).
SBHE#	B	48	***System Byte High Enable.*** The EBC drives this line for Host master cycles (based on HBE[3:0]# and KEN#), for EISA/DMA/Refresh master cycles (based on SBE[3:0]# and from an internal counter during assembly/disassembly instructions). Connected to SBHE# of the EISA connectors through a 74F245 transceiver (or EBB).
HA20	B	105	***Host Address 20.*** The Host master drives this signal into the EBC except during EISA/ISA master cycles when it is based on LA20. HA20 is connected to Host CPU A20.
A20M#	I	124	***Address A20 Mask.*** For 386 systems, this is an input from the MCC's A20M# pin and is used to mask Host address A20. For 486 systems, the CPU takes care of the masking (it receives A20M# directly from the MCC) so this pin must be tied high.
LA20 LA20A	B T	34 33	***LA Bus Address A20.*** The EBC drives this line for Host master and DMA cycles (from HA20 & A20M#). It is an input for EISA/ISA master cycles. Connected to LA20 of the EISA connectors.

3.2.10 Register Access

Pin Name	Type	Pin No.	Description
NPCS#	I	138	***Numeric Coprocessor Chip Select.*** Chip select decode for numeric coprocessor access. Active when SA[15:3] decodes to 111X0XXXb and AEN# is inactive. The EBC internally qualifies this during I/O cycles in its coprocessor/387RESET logic. Connected to NPCS# from the DSC.
EBCCS#	I	140	***EBC Chip Select.*** Active for EBC internal register access. This signal goes active when SA[15:2] decodes to C10:C13h and AEN# is inactive. It is connected EBCCS# from the DBC.
XD[3:0]	B	60,59, 58,56	***XD Bus Low Nibble.*** These four bits provide data to/from the EBC during its internal register access. They are connected to XD[3:0] of the ISP.

3.2.11 Ground and VCC

Pin Name	Type	Pin Number	Description
VDD	I	20,37,57,77	+5V
VSS	I	6,13,26,32,44,50,63,70,86,93,107, 109,123,230,143,150	VSS or Ground
NC	I	1	Reserved (tie high)

3.3 EBC Register Description

First Aid Register
Index: C10h

BIT	FUNCTION	DEFAULT
0-3	Reserved (should be 0)	0000

EBC Control Register
Index: C11h

BIT	FUNCTION	DEFAULT
3	Reserved	X
2	Asynchronous START#. If enabled, the leading edge of START# occurs with the CLKIN signal and BCLKOUT is stretched to provide the required width of START# 1 = enable 0 = disable	0
1	HIDREF (hidden refresh). Enables hidden refreshes to the EISA bus. It should be enabled in conjunction with the host memory HIDREF bit in the MCC (Reg C30<1>). 1 = enable hidden refresh to EISA bus 0 = disable hidden refresh to EISA bus	0
0	Reserved	X

I/O Delay Control Register
Index: C12h

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>DEFAULT</th></tr>
<tr><td>3-0</td><td>Back-to-back I/O cycle delay. This register specifies the number of BCLKs from the end of CMD# to the beginning of START# for 8 and 16 bit I/O slaves.
<table>
<tr><th>Bit 3210</th><th># of BCLK 8-bit slave</th><th># of BCLK 16-bit slave</th><th></th></tr>
<tr><td>0000</td><td>N/A</td><td>N/A</td><td></td></tr>
<tr><td>0001</td><td>1</td><td>1</td><td></td></tr>
<tr><td>0010</td><td>2</td><td>2</td><td>(default BIOS initialization)</td></tr>
<tr><td>0011</td><td>3</td><td>3</td><td></td></tr>
<tr><td>0100</td><td>4</td><td>4</td><td></td></tr>
<tr><td>0101</td><td>5</td><td>4</td><td></td></tr>
<tr><td>0110</td><td>6</td><td>4</td><td></td></tr>
<tr><td>0111</td><td>7</td><td>4</td><td></td></tr>
<tr><td>1000</td><td>8</td><td>4</td><td></td></tr>
<tr><td>1001</td><td>9</td><td>4</td><td></td></tr>
<tr><td>1010</td><td>10</td><td>4</td><td></td></tr>
<tr><td>1011</td><td>11</td><td>4</td><td></td></tr>
<tr><td>1100</td><td>12</td><td>4</td><td></td></tr>
<tr><td>1101</td><td>13</td><td>4</td><td></td></tr>
<tr><td>1110</td><td>14</td><td>4</td><td></td></tr>
<tr><td>1111</td><td>15</td><td>4</td><td></td></tr>
</table></td><td>1111</td></tr>
</table>

EBC Revision-Number Register
Index: C13h

BIT	FUNCTION	DEFAULT
3-2	Reflects the configuration of the speed strapping option pins SPEED[1:0]# (read only) 11 = 20, 25 MHz 10 = 33 MHz 01 = 40 MHz 00 = 50 MHz	N/A
1-0	EBC revision number (read only)	00

3.4 AC/DC SPECIFICATIONS

3.4.1 82C681 (EBC) Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	70	C
Tstg	Storage Temperature	-40	125	C

Note: Permanent device damage may occur if Absolute maximum Ratings are exceeded.

3.4.2 82C681 (EBC) DC Characteristics

Temperature: 0C to 70C, Vcc: 5V +/- 5%

Sym	Description	Min	Max	Units
VIL	Input Low Voltage		0.8	V
VIH	Input High Voltage		2.0	V
VOL	Output Low Voltage (IOL = 4.0 mA)		0.4	V
VOH	Output High Voltage (IOH = -1.6mA)	2.4		V
IIL	Input Leakage Current, VIN = Vcc		10	uA
IOZ	Tristate Leakage Current		10	uA
CIN	Input Capacitance		20	pF
COUT	Output Capacitance		20	pF
ICC	Power Supply Current			mA

3.4.3 82C681(EBC) A.C. Specification Tables

Sym	Description	Min	Typ	Max
t1	HADS# setup time from CLKIN^			
t2	HADS# hold time from CLKIN^			
t3	HD/C#, HW/R#, HMI/O# setup time from CLKIN^			
t4	HD/C#, HW/R#, HMI/O# hold time from CLKIN^			
t5	HHOLD active delay from CLKIN^			
t6	HHLDA setup time from CLKIN^			
t7	HHLDA hold time from CLKIN^			
t8	WCS# setup time from CLKIN^			
t9	WCS# hold time from CLKIN^			
t10	HLOCM#, HLOCDEV# setup time from CLKIN^			
t11	HLOCM#, HLOCDEV# hold time from CLKIN^			
t12	NPRDY# setup time from CLKIN^			
t13	NPRDY# hold time from CLKIN^			
t14	HRDYO# active delay from CLKIN^			
t15	HRDYO# inactive delay from CLKIN^			
t16	DLRDY setup time from CLKIN^			
t17	DLRDY hold time from CLKIN^			
t18	HLOCK# setup time for host cycle from CLKIN^			
t19	HLOCK# hold time for host cycle from CLKIN^			
t20	BREQ setup time from CLKIN^			
t21	BREQ hold time from CLKIN^			
t22	HKEN# setup time from CLKIN^			
t23	HKEN# hold time from CLKIN^			
t24	NPERR# setup time from CLKIN^			
t25	NPERR# hold time from CLKIN^			
t26	EADS# active delay from CLKIN^			
t27	EADS# inactive delay from CLKIN^			
t28	DHOLD setup time to CLKIN^			
t29	DHOLD hold time from CLKIN^			
t30	REFRQ setup time to CLKIN^			
t31	DHOLD hold time from CLKIN^			
t32	SLOWH# setup time to CLKIN^			
t33	SLOWH# hold time from CLKIN^			
t34	MCCRDY setup time to CLKIN^			
t35	MCCRDY hold time from CLKIN^			
t36	RDHLDA active delay			
t37	CPUMISS# active delay			
t38	ST[3..0] setup time to CLKIN^			
t39	ST[3:0] hold time from CLKIN^			
t40	ST[3:0] active delay			

3.4.3 82C681(EBC) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t41	ST[3:0] inactive delay			
t42	DRDY setup time			
t43	DRDY hold time			
t44	DRDY active delay			
t45	EXMASTER# active delay from BCLKIN^			
t46	EMSTR16# active delay from BCLKIN^			
t47	BALE active delay from BCLKIN^ during START#			
t48	BALE active delay from BCLKIN or STARTt#			
t49	CHRDY, CHRDYA active delay for ISA master cycle			
t50	CHRDY, CHRDYA float delay from BCLKIN^			
t51	CHRDY, CHRDYA negated setup time from BCLKIN^			
t52	CHRDY, CHRDYA asserted setup time from BCLKIN			
t53	GT16M# setup time from BCLKIN^			
t54	GT16M# hold time from BCLKIN^			
t55	M16#, M16A# setup time from BCLKIN^ for EISA master, DMA & host cycle			
t56	M16#, M16A# hold time from BCLKIN^ for EISA master, DMA & host cycle			
t57	IO16#/TSEL setup time from BCLKIN			
t58	IO16#/TSEL hold time from BCLKIN			
t59	NOWS# setup time from BCLKIN			
t60	NOWS# hold time from BCLKIN			
t61	MRDC#, MWTC# active delay from BCLKIN^ for 16 bit case			
t62	MRDC#, MWTC# active delay from BCLKIN for 8 bit case			
t63	IORC#, IOWC# active delay from BCLKIN^			
t64	SMEMR#, SMEMW# propagation delay from MRDC#, MWTC#			
t65	SMEMR#, SMEMW# propagation delay from GT1M#			
t66	SMEMR#, SMEMW# propagation dealy from REFRESH#			
t67	REFRESH# setup time from BCLKIN^			
t68	REFRESH# hold time from BCLKIN^			
t69	MASTER16# setup time from BCLKIN^ fror EISA master			
t70	MASTER16# hold time from BCLKIN^ for EISA master			
t71	SM/IO#, SM/IOA# active delay from BCLKIN^			
t72	SW/R#, SW/RA# propagation delay from IOWC#, MWTC#			
t73	SW/R#, SW/RA# propagation delay from GT1M#			
t74	SW/R#, SW/RA# propagation delay from REFRESH#			
t75	SLOCK#, SLOCKA# active delay fromBCLKIN^ at START# active			
t76	START#, STARTA# active delay from BCLKIN^			
t77	START#, STARTA# active delay from CLKIN^			
t78	START#, STARTA# pulse width			
t79	START#, STARTA# setup time from BCLKIN^			

3.4.3 82C681(EBC) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t80	START#, STARTA# hold time from BCLKIN^ at START# active			
t81	CMD# active delay from BCLKIN^			
t82	EXRDY, EXRDYA active delay for burst DMA cycle from BCLKIN^			
t83	EXRDY, EXRDYA inactive delay for burst DMA cycle from BCLKIN			
t84	EXRDY, EXRDYA setup time from BCLKIN			
t85	EXRDY, EXRDYA hold time from BCLKIN			
t86	MSBURST#, MSBRSTA# active delay for DMA cycle from BCLKIN			
t87	MSBURST#, MSBRSTA# setup time for EISA master from BCLKIN			
t88	MSBURST#, MSBRSTA# hold time for EISA master from BCLKIN			
t89	SLBURST#, SLBRSTA# setup time for DMA & EISA master from BCLKIN			
t90	SLBURST#, SLBRSTA# hold time for DMA & EISA master from BCLKIN			
t91	EX32#, EX32A#, EX16#, EX16A# active delay for EISA-master-assembly cycle from BCLKIN			
t92	CLKIN period			
t93	CLKIN high, low time			
t94	CLKIN rise, fall time			
t95	BCLKOUT active/inactive delay delay from BCLKIN			
t96	BCLKOUT high, low time			
t97	BCLKOUT rise, fall time			
t98	CLKKB, CLKKB# period			
t99	CLKKB, CLKKB# high, low time			
t100	CLKKB, CLKKB# rise, fall time			
t101	PWRGD setup time from CLK^			
t102	RST# active delay from CLK^			
t103	RSTCPU active delay from CLK^			
t104	MDLE[2..0]# active delay			
t105	MDHDOE1# active delay			
t106	LDMDOE# active delay			
t107	MDSDOE[2..0]# active delay			
t108	SDOE[2..0]# active delay from BCLKIN^			
t109	CPYUP, CPY01#, CPY02#, CPY03#, CPY13# active delay from BCLKIN			
t110	ISAMSTR#, ISAMSTR active delay			

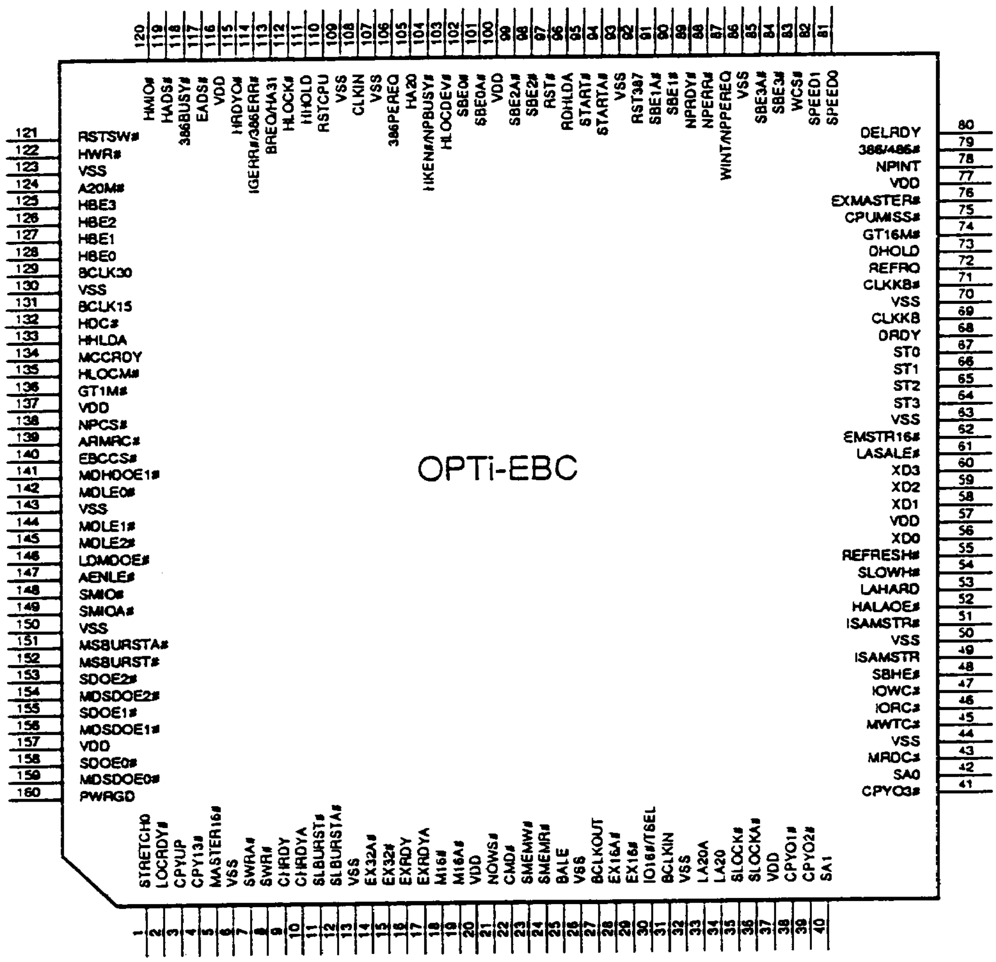
3.4.3 82C681(EBC) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t111	ISAMSTR#, ISAMSTR inactive delay			
t112	HALAOE# active delay			
t113	LAHARD active delay			
t114	LASALE# active delay			
t115	AENLE# active delay from BCLKIN			
t116	HBE[3..0] propagation delay from SBE			
t117	HBE[3..0] setup time from CLKIN^			
t118	HBE[3..0] hold time from CLKIN^			
t119	SBE[3..0] propagation delay from HBE			
t120	SBE[3..0] setup time from BCLKIN^			
t121	SBE[3..0] hold time from BCLKIN^			

Note:

T1^	Rising edge of T1
T1	Falling edge of T1
T2^	Rising edge of T2
T2	Falling edge of T2
BCLK^	Rising edge of BCLK
BCLK	Falling edge of BCLK
CLK^	Rising edge of CLK
CLK	Falling edge of CLK

3.5 82C681, EBC PINOUT

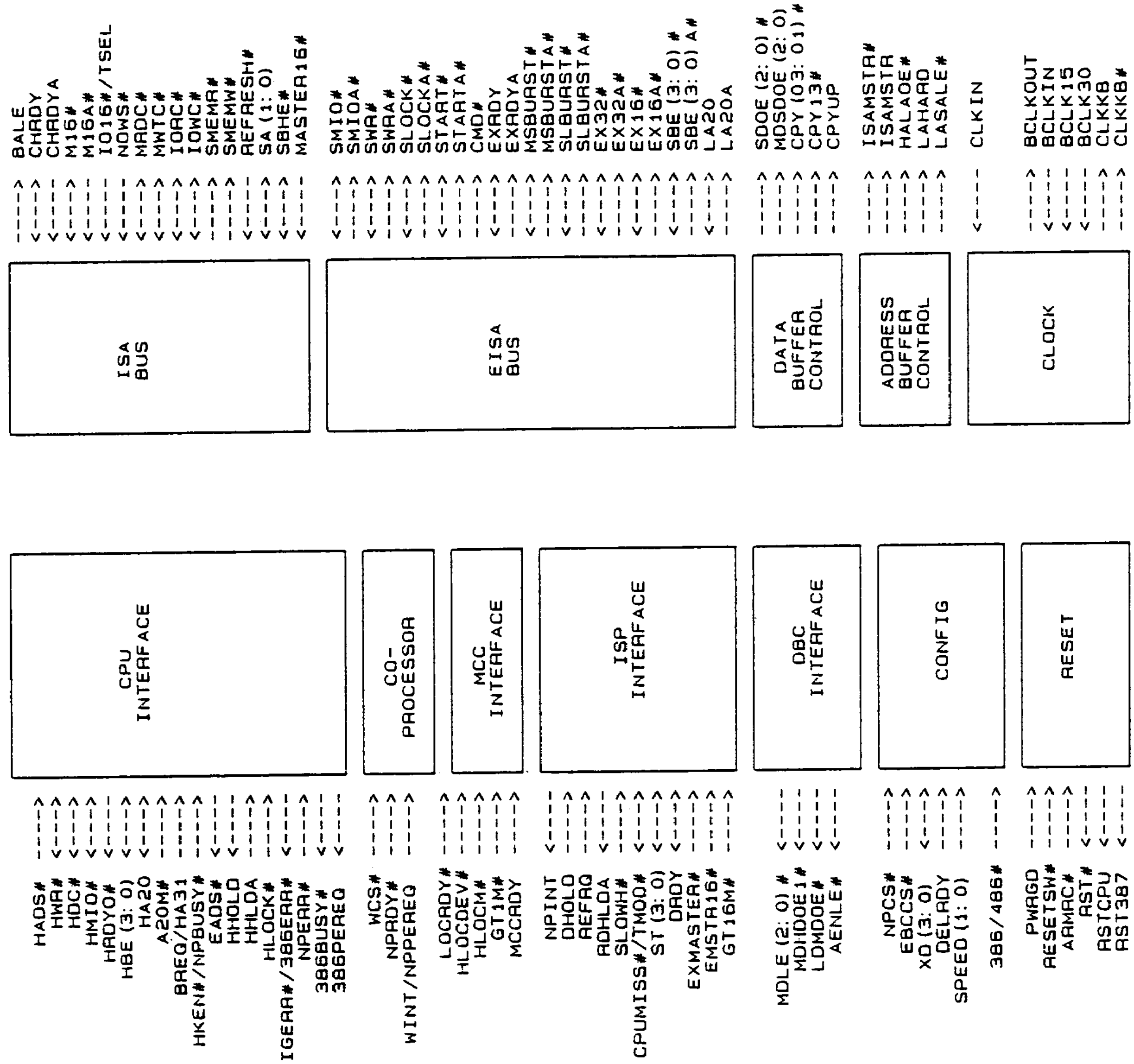


3.5.1 82C681, EBC Numeric Cross Reference

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	41	CPY03#	81	SPEED0	121	RSTSW#
2	LOCRDY#	42	SA0	82	SPEED1	122	HW/R#
3	CPYUP	43	MRDC#	83	WCS#	123	Vss
4	CPY13#	44	VSS	84	SBE3#	124	A20M#
5	MASTER16#	45	MWTC#	85	SBE3A#	125	HBE3
6	Vss	46	IORC#	86	Vss	126	HBE2
7	SWRA#	47	IOWC#	87	WINT/NPPEREQ	127	HBE1
8	SWR	48	SBHE#	88	NPERR#	128	HBE0
9	CHRDY	49	ISAMSTR	89	NPRDY#	129	BCLK30
10	CHRDYA	50	Vss	90	SBE1#	130	Vss
11	SLBURST#	51	ISAMSTR#	91	SBE1A#	131	BCLK15
12	SLBURSTA#	52	HALAOE#	92	RST387	132	HDC#
13	Vss	53	LAHARD	93	Vss	133	HHLDA
14	EX32A#	54	SLOWH#	94	STARTA#	134	MCCRDY
15	EX32#	55	REFRESH#	95	START	135	HLOCM#
16	EXRDY	56	XD0	96	RDHLDA	136	GT1M#
17	EXRDYA	57	VDD	97	RST#	137	VDD
18	M16#	58	XD1	98	SBE2#	138	NPCS#
19	M16A#	59	XD2	99	SBE2A#	139	ARMRC#
20	VDD	60	XD3	100	VDD	140	EBCCS#
21	NOWS#	61	LASALE#	101	SBE0A#	141	MDHDOE1#
22	CMD#	62	EMSTR16#	102	SBE0#	142	MDLE0#
23	SMEMW#	63	Vss	103	HLOCDEV#	143	Vss
24	SMEMR#	64	ST3	104	HKEN#/NPBUSY#	144	MDLE1#
25	BALE	65	ST2	105	HA20	145	MDLE2#
26	Vss	66	ST1	106	386PEREQ	146	LDMDOE#
27	BCLKOUT	67	ST0	107	Vss	147	AENLE#
28	EX16A#	68	DRDY	108	CLKIN	148	SM/IO#
29	EX16#	69	CLKKB	109	VSS	149	SM/IOA#
30	IO16#/TSEL	70	Vss	110	RSTCPU	150	Vss
31	BCLKIN	71	CLKKB#	111	HHOLD	151	MSBURSTA#
32	Vss	72	REFRQ	112	HLOCK#	152	MSBURST#
33	LA20A	73	DHOLD	113	BREQ/HA31	153	SDOE2#
34	LA20	74	GT16M#	114	IGERR#/386ERR#	154	MDSDOE2#
35	SLOCK#	75	CPUMISS#	115	HRDY0#	155	SDOE1#
36	SLOCKA#	76	EXMASTER#	116	VDD	156	MDSDOE1#
37	VDD	77	VDD	117	EADS#	157	VDD
38	CPY01#	78	NPINT	118	386BUSY#	158	SDOE0#
39	CPY02#	79	386/486#	119	HADS#	159	MDSDOE0#
40	SA1	80	DELRDY	120	HM/IO#	160	PWRGD

3.5.2 82C681, EBC Alphabetical Cross Reference

Name	Pin	Name	Pin	Name	Pin	Name	Pin
386/486#	79	HADS#	119	MSBURST#	152	SPEED0	81
386BUSY#	118	HALAOE#	52	MSBURSTA#	151	SPEED1	82
386PEREQ	106	HBE0	128	MWTC#	45	ST0	67
A20M#	124	HBE1	127	NC	1	ST1	66
AENLE#	147	HBE2	126	NOWS#	21	ST2	65
ARMRC#	139	HBE3	125	NPCS#	138	ST3	64
BALE	25	HDC#	132	NPERR#	88	START	95
BCLK15	131	HHLDA	133	NPINT	78	STARTA#	94
BCLK30	129	HHOLD	111	NPRDY#	89	SWR	8
BCLKIN	31	HKEN#/NPBUSY#	104	PWRGD	160	SWRA#	7
BCLKOUT	27	HLOCDEV#	103	RDHLDA	96	VDD	20
BREQ/HA31	113	HLOCK#	112	REFRESH#	55	VDD	37
CHRDY	9	HLOCM#	135	REFRQ	72	VDD	57
CHRDYA	10	HM/IO#	120	RST#	97	VDD	77
CLKIN	108	HRDY0#	115	RST387	92	VDD	100
CLKKB	69	HW/R#	122	RSTCPU	110	VDD	116
CLKKB#	71	IGERR#/386ERR#	114	RSTSW#	121	VDD	137
CMD#	22	IO16#/TSEL	30	SA0	42	VDD	157
CPUMISS#	75	IORC#	46	SA1	40	VSS	44
CPY01#	38	IOWC#	47	SBE0#	102	VSS	109
CPY02#	39	ISAMSTR	49	SBE0A#	101	Vss	6
CPY03#	41	ISAMSTR#	51	SBE1#	90	Vss	13
CPY13#	4	LA20	34	SBE1A#	91	Vss	26
CPYUP	3	LA20A	33	SBE2#	98	Vss	32
DELRDY	80	LAHARD	53	SBE2A#	99	Vss	50
DHOLD	73	LASALE#	61	SBE3#	84	Vss	63
DRDY	68	LDMDOE#	146	SBE3A#	85	Vss	70
EADS#	117	LOCRDY#	2	SBHE#	48	Vss	86
EBCCS#	140	M16#	18	SDOE0#	158	Vss	93
EMSTR16#	62	M16A#	19	SDOE1#	155	Vss	107
EX16#	29	MASTER16#	5	SDOE2#	153	Vss	123
EX16A#	28	MCCRDY	134	SLBURST#	11	Vss	130
EX32#	15	MDHDOE1#	141	SLBURSTA#	12	Vss	143
EX32A#	14	MDLE0#	142	SLOCK#	35	Vss	150
EXMASTER#	76	MDLE1#	144	SLOCKA#	36	WCS#	83
EXRDY	16	MDLE2#	145	SLOWH#	54	WINT/NPPEREQ	87
EXRDYA	17	MDSDOE0#	159	SM/IO#	148	XD0	56
GT16M#	74	MDSDOE1#	156	SM/IOA#	149	XD1	58
GT1M#	136	MDSDOE2#	154	SMEMR#	24	XD2	59
HA20	105	MRDC#	43	SMEMW#	23	XD3	60



EBC BLOCK DIAGRAM

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4. 82C686, OPTi INTEGRATED SYSTEM PERIPHERAL (ISP)

4.1 FEATURES

The ISP is a 160-pin PFP (Plastic Flat Package) device. It integrates two 8254 timers, EISA NMI/Time-out logic, two modified 8259 Interrupt controllers, the EISA DMA/Refresh controller, and the EISA system arbiter.

It includes the following features:

* 160-pin Plastic Flat Package
* Two Programmable Interval Timers (equivalent to two 8254Timer/Counters)
* NMI/Timeout logic
* Two 8259 Interrupt controllers
* Enhanced DMA/Refresh Functions
* EISA system arbiter
* Integrated XD /SD buffers reduce external logic
* Built-in Tristate test mode enhances manufacturability

4.1.1 Timer/Counter

The ISP provides two programmable interval timers (equivalent to two 8254s) which appear as five counter/timers. These timers are programmed the same as discrete 8254s and are accessed by software through I/O instructions. Timer-1 occupies I/O space 40-43h and Timer-2 occupies the I/O range 48-4Bh. Timer-1 contains three counters and Timer-2 contains two counters. The middle counter of Timer-2 is reserved in EISA systems and is not accessible.

Timer-1, counter-0 is used for the system timer interrupt (IRQ0). Timer-1, counter-1 generates DRAM refresh requests (REFRQ). Timer-1, counter-2 generates the speaker output (SPKR).

Timer-2, counter-0 provides a fail-safe timer. Timer-2, counter-1 is not implemented by EISA systems. Timer-2, counter-2 is available for any additional timing function needed.

4.1.2 NMI/Timeout logic

The ISP integrates the NMI/Timeout ports defined by the Standard EISA specification. Programming and feature details are beyond the scope of this text. Please refer to EISA Specification 3.11 or later for further information and detailed descriptions of this logic (pp231-232, 281-285).

The logic includes the following:

NMI:
8-bit NMI Status and Control Port at 061h
1-bit NMI Enable/Disable at Port 070<7>
8-bit Extended NMI Status Control port at 461h

Write only Software NMI Generation Port at 462h

Timeout Logic:
6-bit timeout counter triggered by EISA master bus preemption request
8-bit timeout counter triggered by CMD#

4.1.3 Interrupt Controller

The ISP integrates logic built around two 8259 equivalent interrupt controllers. These interrupt controllers are enhanced to comply with the EISA standard. Independent edge/level triggering for each bus IRQ has been added as well as the muxing of the NPINT signal with the chaining interrupt (IRQ2). Programming and feature details are beyond the scope of this text. Please refer to EISA Specification Revision 3.10 or later for further information and detailed descriptions of this logic (pp230-233, 265-280).

The logic includes the following:

Two registers control the edge/level triggering of each IRQ.
Two enhanced 8259 equivalent interrupt controllers occupying I/O address 20-21h, A0-A1h & 4D0-4D1h as defined in the EISA system board specification.

4.14 DMA/Refresh Controller

The DMA/Refresh logic is a superset of the AT DMA and Refresh controller (except the bus-control-strobe generation which is delegated to the EBC). It includes a register set occupying I/O address space 0-1Fh, 80-8Fh, C0-DFh, 400-40Bh, 481-48Fh, 4C2-4CEh, 4D4-4D6h, 4E0-4EEh and 4F4-4FEh. It also includes a 4+3 channel priority arbitration logic. This block also generates the internal address and chip-selects for all ISP blocks. The decode logic also generates GT16M# for the EBC. For a complete description of I/O decode and DMA functions refer to the EISA specification Revision 3.10 or later (pp230-264).

4.1.5 System Arbiter

The arbiter in the ISP uses the multilevel rotating priority arbitration method described in the EISA Bus specification. At the highest level, the ISP arbitrates sequentially between a DMA channel, the Refresh Controller and the Host/EISA/ISA bus master. Each gains access to the EISA/ISA bus at least once every three arbitration cycles if all of them are simultaneously requesting the bus. Devices not requesting the bus are skipped in the rotation.

Within these three main groups, additional arbitration occurs. For instance, the ISP arbitrates back and forth between the host CPU and any additional bus master. The bus masters are arranged in a rotating priority so that a new bus master is serviced after each CPU access. Similarly, DMA priorities can be modified by programming the DMA controller command registers to rotating priority.

NMI's have a special priority that cause the bus masters and DMA controller to be bypassed each time they come up for rotation. This gives the CPU complete control of the bus to perform the NMI service.

This block consists of three rotating priority arbiters:

a) 3-way arbiter between Refresh, DMA and Host/EISA-Master,
b) 2-way arbiter between Host- and EISA-Masters
c) 6-way arbiter between EISA-Masters

It also includes two read-only registers at I/O address 40Ch and 464h that indicate CPU/EISA Master and the Last EISA Master Granted. For a description of the arbiter, refer to EISA specification Revision 3.10 or later(pp135-147, pp230-264 and pp285-286.)

4.1.6 Data Buffer

The ISP eliminates the external logic required to create the local peripheral bus (XD-bus) by providing internal buffering between SD[7:0] and XD[7:0]. Also, data read from internal ISP registers is presented directly on the SD bus.

4.1.7 Testability

I/O configuration register C20h <7:5> contains a 3-bit read only value that indicates the revision level of the ISP. This allows the revision level of the ISP to be verified by software.

The ISP includes a tristate test mode to enhance board level testability/manufacturability. When this test mode is entered, all outputs and bidirectional pins become tristated, allowing electrical isolation between the ISP and signals on the PCB.

At the trailing edge of the motherboard reset (RST#), the ISP samples two pins to determine whether the tristate test mode should be entered. GT16M#/TMOD# must be low and IRQ8#/TSEL must be high at this sample point to guarantee entering this test state. The following table illustrates this:

GT16M#/ TMOD#	IRQ8#/ TSEL	Function
Low	Low	Reserved
Low	High	Tristate Test Mode
High	X	Normal Operation

4.2 ISP Pin Description

4.2.1 Bus Interface

Pin Name	Type	Pin No.	Description
HA[31:16]	O	71-78, 82-89	***Host Address Bus.*** Driven during DMA with memory address. Connected to Host CPU A[31:16].
IA[15:8]	B	149-142	***Intermediate Address Bus.*** Driven during DMA/Refresh with memory address. Connected to LA[15:8] of the EISA connectors thru a transceiver (or EBB).
LA[7:2]	B	138,137, 135,134, 132,131	***EISA Latched Address Bus.*** Driven during DMA/Refresh with memory address. Connected to LA[7:2] of the EISA connectors.
LASALE#	I	136	***LA Bus to SA Bus Latch Enable.*** Latch enable control for LA-SA buffer. Connected to LASALE# from the EBC.
IALAOE	O	133	***IA Bus to LA Bus Output Enable.*** Direction control for IA-LA transceiver. It is connected to an external transceiver (or EBB).
SBE[3:0]#	B	127,126, 124,123	***System Byte Enables.*** These are sampled/used in the same way as IA[15:8]. Connected to SBE[3:0]# of the EISA connectors.
HW/R#	O	69	***Host Write / Read.*** Driven during DMA indicating data direction to memory. Connected to Host CPU W/R#.
START#	I	94	***START.*** Used to Start an EISA cycle. Connected to START# of the EISA connectors.
IORC#	I	156	***I/O Read Command.*** Used to read ISP internal registers onto the SD bus. Connected to IORC# of the EISA connectors.
IOWC#	I	158	***I/O Write Command.*** Used to write to the ISP internal registers. Connected to IOWC# of the EISA connectors.
SD[7:0]	B	17,16,14, 13,157, 155,153, 151	***System Data Bus.*** Data lines used for programming the ISP and for buffering XD[7:0]. Connected to XD[7:0] of DBC.
XD[7:0]	B	2-9	***Peripheral Data Bus.*** Data lines that connect to SD[7:0] thru the integrated transceiver. These lines are driven when XDEN# is active and XDRD# inactive. Connected to XD[7:0]
XDEN#	I	152	***XD Bus Enable.*** Enables the XD output buffer. Connected to XDEN# from the DSC
XDRD#	I	154	***XD Bus Read.*** Controls the direction of data on the XD bus. Connected to XDRD# from the DSC.

ST[3:0]	B	98..95	Inter-Chip Status Bus. Connected to ST[3:0] of the EBC. During DMA/Refresh, the ISP drives these lines. a) ST[3:2] encodes the DMA requester width as follows: ST[3:2] REQUESTER WIDTH 00 8-bit 01 16-bit 10 32-bit 11 Idle b) ST[1:0] encodes the DMA cycle timing as follows: ST[1:0] CYCLE TIMING 00 Compatible 01 Type-A 10 Type-B 11 Burst (only for 16/32bit)
DRDY	B	93	***DMA Ready***. The EBC drives this line during DMA or Refresh. Connected to DRDY of the EBC.
BCLK	I	102	***EISA Bus Clock***. Connected to BCLK of the EISA connectors.

4.2.2 Timer

Pin Name	Type	Pin No.	Description
OSC	I	22	***Timer Oscillator***. This is the main clock used by the internal 8254 timers. Connected to 14.31818 MHz oscillator.
SPKR	O	18	***Speaker Tone***. Used to drive the system-board speaker. This signal is derived from the Timer-0 Counter-2 and a Port-B bit.
SLOWH#	O	23	***Slowdown Hold Request***. Used to make the CPU appear to "slow down" when necessary for compatibility reasons. Driven from the output of Timer-1 Counter-2.

4.2.3 NMI/Timeout logic

Pin Name	Type	Pin No.	Description
PARITY#	I	27	***Parity Error Strobe***. The falling edge of this signal indicates a host DRAM parity failure. Connected to PARITY# from the DSC.
IOCHK#	I	28	***I/O Channel Check***. An EISA/ISA device signals a fatal error by driving this line low. Connected to IOCHK# of the EISA connectors.
NMI	O	26	***Non-Maskable-Interrupt***. NMI is generated in response to PARITY#, IOCHK#, slave timeout, fail-safe timer timeout, EISA master timeout or I/O writes to port 462h. Connected to the host CPU's NMI pin.
RST#	I	31	***Motherboard Reset***. It is driven active when PWRGD or RESETSW# is low. Connected to RST# from the EBC.
CMD#	I	24	***EISA Bus Command***. This is used to generate a slave timeout. It is connected to CMD# of the EISA connectors.
RSTDRV	O	29	***Reset Drive***. This is driven active during RST# or due to a software-reset or slave/EISA-master timeout. Connected to RSTDRV of the EISA connectors.

4.2.4 Interrupt

Pin Name	Type	Pin No.	Description
IRQ[15:9]	I	49-44,39	***Interrupt Request Bus.*** Connected to IRQ[15:14] of the EISA connectors, NPINT from the EBC and IRQ[12:9] of the EISA connectors.
IRQ8#/TSEL	I	38	***Interrupt Request 8 or Test Mode Select.*** This pin normally functions as the IRQ8 input and is connected to IRQ# from the RTC. The second function of IRQ8#/TSEL is to force the ISP into test mode. The ISP will enter its tristate test mode when this pin is sampled high on the trailing edge of RST# AND GT16M#/TMOD# is sampled low.
IRQ[7:3],1	I	37-32	***Interrupt Request Bus.*** Connected to IRQ[7:3] of EISA connectors and IRQ1 from the Keyboard Controller.
INT	I	43	***Interrupt.*** Connected to Host-CPU INT.

4.2.5 DMA/Refresh

Pin Name	Type	Pin No.	Description
DRQ[7:5] DRQ[3:0]	I	105-109, 111,112	***DMA Request Bus.*** Connected to DRQ[7:5],[3:0] of the EISA connectors.
DACK[7:5] DACK[3:0]	O	113-119	***DMA Acknowledge Bus.*** Connected to DACK[7:5],[3:0] of the EISA connectors.
REFRESH#	B	11	***Refresh.*** Refresh is driven low for non ISA master refresh cycles to the EISA bus. It is used as an asynchronous input for ISA master generated refresh and for ST[3:0] and DRDY direction control. Connected to REFRESH# of the EISA connectors.
EOP	B	129	***End-of-Process.*** As an output, it indicates that the DMA channel's word count has reached terminal count. As an input, it indicates that a DMA slave wishes to stop the a DMA transfer. Connected to TC of the EISA connectors.
AEN#	O	128	***Address Enable.*** Indicates that an address is being driven by the DMA controller and is used for the I/O decode and slot-specific generation of AENx. Connected to the corresponding pin of the DBC.

4.2.6 I/O Decodes

Pin Name	Type	Pin No,	Description
RTCAS	O	25	***Real Time Clock AS.*** Active for 2 BCLK's from the leading edge of CMD# if address 111 X XX0b is decoded from LA[15:2], SBE[3:0]# and AEN#. It remains active from RST# until the first CMD#. Connected to AS of the RTC.
GT16M#/ TMOD#	B	68	***Greater Than 16M or Test Mode.*** This pin has two functions. Normally, it is driven active during DMA cycles when an address greater than 16M is presented on HA[31:24]. The second function of this pin is to allow the ISP to enter its test mode. If sampled low at the trailing edge of reset (RST#), along with IRQ8#/TSEL being high, then the ISP enters its Tristate test mode. This signal is tristated during RST# and a weak internal pull-up keeps it high when no outside tester or source is driving it.

4.2.7 System Arbiter

Pin Name	Type	Pin No.	Description
MREQ[6:1]#	I	58, 62-66	***Slot Specific EISA Master Bus Request.*** Each slot provides an EISA bus master to have its own bus request line. Connected to slot-specific MREQx# of the EISA connectors.
MACK[6:1]#	O	52-57	***Slot Specific EISA Master Bus Request Acknowledge.*** Connected to slot-specific MACKx# of the EISA connectors.
CPUMISS#	I	67	***CPU Miss.*** This signal tells the arbiter that the host CPU is waiting for the bus. This signal is asynchronous with BCLK. Connected to CPUMISS# from the EBC.
DHOLD	O	91	***DMA Hold.*** This is a request for the Host and EISA bus, generated when the arbiter wants to transfer control to an EISA/ISA/DMA master. Connected to DHOLD of the EBC.
REFRQ	O	92	***Refresh Request.*** . This is a request for the EISA bus, generated when the arbiter wants to transfer control to the Refresh controller. Connected to REFRQ of the EBC & MCC
RDHLDA	I	103	***Refresh/DMA Hold Acknowledge.*** This is the acknowledgement to DHOLD or REFRQ, indicating that the requested bus/busses is/are free. RDHLDA's leading edge is asynchronous and the trailing edge is caused combinatorially from DHOLD or REFRQ. Connected to RDHLDA from the EBC.
EXMASTER#	O	51	***EISA Master.*** This indicates that an EISA master is in control of the Host/EISA bus. Connected to EXMASTER# of the EBC.
EMSTR16#	O	104	***ISA Master.*** This indicates that an ISA master is in control of the Host/EISA bus. Connected to EMSTR16# of the EBC and the MCC.

4.2.8 Ground and VCC

Pin Name	Type	Pin Number	Description
VDD	I	1,20,40,60,81,100,120,140	+5V
VSS	I	10,19,21,30,41,42,50,59,61, 70,79,80,90,99,101,110, 121,122,130,139, 141,150,159,160	VSS or Ground

4.3 ISP Register Description

ISP Revision-Number Register
Index: C20h

BIT	FUNCTION	DEFAULT
7-5	The revision number of ISP chip (read only)	
4-0	DHOLD is delayed by the number of BCLK's determined by the content of the 5-bit register (R/W)	00000

Index: C21h, C22
Reserved for test purpose

Index: 40-48h, 4A-4Bh
Defined in EISA spec Rev-3.10, pp230 & 287-293

Index: 61h, 70h bit-7, 461h, 462h
Defined in EISA spec Rev-3.10 pp231-232 & pp281-285

Index: 20-21h, A0-A1h, 4D0-4D1h
Defined in EISA spec Rev-3.10 pp230-233 & pp265-280

**Index: 0-1Fh, 80-8Fh, C0-DFh, 400-40Bh,481-48Fh,4C2-4CEh,
4D4-4D6h, 4E0-4EEh, & 4F4-4FEh**
For a complete description of I/O decode and DMA functions refer to EISA spec Rev-3.10 pp230-264

Index: 464h
This read-only register indicate the Last EISA Master Granted. For a description of the arbiter refer to EISA spec Rev-3.10 pp135-147, pp230-264 and pp285-286.

4.4 AC/DC SPECIFICATIONS

4.4.1 82C686 (ISP) Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	70	C
Tstg	Storage Temperature	-40	125	C

Note: Permanent device damage may occur if Absolute maximum Ratings are exceeded.

4.4.2 82C686 (ISP) DC Characteristics

Temperature: 0C to 70C, Vcc: 5V +/- 5%

Sym	Description	Min	Max	Units
VIL	Input Low Voltage		0.8	V
VIH	Input High Voltage		2.0	V
VOL	Output Low Voltage (IOL = 4.0 mA)		0.4	V
VOH	Output High Voltage (IOH = -1.6mA)	2.4		V
IIL	Input Leakage Current, VIN = Vcc		10	uA
IOZ	Tristate Leakage Current		10	uA
CIN	Input Capacitance		20	pF
COUT	Output Capacitance		20	pF
ICC	Power Supply Current			mA

4.4.3 82C686(ISP) A.C. Specification Tables

Sym	Description	Min	Typ	Max
t1	HA[31..16] active delay (DMA with memory address)	10		35
t2	HA[31..16] inactive delay (DMA with memory address)	7		30
t3	IA[15..8] setup time to BALE	5		
t4	IA[15..8] hold time from BALE	10		
t5	LA[7..2] setup time to BALE	5		
t6	LA[7..2] hold time from BALE	10		
t7	LA[7..2] active delay (DMA/refresh)	7		30
t8	LA[7..2] inactive delay (DMA/refresh)	7		30
t9	LASALE# setup time to BALE			
t10	LASALE# hold time from BALE			
t11	SBE[3..0]# setup time to BALE	5		
t12	SBE[3..0]# hold time from BALE	10		
t13	SBE[3..0]# active delay (DMA/refresh)	5		25
t14	SBE[3..0]# inactive delay (DMA/refresh)	5		25
t15	HW/R# setup time to BCLK (DMA)	5		
t16	HW/R# hold time from BCLK (DMA)	10		
t17	START# setup time			
t18	START# hold time			
t19	IORC#, IOWC#			
t30	SD setup time to IOWC	0		
t31	SD hold time from IOWC	15		
t32	XD setup time to IOWC	0		
t33	XD hold time from IOWC	15		
t34	XDEN# active delay			
t35	XDEN# inactive delay			
t36	XDRD# activedelay			
t37	XDRD# inactive delay			
t38	ST[3..0] active delay	5		25
t39	ST[3..0] inactive delay	7		25
t40	ST[3..0] float	7		31
t41	DRDY setup time	10		
t42	DRDY hold time	15		
t43	OSC period	65		
t44	OSC high time	20		
t45	OSC low time	20		
t46	SPKR active delay from OSC rising edge	10		40
t47	SPKR inactive delay from OSC rising edge	8		30
t48	SLOWH# active delay	10		40
t49	SLOWH# inactive delay	8		30
t50	NMI active delay from BCLK rising edge	5		30

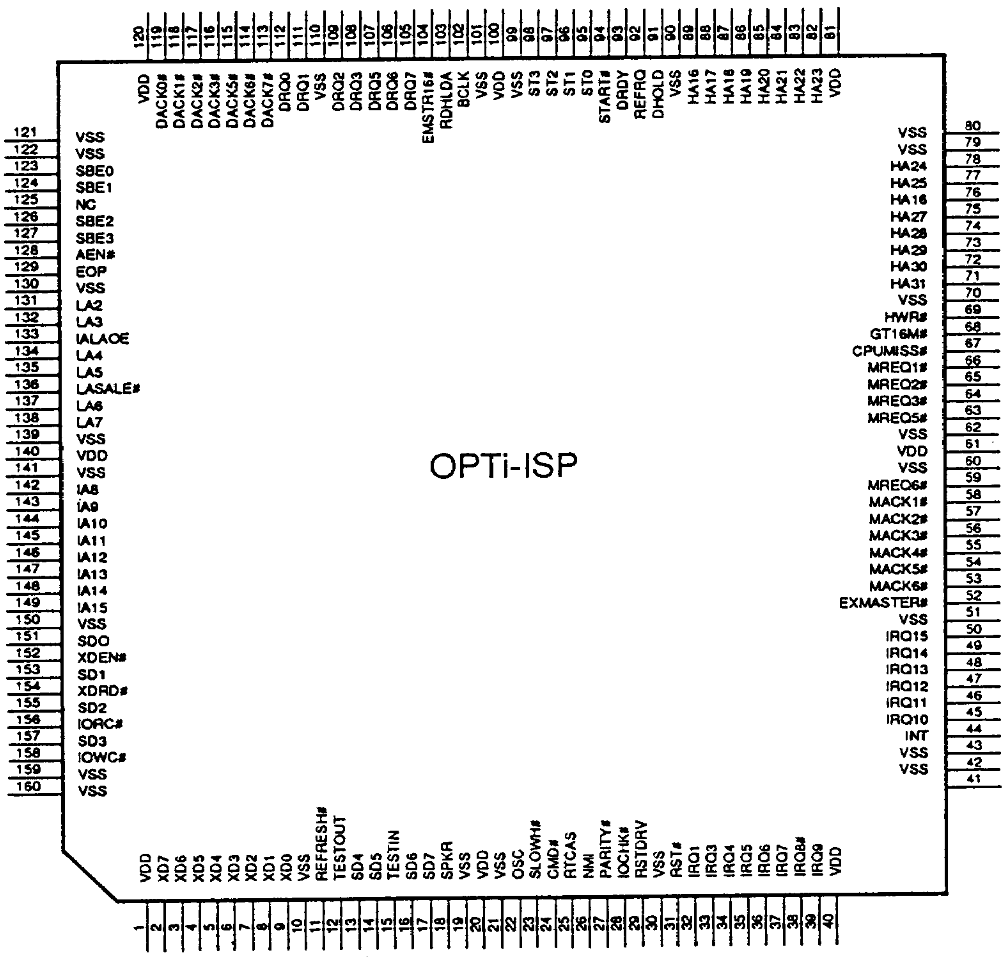
4.4.3 82C686(ISP) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t51	NMI inactive delay from BCLK rising edge	5		30
t52	NMI active delay from OSC rising edge			120
t53	RST# active pulse width	1000		
t54	CMD# setup time (sync. active/inactive)	10		
t55	CMD# hold time (sync. active/inactive)	10		
t56	RSTDRV delay active (bus timeout)	6		25
t57	RSTDRV delay active (port/RST)	3		13
t58	RSTDRV delay inactive	4		15
t59	INT active delay from IRQ active/inactive	5		35
t70	INT inactive delay from IRQ active/inactive	10		50
t71	INT active delay from OSC rising edge	10		40
t72	INT inactive delay from OSC rising edge	15		50
t73	DRQ setup time (sync. trailing edge)	10		
t74	DRQ hold time (sync. trailing edge)	15		
t75	DRQ setup time (async. leading/trailing edge)	10		
t76	DRQ hold time (async. leading/trailing edge)	15		
t77	DACK delay active/inactive (ISA masters) from BCLK^	6		30
t78	DACK delay active/inactive (DMA devices) from BCLK^	7		30
t79	DACK delay active/inactive (ISA masters) from BCLK	5		25
t80	DACK delay active/inactive (DMA devices) from BCLK	6		25
t81	REFRESH# delay active			
t82	REFRESH# float inactive			
t83	REFRESH# setup time	10		
t84	REFRESH# hold time	15		
t85	EOP delay active (non-burst)	5		20
t86	EOP active delay	5		20
t87	EOP inactive delay	7		25
t88	EOP float from DACK from DACK active			
t89	EOP setup time (sync. burst mode)	15		
t90	EOP hold time (sync. burst mode)	15		
t91	EOP setup time (async. non-burst)	15		
t92	EOP hold time (async. non-burst)	15		
t93	AEN# active delay from BCLK	10		35
t94	AEN# inactive delay from BCLK	7		25
t95	RTCAS delay active	5		30
t96	RTCAS delay inactive	5		30
t97	GT16#/TMOD# active delay	7		30
t98	GT16#/TMOD# inactive delay	8		35
t99	MREQ# setup time (BCLK rising)	10		

4.4.3 82C686(ISP) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t110	MREQ# setup time (BCLK falling)			
t111	MREQ# hold time	15		
t112	MACK# active delay	6		25
t113	MACK# inactive delay	4		20
t114	CPUMISS# setup time (asyn.)	10		
t115	CPUMISS# hold time (asyn.)	15		
t116	DHOLD active delay	5		25
t117	DHOLD inactive delay	7		30
t118	REFRQ active delay	5		25
t119	REFRQ inactive delay	7		30
t120	RDHLDA setup time	10		
t121	RDHLDA hold time	15		
t122	EXMASTER# active delay	7		30
t123	EXMASTER# inactive delay	5		25
t124	EMSTR16# active delay	7		30
t125	EMSTR16# inactive delay	6		25

4.5 82C686, ISP PIN-OUT



4.5.1 82C686, ISP Numeric Cross Reference

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	41	Vss	81	VDD	121	Vss
2	XD7	42	Vss	82	HA23	122	Vss
3	XD6	43	INT	83	HA22	123	SBE0
4	XD5	44	IRQ10	84	HA21	124	SBE1
5	XD4	45	IRQ11	85	HA20	125	NC
6	XD3	46	IRQ12	86	HA19	126	SBE2
7	XD2	47	IRQ13	87	HA18	127	SBE3
8	XD1	48	IRQ14	88	HA17	128	AEN#
9	XD0	49	IRQ15	89	HA16	129	EOP
10	Vss	50	Vss	90	Vss	130	Vss
11	REFRESH#	51	EXMASTER#	91	DHOLD	131	LA2
12	TESTOUT	52	MACK6#	92	REFRQ	132	LA3
13	SD4	53	MACK5#	93	DRDY	133	IALAOE
14	SD5	54	MACK4#	94	START#	134	LA4
15	TESTIN	55	MACK3#	95	ST0	135	LA5
16	SD6	56	MACK2#	96	ST1	136	LASALE#
17	SD7	57	MACK1#	97	ST2	137	LA6
18	SPKR	58	MREQ6#	98	ST3	138	LA7
19	Vss	59	Vss	99	Vss	139	Vss
20	VDD	60	VDD	100	VDD	140	VDD
21	Vss	61	Vss	101	Vss	141	Vss
22	OSC	62	MREQ5#	102	BCLK	142	IA8
23	SLOWH#	63	MREQ4#	103	RDHLDA	143	IA9
24	CMD#	64	MREQ3#	104	EMSTR16#	144	IA10
25	RTCAS	65	MREQ2#	105	DRQ7#	145	IA11
26	NMI	66	MREQ1#	106	DRQ6#	146	IA12
27	PARITY#	67	CPUMISS#	107	DRQ5#	147	IA13
28	IOCHK#	68	GT16M#	108	DRQ3#	148	IA14
29	RSTDRV	69	HW/R#	109	DRQ2#	149	IA15
30	Vss	70	Vss	110	Vss	150	Vss
31	RST#	71	HA31	111	DRQ1#	151	SD0
32	IRQ1	72	HA30	112	DRQ0#	152	XDEN#
33	IRQ3	73	HA29	113	DACK7#	153	SD1
34	IRQ4	74	HA28	114	DACK6#	154	XDRD#
35	IRQ5	75	HA27	115	DACK5#	155	SD2
36	IRQ6	76	HA26	116	DACK3#	156	IORC#
37	IRQ7	77	HA25	117	DACK2#	157	SD3
38	IRQ8#	78	HA24	118	DACK1#	158	IOWC#
39	IRQ9	79	Vss	119	DACK0#	159	Vss
40	VDD	80	Vss	120	VDD	160	Vss

4.5.2 82C686, ISP Alphabetical Cross Reference

Name	Pin	Name	Pin	Name	Pin	Name	Pin
AEN#	128	HW/R#	69	MACK6#	52	VDD	40
BCLK	102	IA10	144	MREQ1#	66	VDD	60
CMD#	24	IA11	145	MREQ2#	65	VDD	81
CPUMISS#	67	IA12	146	MREQ3#	64	VDD	100
DACK0#	119	IA13	147	MREQ4#	63	VDD	120
DACK1#	118	IA14	148	MREQ5#	62	VDD	140
DACK2#	117	IA15	149	MREQ6#	58	Vss	10
DACK3#	116	IA8	142	NC	125	Vss	19
DACK5#	115	IA9	143	NMI	26	Vss	21
DACK6#	114	IALAOE	133	OSC	22	Vss	30
DACK7#	113	INT	43	PARITY#	27	Vss	41
DHOLD	91	IOCHK#	28	RDHLDA	103	Vss	42
DRDY	93	IORC#	156	REFRESH#	11	Vss	50
DRQ0#	112	IOWC#	158	REFRQ	92	Vss	59
DRQ1#	111	IRQ1	32	RST#	31	Vss	61
DRQ2#	109	IRQ10	44	RSTDRV	29	Vss	70
DRQ3#	108	IRQ11	45	RTCAS	25	Vss	79
DRQ5#	107	IRQ12	46	SBE0	123	Vss	80
DRQ6#	106	IRQ13	47	SBE1	124	Vss	90
DRQ7#	105	IRQ14	48	SBE2	126	Vss	99
EMSTR16#	104	IRQ15	49	SBE3	127	Vss	101
EOP	129	IRQ3	33	SD0	151	Vss	110
EXMASTER#	51	IRQ4	34	SD1	153	Vss	121
GT16M#	68	IRQ5	35	SD2	155	Vss	122
HA16	89	IRQ6	36	SD3	157	Vss	130
HA17	88	IRQ7	37	SD4	13	Vss	139
HA18	87	IRQ8#	38	SD5	14	Vss	141
HA19	86	IRQ9	39	SD6	16	Vss	150
HA20	85	LA2	131	SD7	17	Vss	159
HA21	84	LA3	132	SLOWH#	23	Vss	160
HA22	83	LA4	134	SPKR	18	XD0	9
HA23	82	LA5	135	ST0	95	XD1	8
HA24	78	LA6	137	ST1	96	XD2	7
HA25	77	LA7	138	ST2	97	XD3	6
HA26	76	LASALE#	136	ST3	98	XD4	5
HA27	75	MACK1#	57	START#	94	XD5	4
HA28	74	MACK2#	56	TESTIN	15	XD6	3
HA29	73	MACK3#	55	TESTOUT	12	XD7	2
HA30	72	MACK4#	54	VDD	1	XDEN#	152
HA31	71	MACK5#	53	VDD	20	XDRD#	154

5. 82C687, OPTi DATA BUS CONTROLLER (DBC)

5.1 FEATURES

The Data Bus Controller (DBC) is a 160-pin PFP (Plastic Flat Package) device. It performs numerous steering logic and control/decode functions. It integrates data buffers and provides data buffer control, XD bus control, AEN generation, parity generation/checking logic, decode logic for an external keyboard controller, real time clock control, system configuration RAM control as well as EISA ID register support and general purpose chip selects. The DBC supports the following features and functions:

* 160-pin Plastic Flat Package
* Data bus conversion
* Data assembly/disassembly for EISA/DMA master accesses
* Parity generation/checking
* Slot specific AEN generation for 8 EISA connectors
* Fast CPU warm reset
* Decodes for Keyboard-controller, RTC, Configuration RAM and Numeric-error clearing
* Provides two programmable general purpose chip-selects
* Supports 4-8k of external CMOS configuration SRAM
* General purpose single bit I/O port
* EISA ID register support
* Built-in Tristate test mode enhances manufacturability

5.1.1 Data Bus Conversion

The DBC performs data bus conversion when a system master accesses 8, 16, or 32-bit devices through 16-bit or 32-bit instructions. The DBC also handles DMA and EISA bus master cycles that transfer data between local DRAM or cache memory and locations on the EISA bus. The DBC receives data buffer control signals from the EBC and the ISP. It generates XD bus control signals XDEN# and XDRD#.

5.1.2 Parity Generation/Detection logic

During local DRAM write cycles, the DBC generates a parity bit for each byte of data from the processor. Parity bits are stored in dedicated local DRAM. During a DRAM read, within the timing window of PAREN#, the DBC checks whether each parity bit is correct for its corresponding data byte. If it detects incorrect parity, the DBC generates a parity error to the ISP. Parity error detection can be disabled through software.

5.1.3 AEN generation

LA[15:8], AEN#, AENLE#, and M/IO are used to generate a unique AENx (AEN[8:1]) for each EISA slot. AENx is used by slot specific I/O slaves during address decoding. When active, this slot specific signal indicates that an I/O on the EISA or ISA bus may respond to the address or I/O command currently on the bus. AENx is asserted high during DMA or refresh cycles to prevent slot specific I/O from misinterpreting DMA or refresh cycles as valid I/O cycles.

5.1.4 Fast Warm Reset

The DBC snoops accesses to I/O address range 0110 X1X0b (64h) and generates ARMRC# (arm the CPU reset) if a value of F0 is written to this area. This allows the DBC to detect and intercept CPU reset commands destined for the keyboard controller. The DBC is able to respond much faster than the 8042 and as a result, system performance is enhanced for those programs using keyboard resets to switch out of protected mode. This "fast warm reset" is supported by the EBC which generates the actual reset signal (RSTCPU) from the DBC's ARMRC# output.

5.1.5 I/O Decode

The DBC generates chip select signals for the keyboard controller, real time clock chip, configuration non-volatile-memory (NVM) and the EBC's configuration registers. It also generates control logic based on address decoding for numeric coprocessor error clearing, the EISA ID register, the real time clock chip, configuration NVM and Fast CPU warm resets.

5.1.6 General Purpose Chip Selects

The DBC provides two programmable general purpose chip select outputs, IOCS1# and IOCS0#. Both outputs can independently decode an I/O block from 1-128 bytes in size located at any multiple of the block size. Each chip select uses the lower 6 bits of a configuration register to store a block mask that corresponds to SA[6:0]. Setting any combination of these bits masks the corresponding address lines and causes them to be ignored in the decoding, thus allowing programmable ranges within the I/O decode. Each chip select also uses a base I/O address, specified in two additional configuration registers. These registers store a starting address corresponding to SA[15:0]. In addition, a configuration register bit for each chip select allows the XDEN# signal to be selectively enabled or disabled based on the motherboard requirements.

IOCS1# uses configuration registers C5h and C4h for the base starting address, C7h<6:0> for the mask register, and C7h<6> to enable XDEN#. The default state of IOCS1# provides a 128-byte block decode starting at address 0 with XDEN# disabled.

IOCS0# uses configuration registers C3h and C2h for the base starting address, C6h<6:0> for the mask register, and C6h<6> to enable XDEN#. The default state of IOCS0# provides a 1-byte decode starting at address 0 with XDEN# disabled.

5.1.7 Configuration Non-Volatile-Memory (NVM)

The DBC provides two modes of supporting configuration non-volatile-memory (NVM). The first method (default) is compatible with DS1488/DS1387 implementations which integrate either 4kB or 8kB of battery-backed CMOS SRAM with a real-time-clock (RTC) chip. The second method is compatible with DS1225 applications which keep the NVM separate from the RTC. Configuration register C00<6> determines which protocol is used.

For the combined NVM/RTC mode, 8k of CMOS SRAM is available with the DS1488 and 4k of SRAM is available with the DS1387. I/O writes to register C01h[4:0] cause the DBC to strobe the upper 5 bits of the address index (A12:A8) into the NVM chip via the XD[4:0] bus. I/O writes to register C08h[7:0] cause the DBC to strobe the lower 8 bits of the address index (A7:A0) into the NVM chip via the XD[7:0] bus. Once the address index is programmed, a read or write to I/O location 08XXh will cause an NVM data access. Note that in this mode, the NVM will respond to any I/O access in the range of 08XXh with the same results since the indexed address is completely specified by I/O writes to registers C01h and C08h. To read a different NVM location, either C01h or C08h must be written with a new index value.

In the separate NVM/RTC mode, the DBC provides access to 4k of battery-backed CMOS SRAM. In this case, the upper four address bits into the CMOS SRAM select a 256-byte NVM page window that is mapped into I/O address space beginning at location 0800h. These four upper address bits are stored in configuration register C00h[3:0] and correspond to output pins PORT[3:0] which are connected to the SRAM's upper address inputs. Once these upper address bits have been programmed, accesses can be made to any NVM byte in the window corresponding to I/O locations 08XXh. Note that all 256 bytes in the same window can be accessed without having to change the contents of C00h[3:0].

5.1.8 General Purpose Single bit I/O port

The DBC defaults to DS1488 mode (combined NVM/RTC, Reg C00h<6>=0). This frees up the PORT0 pin to be used as a general purpose I/O port which can be written to or read from C00h<0>. Register C00<4> selects whether the pin is an input or an output (0=input, 1=output). Note that if the battery-backed SRAM mode is chosen (C00h<6>=1) then this pin is no longer an I/O port and instead functions as an address pin into the SRAM.

5.1.9 EISA ID Registers

Four, byte-wide ports are available as EISA ID registers. These registers are writeable once after a motherboard reset (RST#) and can be read any time the EISA ID register bit is enabled (C00<7>=1). This architecture provides designers with the flexibility of loading the EISA ID registers from the BIOS ROM or else providing a separate PLD/ROM and disabling the EISA ID register bit.

5.1.10 Testability

I/O configuration register C01h<3:0> contains a 4-bit read only value that indicates the revision level of the DBC. This allows the revision level of the DBC to be verified by software.

The DBC includes a tristate test mode to enhance board level testability/manufacturability. When this test mode is entered, all outputs and bidirectional pins become tristated, allowing electrical isolation between the DBC and signals on the PCB.

At the trailing edge of the reset signal (RST#) the DBC samples two pins to determine whether the tristate test mode should be entered. KBDCS#/TMOD# must be low and IO16#/TSEL must be high at this sample point to guarantee entering this test state. The following table illustrates this:

KBDCS#/ TMOD#	PORT0/ TSEL	Function
Low	Low	Reserved
Low	High	Tristate Test Mode
High	X	Normal Operation

5.2 DBC PIN DESCRIPTION

5.2.1 Data Bus Interface

Pin Name	Type	Pin No.	Description
HD[31:0]	B	104,101, 99,95, 93-88, 86-81,79-71, 69,68	***Host Data Bus.*** 32-bit local host bus connected to Host CPU D[31:0]
MD[31:0]	B	124-129, 133-136, 138-142, 144-149, 151-159	***Memory Data Bus.*** 32-bit local DRAM data bus connected to DRAMs.
XD[7:0]	B	54-46	Motherboard Peripheral Data Bus. This 8-bit data bus supports motherboard I/O functions. It is connected to the ISP, MCC, 8042, RTC, Configuration RAM and BIOS ROM

5.2.2 Data Buffer Control

Pin Name	Type	Pin No.	Description
MDHDCLK	I	40	***MD to HD Control Clock.*** The rising edge of this signal is used to clock data from the memory data bus (MD[31:0]) and the memory parity bus (MP[3:0]) into DSC's internal flip-flops. It is connected to MDHDCLK from the MCC.
MDLE[2:0]#	I	36-38	***Memory Data Bus Latch Enables.*** These latch enables allow the DBC to sample data on the MD bus on a byte-by-byte basis. They are used for all EISA/ISA/DMA master writes and read assembly cycles. MDLE0# controls byte-lane 0, MDLE1# controls byte-lane 1 and MDLE2# controls byte-lane 3. Byte-lane 2 is enabled when MDLE2# is active AND SA[1:0] does NOT equal 11b. These signals are connected from the EBC's MDLE[2:0]# output pins.
MDHDOE1# MDHDOE0#	I	32 39	***Memory Data to Host Data Output Enables.*** Both of these signals are normally inactive. When MDHDOE0# is active, data from the MD bus flip-flops are driven onto the HD bus. When MDHDOE1# is active, data from the MD bus latches are driven onto the HD bus . MDHDOE0# is connected to MDHDOE# from the MCC while MDHDOE1# is connected to MDHDOE# from the EBC.
LDMDOE#	I	30	***Latched Data to Memory Data Output Enable.*** When this signal goes active, data from the MD-bus latches are driven back onto the MD bus. LDMDOE# is connected to EBC.
HDMDLE#	I	43	***Host Data to Memory Data Latch Enable.*** This signal enables data from the HD bus to the DBC's internal latches. It is connected to HDMDLE# from the MCC.
HDMDOE#	I	42	***Host Data to Memory Data Output Enable.*** This signal enables data from the HD bus latches to the MD bus (MD[31:0]) and also enables the internally generated parity information onto the MP bus (MP[3:0]). It is connected to HDMDOE# from the MCC.
ROMCS#	I	31	***ROM Chip Select.*** This input is used to qualify XDEN# and XDRD. It is connected to ROMCS0# from the MCC.

MRDC#	I	18	***ISA Memory Read Command.*** This input is used to help decode and generate the XDRD# signal when ROMCS# is active. It is connected to MRDC# of the EISA bus.
RDHLDA	I	25	***Refresh/DMA Hold Acknowledge.*** This input is used to qualify XDEN# and XDRD# during INTA cycles and manufacturer specific I/O decodes. It is connected to RDHLDA from the EBC.
ST2	I	24	***Inter-Chip Status bit-2.*** Connected to ST2 from the EBC.
XDEN#	O	56	***X-Bus Data Enable.*** This control signal enables the transceiver between XD[7:0] and SD[7:0].
XDRD#	O	55	***X-Bus Data Read.*** This control signal sets the direction of the transceiver from XD[7:0] to SD[7:0].

5.2.3 Parity and Control

Pin Name	Type	Pin No.	Description
MP[3:0]	B	119,120, 122,123	***Memory Parity Bus.*** 4-bit bus (one bit per byte) connected to DRAM parity bits.
PAREN#	I	35	***Parity Enable .*** PAREN# provides the timing for generating PARITY# in the event of a parity failure. It is connected to PAREN# of the MCC .
PARITY#	O	44	Parity Error. This signal goes active if during a parity failure if parity is enabled (PAREN#). It is connected to PARITY# of the ISP

5.2.4 I/O Address and Control

Pin Name	Type	Pin No.	Description
LA[15:2]	I	1-6,8-13, 15,16	***EISA/ISA Latched Address Bus.*** This bus is used for AEN[8:1] generation and other I/O decodes. Connected to LA[15:2] of the EISA connectors.
SM/IO#	I	17	***EISA System Memory/IO.*** Used for AEN[8:1] decoding only. It is connected to SM/IO# of the EISA connectors.
SA[1:0]	I	19,21	*EISA System Address Bus bits [1:0].* These two low order address bits are used for I/O decodes and also to enable the proper byte-lane latches on the MD bus. Connected to SA[1:0] of the EISA connectors.
AENLE#	I	28	***AEN Latch Enable.*** The low to high transition of this input latches the current state of AEN[8:1] and all I/O chip-select outputs. It is connected to AENLE# from the EBC.
LASALE#	I	33	***LA Bus Latch Enable.*** The low to high transition of this input signal latches the current state of I/O decodes from the LA bus. It is connected to LASALE# from the EBC.
IORC#	I	22	***EISA I/O Read Command.*** This input is used to generate RTCRD# and XDRD# as well as to enable internal register data onto the XD bus. It is connected to IORC# of the EISA connectors.
IOWC#	I	23	***EISA I/O Write Command.*** This input is used to generate KBDWR#, RSTNERR#, NPRST# and to write to the internal configuration registers. It is connected to IOWC# of the EISA connectors.
AEN#	I	26	***Address Enable.*** AEN indicates that the current address is being driven by the DMA controller. It is used to qualify AEN[8:1] as well as other I/O decodes.

RST#	I	29	***Motherboard Reset.*** This reset input is active when powergood (PWRGD) is low or when the reset switch is active (RESETSW#). It is connected to RST# from EBC and is used to reset the motherboard peripherals.

5.2.5 Fast CPU Reset Control

Pin Name	Type	Pin No.	Description
ARMRC#	O	57	***Arm CPU Reset.*** The DBC snoops accesses to I/O port 0110 X1X0b (64h) and generates ARMRC# if an F0h is written to this location. Warm reset cycle times are greatly reduced through this emulation. This signal is connected to the ARMRC# input of the EBC where it is processed to create the CPURST signal.

5.2.6 I/O decode

Pin Name	Type	Pin No.	Description
AEN[8:1]	O	118..115, 113..110	***Slot Specific AEN Bus.*** Each EISA slot receives a unique AEN signal to indicate whether it can respond to addresses and I/O commands on the EISA bus. Each signal is connected to its corresponding slot-specific AENx on the EISA connectors.
CRAMOE#/ CRAMCS#	O	65	***CMOS RAM Control.*** This signal is active when 08XXh is decoded from LA[15:8] and drives the output enable of the DS1488 and the chip enable (CE#) of the battery-backed CMOS SRAM.
KBDCS#/ TMOD#	B	61	***Keyboard Chip Select or Test Mode.*** This pin has two functions. Normally, it serves as the keyboard chip select output which goes active when address 0110 XXX0b is decoded from LA bus and SA bus addresses. It is connected to the CS# input of the keyboard controller. The second function of this pin is to allow the DBC to enter it's test mode. If this signal is low on the trailing edge of RST# and PORT7/TSEL is high, then the DBC enters its Tristate Test mode. A weak internal pull-up on this signal keeps it high during RST# if no outside tester/source is driving it.
KBDWR#	O	62	***Keyboard Write.*** KBDWR# goes active with IOWC# except when ARMRC# goes active. It is connected WR# of 8042/8742.
NPCS#	O	63	***Numeric Coprocessor Chip Select.*** This output is used by the EBC in its coprocessor qualification logic. It is active for LA[15:3] decodes in the range of 111X 0XXXb when AEN# is inactive. It is connected to NPCS# of the EBC.
RTCDS#	O	59	***Real Time Clock Select.*** This output is active when IORC# or IOWC# is active and 0111 XXX1b is decoded from LA and SA addresses. It is connected to the DS input of the real time clock.
RTCWR#	O	60	***Real Time Clock Read/Write.*** . This signal is active when IOWC# is active and 0111 XXX1b is decoded from LA and SA addresses. It is connected to R/W# of the RTC
EBCCS#	O	45	***EBC Chip Select.*** This output goes active when the I/O address range [C10:C1F]h is decoded from LA[15:2] and AEN#. The EBC uses this signal as a chip select to qualify access to its internal configuration registers. It is connected to EBCCS# of the EBC.

IOCS0#	O	66	***General purpose ISA I/O chip select 0.*** This pin can decode an I/O block of 1-128 bytes located at any multiple of the block size. The address comparison for IOCS0# is done with internal registers at I/O address [C03:C02]h. Additionally, when configuration register C06h<6:0> is set, the corresponding address bits of SA[6:0] are masked in the decoding. Configuration register C06h<7> determines whether XDEN# is active for this chip select (the default state is off for XDEN#). This output defaults to a one byte decode at I/O address 0.
IOCS1#	O	67	***General purpose ISA I/O chip select 1.*** This pin can decode an I/O block of 1-128 bytes located at any multiple of the block size. The address comparison for IOCS0# is done with internal registers at I/O address [C05:C04]h. Additionally, when configuration register C07h<6:0> is set, the corresponding address bits of SA[6:0] are masked in the decoding. Configuration register C07h<7> determines whether XDEN# is active for this chip select (the default state is off for XDEN#). This output defaults to a 128 byte decode at I/O address 0.

5.2.7 Port Control

Pin Name	Type	Pin No.	Description
PORT0/ TSEL	B	105	***Port 0 or Test Mode Select.*** This pin functions as either a parallel I/O port or a test mode select input. When configuration register C00h<6>=0 (default, DS1488 support mode), this becomes a general purpose I/O port written and read at address C00h<0>. This bit is an input if C00h<4>=0 (default) and an output if C00h<4>=1. When C00h<6>=1 (battery-backed SRAM mode), this bit is always an output and is connected to A11 of the SRAM. PORT0/TSEL must be high on the trailing edge of RST# (and KBDCS#/TMOD# must be low) for the chip to enter its tristate test mode. This test mode forces all outputs and bidirectional pins into a tristate configuration.
AS1#/PORT1	O	106	***Addresss Strobe 1 or Port1.*** In DS1488 support mode, AS1# is connected to the corresponding AS1# pin of the DS1488 real time clock. In battery-backed SRAM mode, PORT1 is connected to A9 of the battery-backed CMOS SRAM.
AS0#/PORT2	O	108	***Address Strobe 0 or Port2.*** In DS1488 support mode, AS0# is connected to the corresponding AS0# pin of the DS1488 Real time clock. In battery-backed SRAM mode, PORT2 is connected to A10 of the battery-backed CMOS SRAM.
CRAMWE#/ PORT3	O	109	***CMOS RAM Write Enable or PORT3.*** In DS1488 support mode, CRAMWE# is connected to the WE# pin of the DS1488 real time clock. In battery-backed SRAM mode, PORT3 is connected to A11 of battery-backed CMOS SRAM.

5.2.8 Ground and VCC

Pin Name	Type	Pin Number	Description
VDD	I	20,41,58,80,100,121,143,160	+5V
VSS	I	7,14,27,34,50,64,70,87,107,114,130, 137,150	VSS or Ground

5.3 DBC Register Description

Non-Volatile-Memory (NVM) Access
I/O Address Range: 08XXh

This range defaults to DS1488 Mode (C00h<6>=0). In this combined NVM/RTC mode, any I/O access to the address range 08XXh will cause an access into NVM that corresponds to the address index that was previously written into C01h<4:0> (A12:A8) and C08h<7:0> (A7:A0). Since the complete index is specified by I/O writes to C01h and C08h, the NVM will respond to any I/O access in the range of 08XXh with the same results. ie: The Address range 08XXh just produces a chip select for the NVM while the address of the SRAM was previously specified by I/O writes to C01h and C08h. The DS1488 supports 8k of SRAM and uses C01h<4> (corresponding to SRAM address A12), while the DS1387 supports 4k of SRAM and disregards C01<4>. This fact can be used by software that wishes to determine which chip is installed.

The other mode supported is referred to as battery-backed-SRAM or separate NVM/RTC mode (C00h<6>=1). In this mode, each I/O address in the range 0800h-08FFh corresponds to an entry in the active window of the SRAM. The SRAM chip (typically a DS1225) requires that the upper four address bits (A11:A8) be provided externally. The DBC does this with the PORT[3:0] pins corresponding to register C00h<3:0>. These upper address bits define the 256 byte active window into the NVM. Note that all 256 bytes in the same SRAM window can be accessed without having to change the contents of C00h<3:0>. This mode allows 4kB of SRAM (16 pages x 256 bytes).

DBC Control Register
Index: C00h

BIT	FUNCTION	DEFAULT
7	EISA ID register read control 0 = Internal EISA ID Register reads disabled 1 = Enable reads to Internal EISA ID Registers (BIOS should enable)	0
6	NVM mode select. Supports both a combined NVM/RTC configuration (DS1488 or DS1387 mode) or a separate NVM/RTC configuration (DS1287A RTC plus DS1225 Battery-Backed CMOS) 0 = Combined NVM/RTC (ie:DS1488 or DS1387) 1 = Separate NVM/RTC (ie:DS1287A plus DS1225)	0
5	Unused	X

4	Dependent upon the state of the NVM mode select (C00<6>. If C00<6>=0 (Combined NVM/RTC), then this bit controls the direction of the single bit I/O port at C00h<0> as follows: If bit4 = 0, Then PORT0 = input (C00h<0>) If bit4 = 1 Then PORT0 = output (C00h<0>) If C00h<6>=1 (Separate NVM/RTC), then this bit is unused and PORT0 (C00h<0>) becomes the output A11 to the battery-backed-SRAM.	
3	A11 of NVM address for separate NVM/RTC mode (C00h<6>=1)	
2	A10 of NVM address for separate NVM/RTC mode (C00h<6>=1)	
1	A9 of NVM address for separate NVM/RTC mode (C00h<6>=1)	
0	A8 of NVM address for separate NVM/RTC mode (C00h<6>=1) PORT0, single bit I/O port when combined NVM/RTC mode is selected (C00h<6>=0). Direction is controlled by C00h<4>.	PORT0

Note: Bit 4 - 7 should not be changed when accessing NVM.

DBC Revision-Number Register
Index: C01h

BIT	FUNCTION	DEFAULT
7-0	Reading this register provides the read only revision number of the DBC. When the DBC is configured for combined NVM/RTC (C00h<6>=0), writes to this port location cause the upper 5 bits of the NVM address index (A12:A8) to be strobed into the DS1488 or DS1387 on the XD[4:0] bus.	

IOCS0# Lower Base Address
Index: C02h

BIT	FUNCTION	DEFAULT
7-0	IOCS0# Lower Base starting Address. Compared with SA[7:0] to decode IOCS0#.	0

IOCS0# Upper Base Address
Index: C03h

BIT	FUNCTION	DEFAULT
7-0	IOCS0# Upper Base starting Address. Compared with SA[15:8] to decode IOCS0#.	0

IOCS0# Mask Register
Index: C06h

BIT	FUNCTION	DEFAULT
7	XDEN# select for IOCS0# 0 = XDEN# IS NOT generated for IOCS0# 1 = XDEN# IS generated for IOCS0#	0
6-0	Mask corresponding bits of SA[6:0]	X

IOCS1# Lower Base Address
Index: C04h

BIT	FUNCTION	DEFAULT
7-0	IOCS1# Lower Base starting Address. Compared with SA[7:0] to decode IOCS1#.	0

IOCS1# Upper Base Address
Index: C05h

BIT	FUNCTION	DEFAULT
7-0	IOCS1# Lower Base starting Address. Compared with SA[15:8] to decode IOCS1#.	0

IOCS1# Mask Register
Index: C07h

BIT	FUNCTION	DEFAULT
7	XDEN# select for IOCS1# 0 = XDEN# IS NOT generated for IOCS1# 1 = XDEN# IS generated for IOCS1#	0
6-0	Mask corresponding bits of SA[6:0]	X

Index: C08h
When the DBC is configured for combined NVM/RTC (C00h<6>=0), writes to this port location cause the lower 8 bits of the NVM address index (A7:A0) to be strobed into the DS1488 or DS1387 on the XD[7:0] bus.

EISA-ID Registers
Index: C80h,C81h,C82h,C83h

BIT	FUNCTION	DEFAULT
0-7	EISA ID registers - 4 x 8, write once (after RST#). These registers are initially programmed by the BIOS after a motherboard reset and then they are write protected. They can only be read when the Internal EISA ID register bit is set (C00h<7>=1).	

5.4 AC/DC SPECIFICATIONS

5.4.1 82C687 (DBC) Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	5.5	V
Vo	Output Voltage	-0.5	5.5	V
Top	Operating Temperature	-25	70	C
Tstg	Storage Temperature	-40	125	C

Note: Permanent device damage may occur if Absolute maximum Ratings are exceeded.

5.4.2 82C687 (DBC) DC Characteristics

Temperature: 0C to 70C, Vcc: 5V +/- 5%

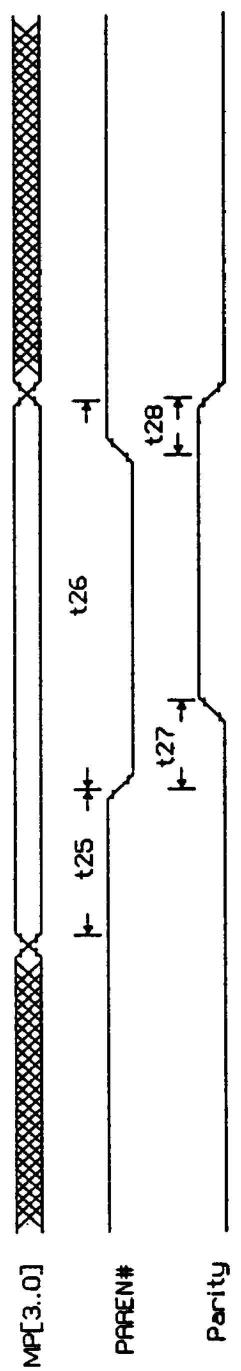
Sym	Description	Min	Max	Units
VIL	Input Low Voltage		0.8	V
VIH	Input High Voltage		2.0	V
VOL	Output Low Voltage (IOL = 4.0 mA)		0.4	V
VOH	Output High Voltage (IOH = -1.6mA)	2.4		V
IIL	Input Leakage Current, VIN = Vcc		10	uA
IOZ	Tristate Leakage Current		10	uA
CIN	Input Capacitance		20	pF
COUT	Output Capacitance		20	pF
ICC	Power Supply Current			mA

5.4.3 82C687(DBC) A.C. Specification Tables

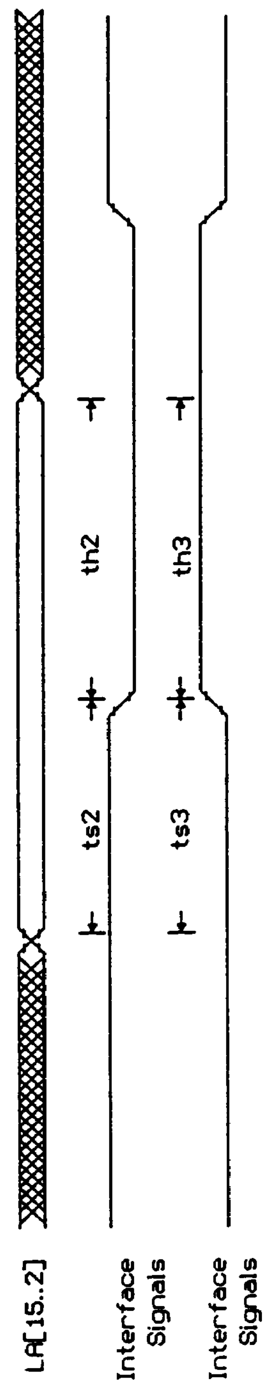
Sym	Description	Min	Typ	Max
t1	HD[31:0] propagation delay from MDHDCLK	5		18
t2	MD[31:0] propagation delay from HDMDLE#	5		18
t3	MP[3:0] propagation delay from HDMDLE#	7		20
t4	MDHDCLK setup time from MD[31:0]	5		18
t5	MDHDCLK hold time from MD[31:0]	5		18
t6	MDLE[2..0]# setup time to MD[31:0]	5		18
t7	MDLE[2..0]# hold time from MD[31:0]	5		18
t8	MDHDOE[2..0]# setup time to MD[31:0]	5		18
t9	MDHDOE[2..0]# hold time from MD	5		18
t10	HDMDLE# setup time to HD[31:0]	5		18
t11	HDMDLE# hold time from HD[31:0]	5		18
t12	HDMDOE# setup time to HD[31:0]	5		18
t13	HDMDOE# hold time from HD[31:0]	5		18
t14	MRDC# setup time to LA[15..2]	5		18
t15	MRDC# hold time from LA[15..2]	5		18
t16	RDHLDA setup time from LA[15..2]	5		18
t17	RDHLDA hold time from LA[15..2]	5		18
t18	ST2 setup time LA[15..2]	5		18
t19	ST2 hold time from LA[15..2]	5		18
t20	XDEN# active delay from LA[15..2]	4		16
t21	XDEN# inactive delayfrom LA[15..2]	5		18
t22	XDRD# active delay from MRDC#	4		16
t23	XDRD# inactive delay from MRDC#	5		18
t24	PAREN# setup time from MP[3..0]	5		18
t25	PAREN# hold time from MP[3..0]	5		18
t26	PARITY# active delay from PAREN#	5		18
t27	PARITY# inactive delay from PAREN#	5		18
t28	SM/IO# hold time from LA[15..2]	5		18
t29	SM/IO# setup time from LA[15..2]	5		18
t30	AENLE# hold time from LA[15..2]	5		18
t31	AENLE# setup time from LA[15..2]	5		18
t32	LASALE# hold time from LA[15..2]	5		18
t33	LASALE# setup time from LA[15..2]	5		18
t34	IORC# hold time from LA[15..2]	6		20
t35	IORC# setup time from LA[15..2]	6		20
t36	IOWC# hold time from LA[15..2]	6		20
t37	IOWC# setup time from LA[15..2]	6		20
t38	AEN# hold time from LA[15..2]	6		20
t39	AEN# setup time from LA[15..2]	6		20
t40	ARMRC# active delay from IOWC#	4		16

5.4.3 82C687(DBC) A.C. Specification Tables (Continued)

Sym	Description	Min	Typ	Max
t41	ARMRC# inactive delay from IOWC#	5		18
t42	AEN[8..1] active delay from LA[15..2]	6.5		20
t43	AEN[8..1] inactive delay from LA[15..2]	8.5		22
t44	CRAMOE# active delay from LA[15..2]	6.5		20
t45	CRAMOE# inactive delay from LA[15..2]	8.5		22
t46	CRAMCS# active delay from IORC#	6.5		20
t47	CRAMCS# inactive delay from IORC#	8.5		22
t48	KBDCS#/TMOD# active delay from LA[15..2]	6.5		20
t49	KBDCS#/TMOD# inactive delay from LA[15..2]	8.5		22
t50	KBDWR# active delay frim IOWC#	4		16
t51	KBDWR# inactive delay from IOWC#	5		18
t52	NPCS# active delay from IOWC#	4		16
t53	NPCS# inactive delay from IOWC#	5		18
t54	RTCRD# active delay from IORC#	4		16
t55	RTCRD# inactive delay from IORC#	5		18
t56	RTCWR# active delay from IOWC#	4		16
t57	RTCWR# inactive delay from IOWC#	5		18
t58	EBCCS# active delay from LA[15..2]	6.5		20
t59	EBCCS# inactive delay from LA[15..2]	8.5		22
t60	PORT0/TSEL active delay from IOWC#	5		18
t61	PORT0/TSEL inactive delay from IOWC#	7		20
t62	AS1#/PORT1 active delay from IOWC#	5		18
t63	AS1#/PORT1 inactive delay from IOWC#	7		20
t64	AS0#/PORT2 active delay from IOWC#	5		18
t65	AS0#/PORT2 inactive delay from IOWC#	7		20
t66	CRAMWE#/PORT3 active delay from IOWC#	5		18
t67	CRAMWE#/PORT3 inactive delay from IOWC#	7		20

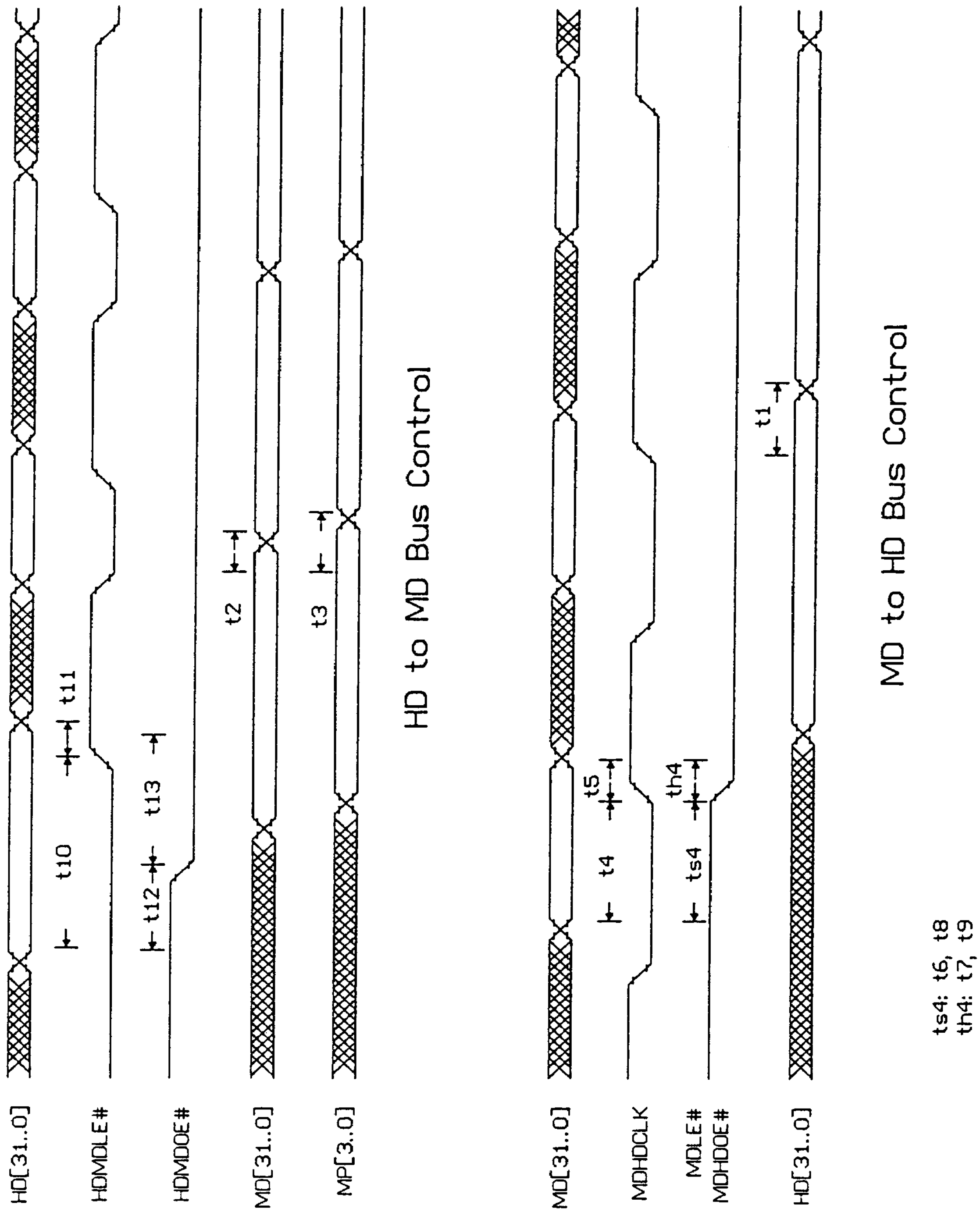


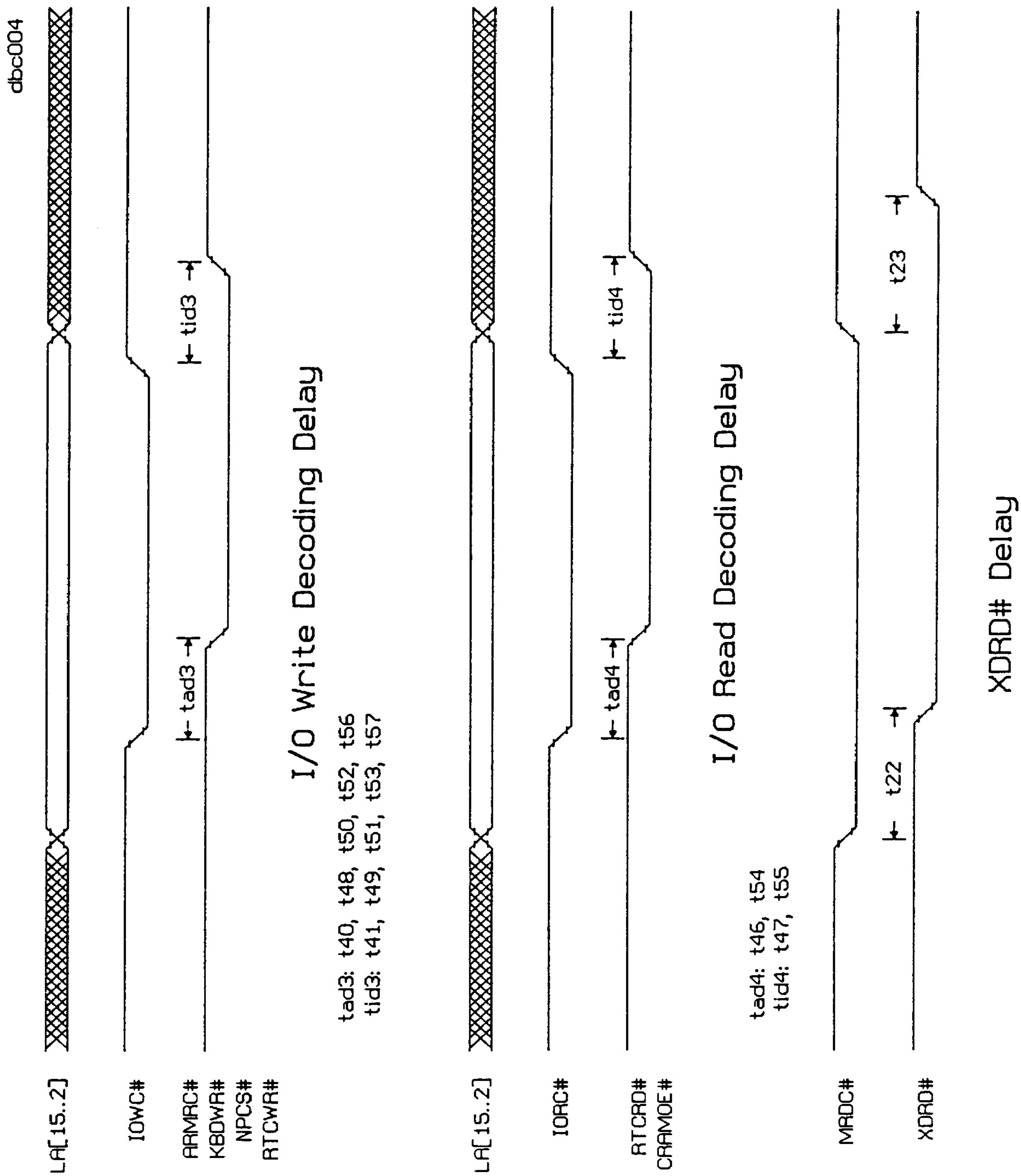
Parity Generation

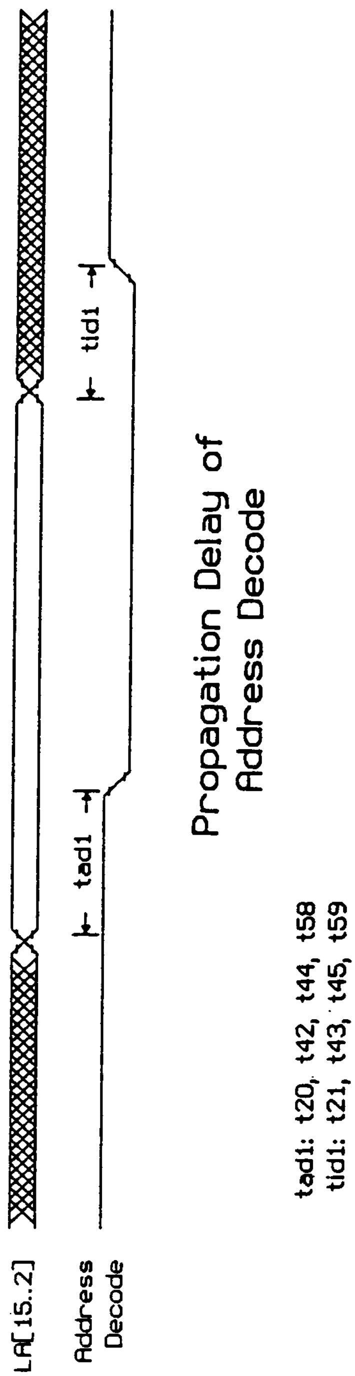


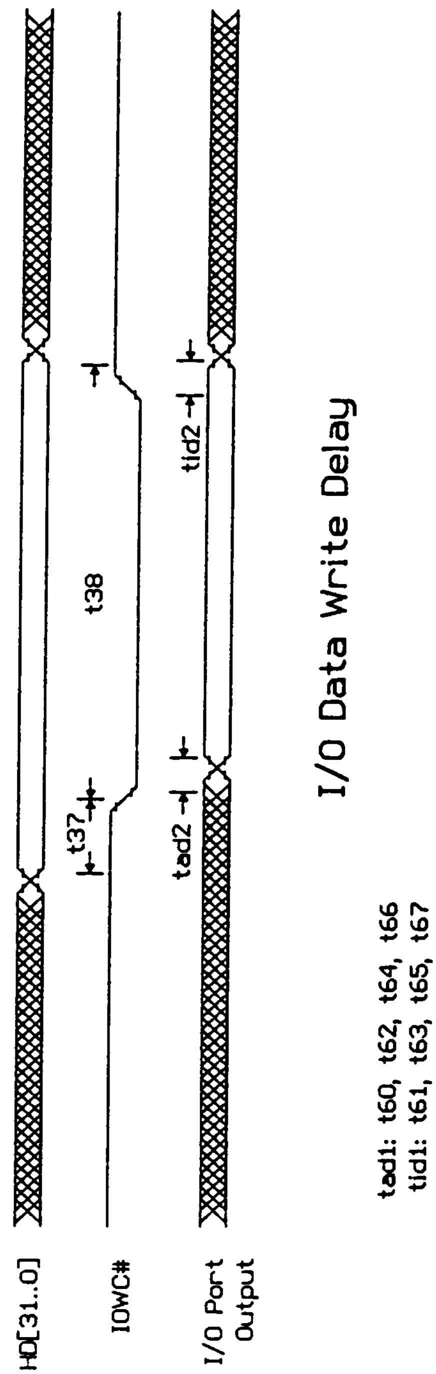
Setup and Hold Time for DBC Interface Signals

ts2: t14, t28, t30, t32, t34, t38
th2: t15, t29, t31, t33, t35, t39
ts3: t16, t18
th3: t17, t19

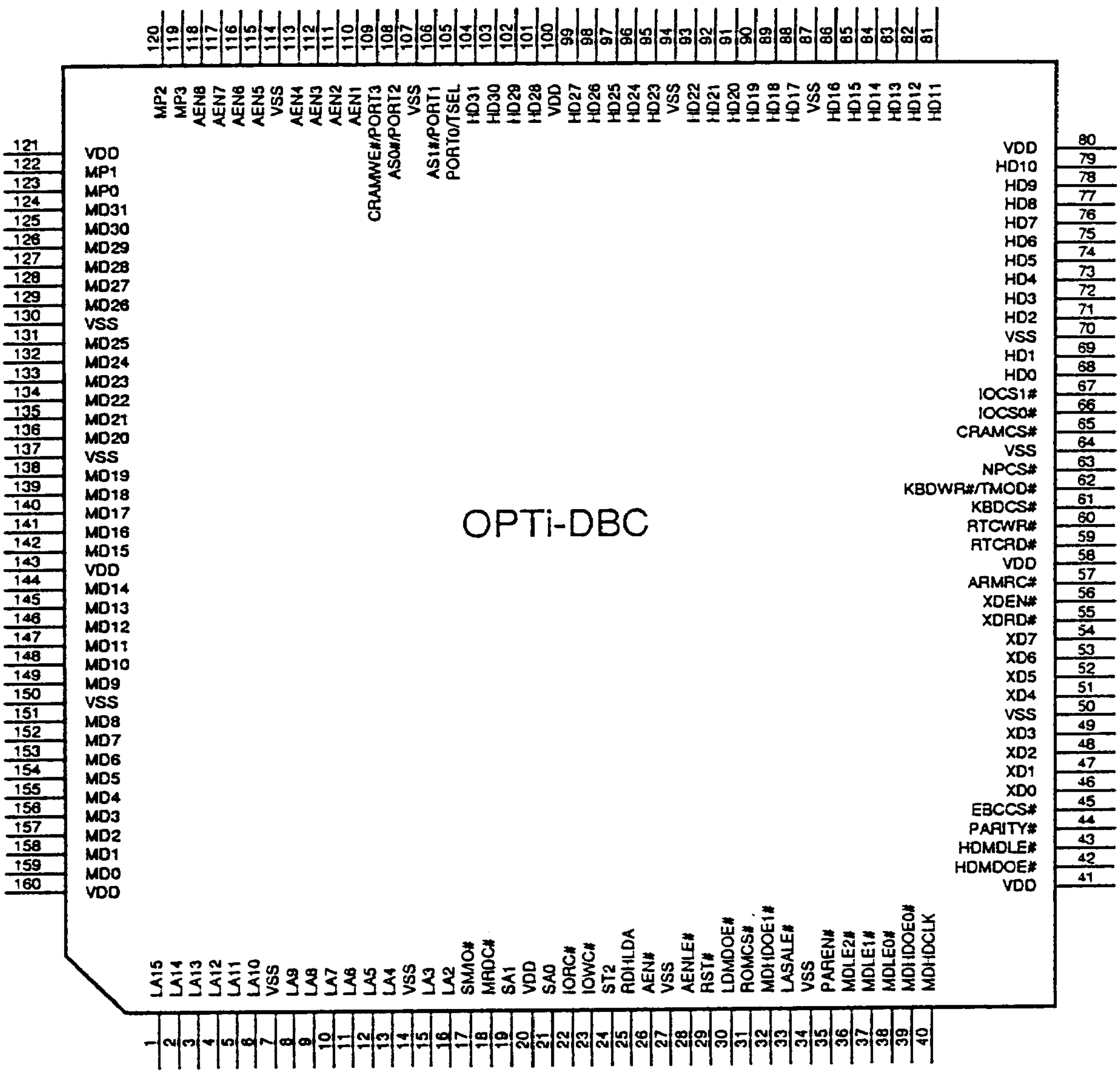

HD[31..0]
HDMDLE#
HDMDOE#
MD[31..0]
MP[3..0]
t10
t11
t12
t13
t2
t3
HD to MD Bus Control
MD[31..0]
MDHDCLK
MDLE#
MDHDOE#
HD[31..0]
t4
t5
ts4
th4
t1
MD to HD Bus Control
ts4: t6, t8
th4: t7, t9


dbc004
LA[15..2]
IOWC#
ARMRC#
KBDWR#
NPCS#
RTCWR#
tad3
tid3
I/O Write Decoding Delay
tad3: t40, t48, t50, t52, t56
tid3: t41, t49, t51, t53, t57
LA[15..2]
IORC#
RTCRD#
CRAMOE#
tad4
tid4
I/O Read Decoding Delay
tad4: t46, t54
tid4: t47, t55
MRDC#
XDRD#
t22
t23
XDRD# Delay


LA[15..2]
Address Decode
tad1
tid1
Propagation Delay of Address Decode
tad1: t20, t42, t44, t58
tid1: t21, t43, t45, t59


HD[31..0]
IOWC#
I/O Port Output
t37
t38
tad2
tid2
I/O Data Write Delay
tad1: t60, t62, t64, t66
tid1: t61, t63, t65, t67

5.5 82C687 DBC PIN-OUT

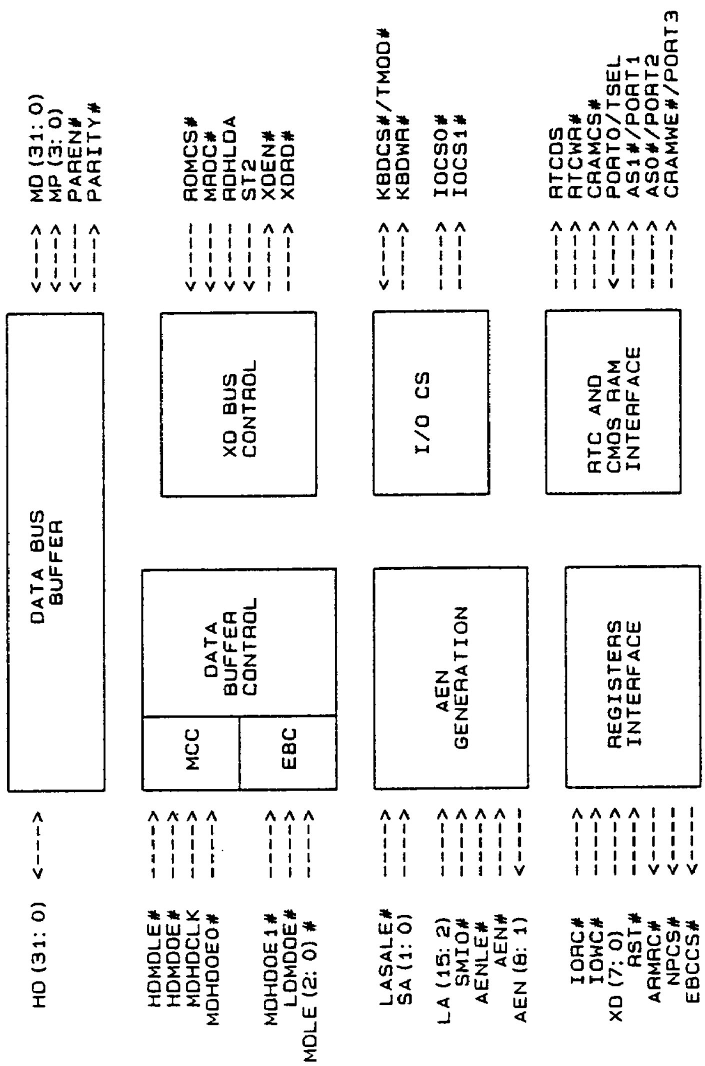


5.5.1 82C687, DBC Numeric Cross Reference

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	LA15	41	VDD	81	HD11	121	VDD
2	LA14	42	HDMDOE#	82	HD12	122	MP1
3	LA13	43	HDMDLE#	83	HD13	123	MP0
4	LA12	44	PARITY#	84	HD14	124	MD31
5	LA11	45	EBCCS#	85	HD15	125	MD30
6	LA10	46	XD0	86	HD16	126	MD29
7	Vss	47	XD1	87	Vss	127	MD28
8	LA9	48	XD2	88	HD17	128	MD27
9	LA8	49	XD3	89	HD18	129	MD26
10	LA7	50	Vss	90	HD19	130	Vss
11	LA6	51	XD4	91	HD20	131	MD25
12	LA5	52	XD5	92	HD21	132	MD24
13	LA4	53	XD6	93	HD22	133	MD23
14	Vss	54	XD7	94	Vss	134	MD22
15	LA3	55	XDRD#	95	HD23	135	MD21
16	LA2	56	XDEN#	96	HD24	136	MD20
17	SM/IO#	57	ARMRC#	97	HD25	137	Vss
18	MRDC#	58	VDD	98	HD26	138	MD19
19	SA1	59	RTCRD#	99	HD27	139	MD18
20	VDD	60	RTCWR#	100	VDD	140	MD17
21	SA0	61	KBDCS#	101	HD28	141	MD16
22	IORC#	62	KBDWR#/TMOD#	102	HD29	142	MD15
23	IOWC#	63	NPCS#	103	HD30	143	VDD
24	ST2	64	Vss	104	HD31	144	MD14
25	RDHLDA	65	CRAMCS#	105	PORT0/TSEL	145	MD13
26	AEN#	66	IOCS0#	106	AS1#/PORT1	146	MD12
27	Vss	67	IOCS1#	107	Vss	147	MD11
28	AENLE#	68	HD0	108	AS0#/PORT2	148	MD10
29	RST#	69	HD1	109	CRAMWE#/PORT3	149	MD9
30	LDMDOE#	70	Vss	110	AEN1	150	Vss
31	ROMCS#	71	HD2	111	AEN2	151	MD8
32	MDHDOE1#	72	HD3	112	AEN3	152	MD7
33	LASALE#	73	HD4	113	AEN4	153	MD6
34	Vss	74	HD5	114	Vss	154	MD5
35	PAREN#	75	HD6	115	AEN5	155	MD4
36	MDLE2#	76	HD7	116	AEN6	156	MD3
37	MDLE1#	77	HD8	117	AEN7	157	MD2
38	MDLE0#	78	HD9	118	AEN8	158	MD1
39	MDHDOE0#	79	HD10	119	MP3	159	MD0
40	MDHDCLK	80	VDD	120	MP2	160	VDD

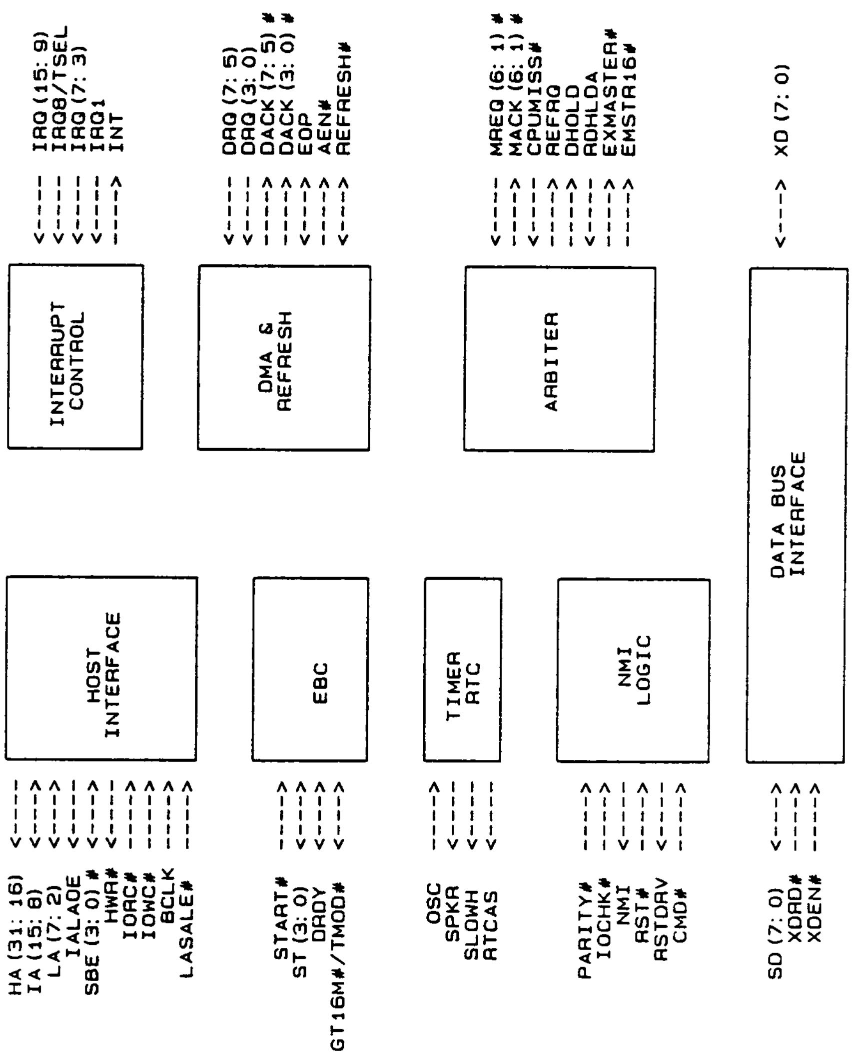
5.5.2 82C687, DBC Alphabetic Cross Reference

Name	Pin	Name	Pin	Name	Pin	Name	Pin
AEN#	26	HD30	103	MD16	141	ROMCS#	31
AEN1	110	HD31	104	MD17	140	RST#	29
AEN2	111	HD4	73	MD18	139	RTCRD#	59
AEN3	112	HD5	74	MD19	138	RTCWR#	60
AEN4	113	HD6	75	MD2	157	SA0	21
AEN5	115	HD7	76	MD20	136	SA1	19
AEN6	116	HD8	77	MD21	135	SM/IO#	17
AEN7	117	HD9	78	MD22	134	ST2	24
AEN8	118	HDMDLE#	43	MD23	133	VDD	20
AENLE#	28	HDMDOE#	42	MD24	132	VDD	41
ARMRC#	57	IOCS0#	66	MD25	131	VDD	58
AS0#/PORT2	108	IOCS1#	67	MD26	129	VDD	80
AS1#/PORT1	106	IORC#	22	MD27	128	VDD	100
CRAMCS#	65	IOWC#	23	MD28	127	VDD	121
CRAMWE#/PORT3	109	KBDCS#	61	MD29	126	VDD	143
EBCCS#	45	KBDWR#/TMOD#	62	MD3	156	VDD	160
HD0	68	LA10	6	MD30	125	Vss	7
HD1	69	LA11	5	MD31	124	Vss	14
HD10	79	LA12	4	MD4	155	Vss	27
HD11	81	LA13	3	MD5	154	Vss	34
HD12	82	LA14	2	MD6	153	Vss	50
HD13	83	LA15	1	MD7	152	Vss	64
HD14	84	LA2	16	MD8	151	Vss	70
HD15	85	LA3	15	MD9	149	Vss	87
HD16	86	LA4	13	MDHDCLK	40	Vss	94
HD17	88	LA5	12	MDHDOE0#	39	Vss	107
HD18	89	LA6	11	MDHDOE1#	32	Vss	114
HD19	90	LA7	10	MDLE0#	38	Vss	130
HD2	71	LA8	9	MDLE1#	37	Vss	137
HD20	91	LA9	8	MDLE2#	36	Vss	150
HD21	92	LASALE#	33	MP0	123	XD0	46
HD22	93	LDMDOE#	30	MP1	122	XD1	47
HD23	95	MD0	159	MP2	120	XD2	48
HD24	96	MD1	158	MP3	119	XD3	49
HD25	97	MD10	148	MRDC#	18	XD4	51
HD26	98	MD11	147	NPCS#	63	XD5	52
HD27	99	MD12	146	PAREN#	35	XD6	53
HD28	101	MD13	145	PARITY#	44	XD7	54
HD29	102	MD14	144	PORT0/TSEL	105	XDEN#	56
HD3	72	MD15	142	RDHLDA	25	XDRD#	55



DBC BLOCK DIAGRAM

4.5 82C686, ISP PIN-OUT

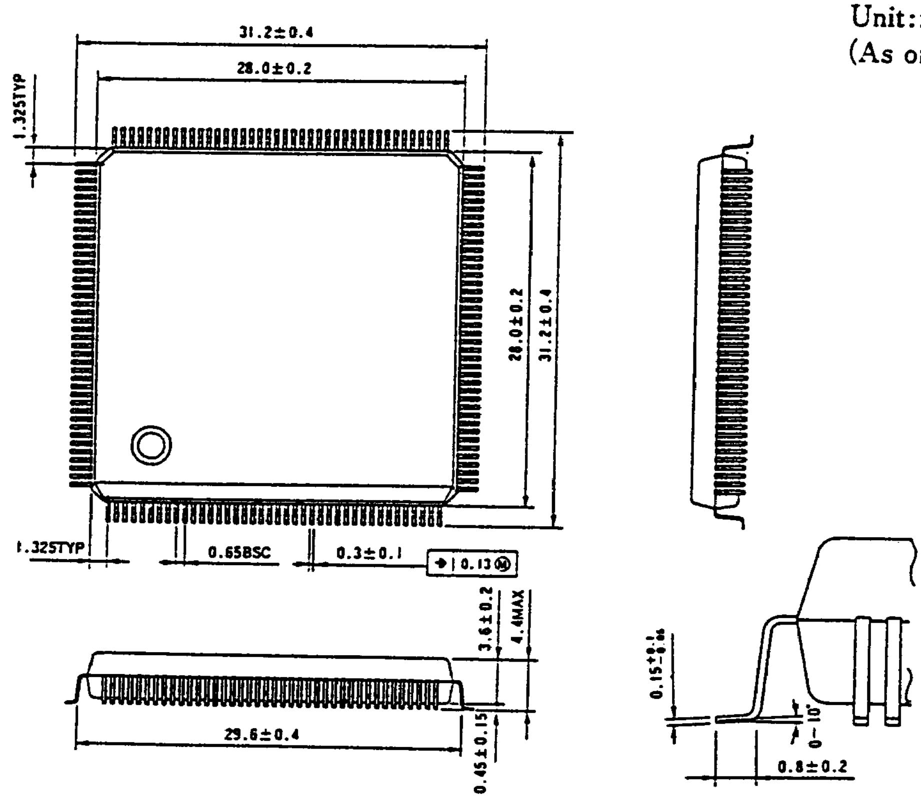


ISP BLOCK DIAGRAM

160-Pin Plastic Flat Package

QFP160-P-2828(160-Pin Plastic Flat Package)

TENTATIVE
Unit: mm
(As of Jul. '89)



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