I-Cube®

LS101

25 Port LAN Switching Element

Features

- Single chip, Fast Ethernet switching fabric
- Up to 100 Mbit per-port switching capacity
- Supports 25 full duplex ports
- Dedicated Multicast output port
- Port mirroring logic
- Simple in-band signaling protocol
- Integrated arbitration logic with round robin arbitration and four priority levels
- 100% JTAG compliant
- 0.5 micron, 3.3V CMOS technology
- 144 Pin TQFP or PQFP package

Description

The LS101 is a 25 port Fast Ethernet, packet switching fabric. It integrates a 100 Mbit per port, full duplex, non-blocking, crossbar switch and switch arbitration logic into a single high density device.

In-band signaling is used to deliver signaling packets to the arbitration logic. A flexible arbitration architecture supports a round robin priority scheme with four levels of priority. The arbitration logic manages all connection setup and teardown functions through the switching matrix.

Although targeted at Fast Ethernet applications, the LS101 may be used as the switching fabric for a wide range of packet switching applications including Frame Relay, FDDI, and Token-Ring.

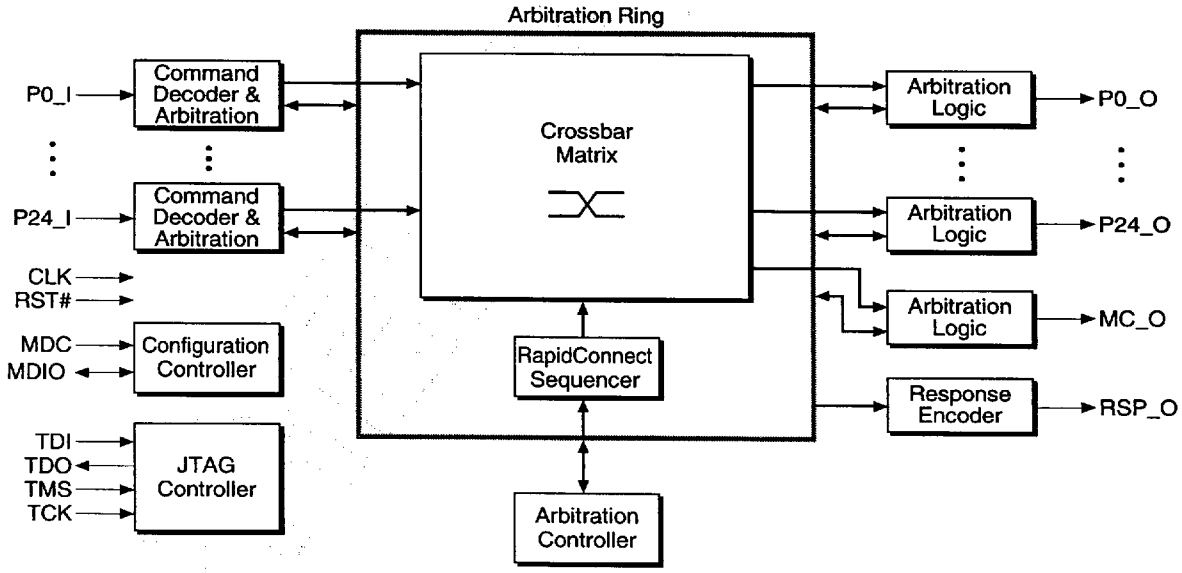


Figure 1: LS101 Functional Block Diagram

April 25, 1997

Confidential

Table of Contents

Introduction

The LS101 is a 25 port switching element for the LS Ethernet SwitchSet™. When combined with other members of the LS family it provides the backbone of a scalable, non-blocking, switching architecture. The key to these features lies in the use of I-Cube's PSID™ crossbar technology for the switch fabric. 25 non-blocking 100 Mb ports are currently supported, with port counts in the hundreds achievable.

Figure 2 shows how the LS101 and LS100 quad port controller can be combined to create a scalable workgroup switching hub. Variations of this architecture can be used for backbone and stackable switch applications.

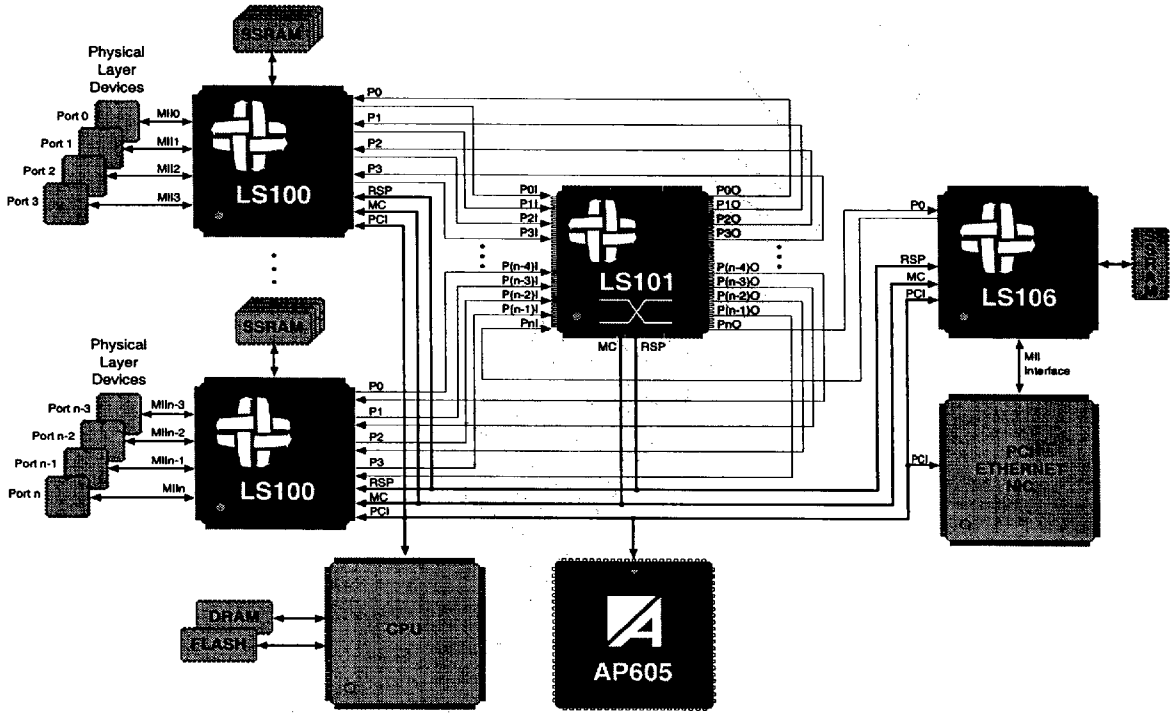


Figure 2: LS Based Workgroup Switch

Packets are transferred between input and output ports by connections established through the switch. These connections are dynamic and are constructed on a demand basis. Requests for connections through the switch are generated by the quad-port ethernet switch devices (LS100s). These requests are sent to the LS101 via the same port interfaces used to transfer the packet data. This process is referred to as in-band signaling. The 4B5B coding scheme used by the LS101 lets it discriminate between packet data and signaling data.

The port datapaths between the LS100s and LS101 are two bits wide. Each general purpose port consists of separate input and output pins, allowing full duplex operation. Each port is identified by a unique port code. The following table shows the port codes recognized by the LS101.

Port Name	Port Code	Description
RSVRD	255	Reserved Port ID
MC	254	Multicast Port
RSVRD	253	Reserved Port ID
⋮	⋮	⋮
RSVRD	25	Reserved Port ID
P24	24	Port 24
P23	23	Port 23
⋮	⋮	⋮
P1	1	Port 1
P0	0	Port 0

Table 1: Switch Ports

In addition to the 25 identical general purpose ports there are two specialized ports. The first of these is the Multicast (MC) port. This port is used to distribute broadcast and multicast packet traffic to the multicast ports on the LS100s.

The second specialized port is the Response (RSP) port. This port is used to distribute response packets to input port connection requests. The response port supports a four bit wide datapath to reduce signaling response times.

LS101 Functional Blocks

Crossbar Matrix

The core of the switch is the Crossbar Matrix. Based on I-Cube's PSID crossbar technology, the matrix is a high performance, non-blocking crossbar switch. The non-blocking feature ensures that there is no interference between two traffic streams that exit the switch through separate ports. This not only insures simultaneous and independent data flow between the ports but the LS101 also supports full duplex data flow on each of them.

Command Decoders

All input ports contain a command decoder observing the data stream entering the port. Each command decoder examines the incoming 4B5B code stream looking for commands directed to the LS101. These commands are contained within Signaling PDUs (Protocol Data Units). Signaling PDUs cannot appear in the middle of any data packets. When detected, commands are decoded into control signals for the other functional blocks.

Arbitration Controller

Arbitration between port connection requests is performed by distributed arbitration logic located in both the input and output block for each port. The arbitration logic in the port blocks interacts by way of an arbitration ring that connects all of the elements involved in port arbitration. The arbitration controller manages the overall sequencing of arbitration cycles. Four levels of priority are supported.

RapidConnect™ Sequencer

After an arbitration cycle has been completed, the RapidConnect Sequencer establishes connections through the switching fabric. It translates port connection requests into configuration cycles for the Crossbar Matrix. These configuration cycles make or break connections within the crossbar by manipulating the state of the configuration memory.

Response Encoder

The Response Encoder generates Response PDUs (Protocol Data Units) under control of the Sequencer. Response PDUs are used to inform port interfaces of connection request status and error conditions. Response PDUs are transmitted via the RSP Port to all the port controllers connected to the LS101.

Multicast Output Port

The Multicast output port on the LS101 is used to distribute broadcast and multicast packet traffic to the multicast ports on the LS100s. It is a separate output port that is addressed by a special port number (see Table 1). The Multicast port is identical to all the other ports on the LS101 except that it does not have an associated input port (it is output only).

Port Mirroring

Any one of the LS101's input ports can be monitored or mirrored by connecting it to an analyzer port. The analyzer port can be any one of the LS101's output ports. This connection is done at the system level and is static as long as its enabled. The selection of the mirrored port number, the analyzer port number and the enable for mirroring is defined via the Configuration Controller.

Configuration Controller

The Configuration Controller supports access to the chip's configuration registers via the MII management protocol (MDC/MDIO). These serial communication lines are used to access these registers. The LS101 uses 30 as its MII address.

JTAG Controller

The LS101 supports the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The same interface can also be used for serially downloading a configuration bit stream into the device.

Pin Description

Pin Name	Type	Description
CLK	Input	System Clock. All switch timing to and from the device is relative to this clock input. This includes the switch input and output ports (P[24:0]_I[1:0] and P[24:0]_O[1:0]) the multicast port (MC_O[1:0]) and the response port (RSP_O[3:0]).
MC_O[1:0]	Output	Multicast Port. The multicast port is an output only version of one of the switch ports and it operates identically to an Output Port. It is connected to by a special port number defined in table 1. The CMOS MC_O[1:0] output pins are designed to go to many devices in a system. Their AC drive is 8mA (DC is 2mA) and their timing is specified with a large load (68pF). Careful layout and routing of these nets in a system is critical.
MDC	Input	Configuration Controller Clock. Used to clock in the serial data stream on the MDIO line.
MDIO	Bidirectional	Configuration Controller Data. Mode, address and data pin for the IEEE 802.3u's MII Management Register interface.
P[24:0]_I[1:0]	Input	Input Ports 0-24 (2 per port). The switch inputs for ports 0 to 24. Unused inputs can be left floating. Setup and hold time specifications must be met for proper operation.
P[24:0]_O[1:0]	Output	Output Ports 0-24 (2 per port). The switch outputs for ports 0 to 24. These CMOS output pins are designed to go to only one device in a system. As such their AC drive is 4mA (DC is 2mA) and their timing is specified with a light load (20pF).
RSP_O[3:0]	Output	Response Port. The result of any switch connection request is output on these pins. The CMOS RSP_O[3:0] pins are designed to go to many devices in a system. Their AC drive is 8mA (DC is 2mA) and their timing is specified with a large load (68pF). Careful layout and routing of these nets in a system is critical.
RST#	Input	Chip and JTAG Reset. This input resets the entire device. It must be connected to the system reset signal.
TCK	Input	JTAG Clock. If JTAG is not used this input can be left floating.
TDI	Input	JTAG Data In. If JTAG is not used this input can be left floating.
TDO	Output	JTAG Data Out. This CMOS output is designed to go to one device in the system. Its AC drive is 4mA (DC is 2mA) and its timing is specified with a light load (20pF).
TMS	Input	JTAG Mode Select. If JTAG is not used this input can be left floating.
DV_{DD}	Power	+3.3V Power for the Core. Bypass capacitors are required on both these pins.
DV_{SS}	Ground	Ground for the Core. Tie these pins to system ground. DV_{SS} and OV_{SS} are connected internally in the device.
OV_{DD}	Power	+3.3V Power for the I/O. Bypass capacitors are recommended on at least half of these pins evenly distributed around the device.
OV_{SS}	Ground	Ground for the I/O. Tie these pins to system ground. OV_{SS} and DV_{SS} are connected internally in the device.

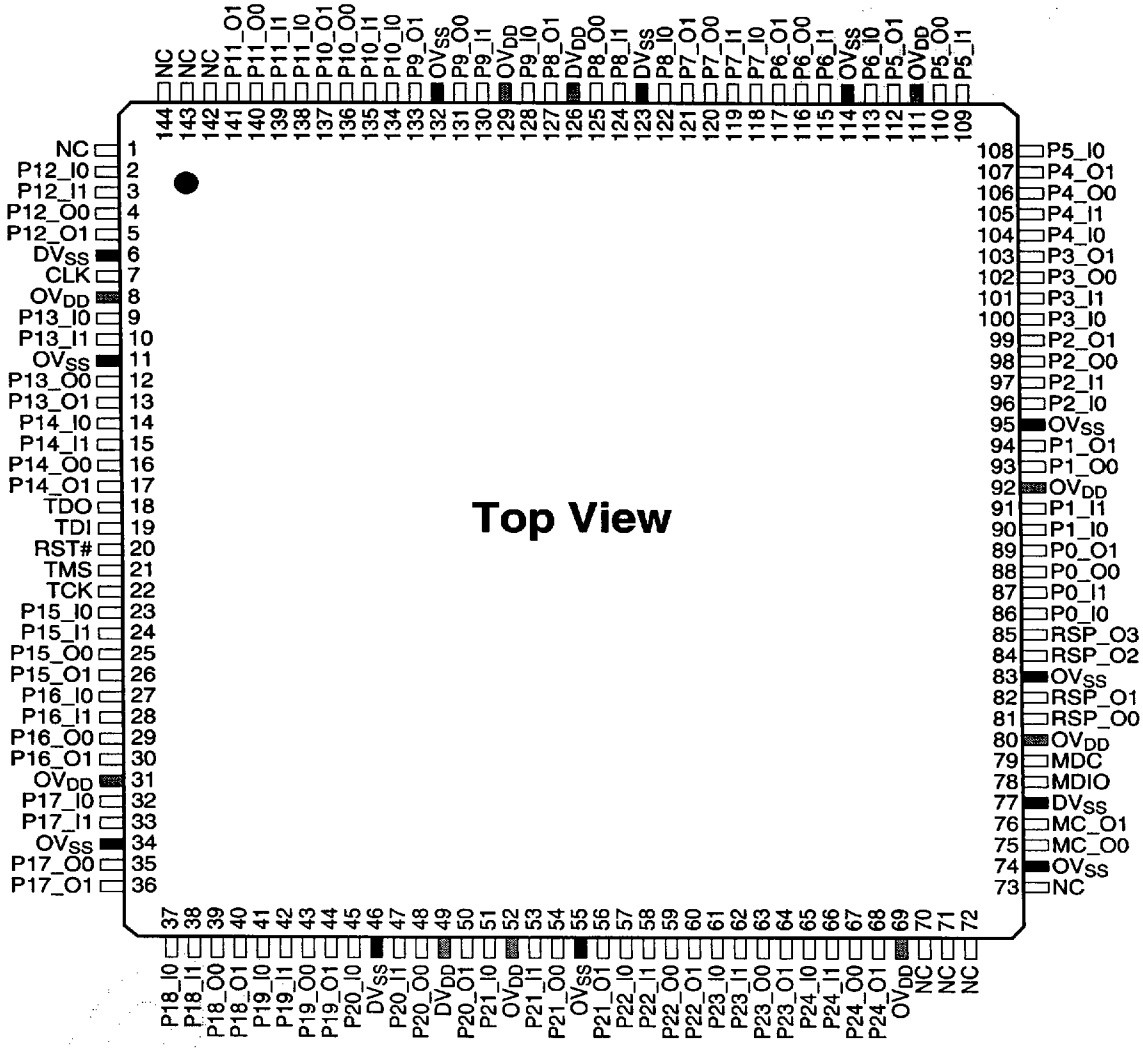
Table 2: Pin Description

Pinout

LS101 [PQFP/TQFP/144 Package] Pinout

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #
CLK	7	P2_I1	97	P11_I1	139	P20_I1	47
DV_{DD}	49	P2_O0	98	P11_O0	140	P20_O0	48
DV_{DD}	126	P2_O1	99	P11_O1	141	P20_O1	50
DV_{SS}	6	P3_I0	100	P12_I0	2	P21_I0	51
DV_{SS}	46	P3_I1	101	P12_I1	3	P21_I1	53
DV_{SS}	77	P3_O0	102	P12_O0	4	P21_O0	54
DV_{SS}	123	P3_O1	103	P12_O1	5	P21_O1	56
MC_O0	75	P4_I0	104	P13_I0	9	P22_I0	57
MC_O1	76	P4_I1	105	P13_I1	10	P22_I1	58
MDC	79	P4_O0	106	P13_O0	12	P22_O0	59
MDIO	78	P4_O1	107	P13_O1	13	P22_O1	60
OV_{DD}	8	P5_I0	108	P14_I0	14	P23_I0	61
OV_{DD}	31	P5_I1	109	P14_I1	15	P23_I1	62
OV_{DD}	52	P5_O0	110	P14_O0	16	P23_O0	63
OV_{DD}	69	P5_O1	112	P14_O1	17	P23_O1	64
OV_{DD}	80	P6_I0	113	P15_I0	23	P24_I0	65
OV_{DD}	92	P6_I1	115	P15_I1	24	P24_I1	66
OV_{DD}	111	P6_O0	116	P15_O0	25	P24_O0	67
OV_{DD}	129	P6_O1	117	P15_O1	26	P24_O1	68
OV_{SS}	11	P7_I0	118	P16_I0	27	RSP_O0	81
OV_{SS}	34	P7_I1	119	P16_I1	28	RSP_O1	82
OV_{SS}	55	P7_O0	120	P16_O0	29	RSP_O2	84
OV_{SS}	74	P7_O1	121	P16_O1	30	RSP_O3	85
OV_{SS}	83	P8_I0	122	P17_I0	32	RST#	20
OV_{SS}	95	P8_I1	124	P17_I1	33	TCK	22
OV_{SS}	114	P8_O0	125	P17_O0	35	TDI	19
OV_{SS}	132	P8_O1	127	P17_O1	36	TDO	18
P0_I0	86	P9_I0	128	P18_I0	37	TMS	21
P0_I1	87	P9_I1	130	P18_I1	38	NC	1
P0_O0	88	P9_O0	131	P18_O0	39	NC	70
P0_O1	89	P9_O1	133	P18_O1	40	NC	71
P1_I0	90	P10_I0	134	P19_I0	41	NC	72
P1_I1	91	P10_I1	135	P19_I1	42	NC	73
P1_O0	93	P10_O0	136	P19_O0	43	NC	142
P1_O1	94	P10_O1	137	P19_O1	44	NC	143
P2_I0	96	P11_I0	138	P20_I0	45	NC	144

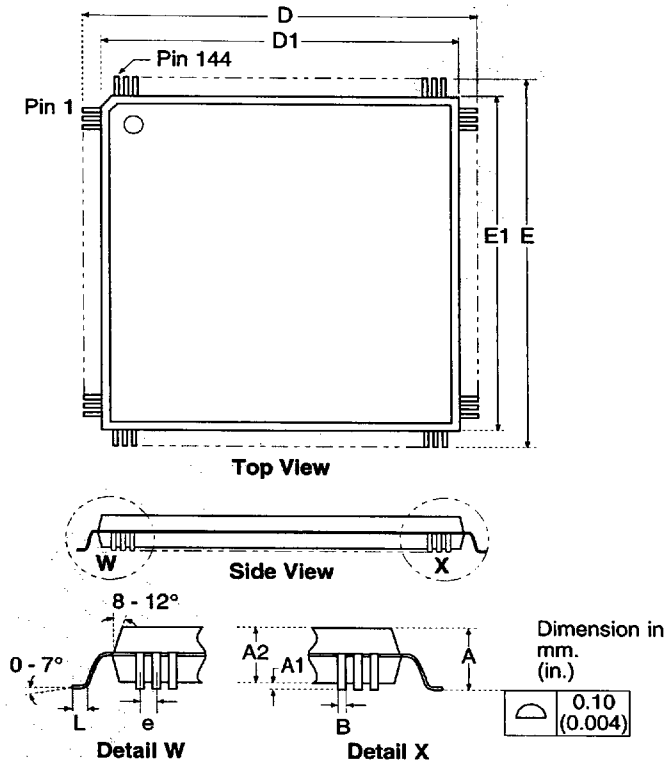
LS101 [PQFP/TQFP/144 Package] Pinout



Confidential

Mechanical Specifications

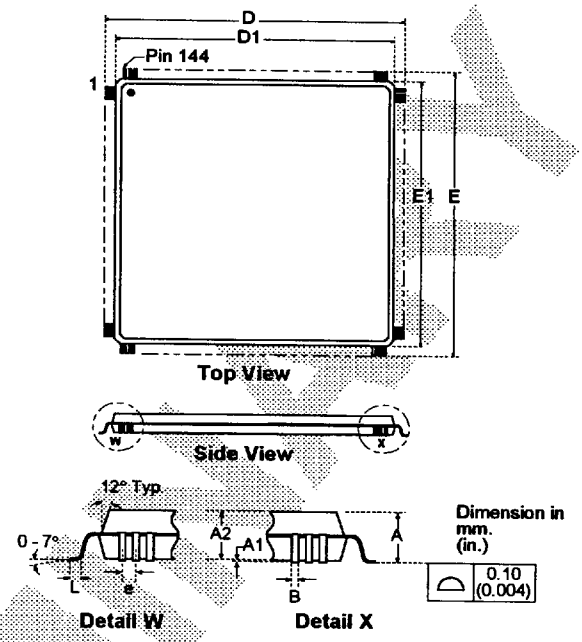
PQ144 Package Dimensions



Package Dimension Table		PQFP/144L	
		inch	mm
A	max	0.157	3.99
A1	min	0.010	0.25
	max	0.017	0.43
A2	min	0.135	3.43
	max	0.140	3.56
D	min	1.219	31.01
	max	1.238	31.49
D1	min	1.098	27.93
	max	1.106	28.14
E	min	1.219	31.01
	max	1.238	31.49
E1	min	1.098	27.93
	max	1.106	28.14
L	min	0.029	0.74
	max	0.041	1.04
B	min	0.009	0.23
	max	0.014	0.36
e	BSC.	0.0256	0.65

Table 3: PQFP/144L Package Dimensions

TQ144 Package Dimensions



Package Dimension Table		TQFP/144L	
		inch	mm
A	max	.063	1.60
A1	min	.002	0.05
	max	.006	0.15
A2	min	.053	1.35
	max	.057	1.45
D	min	.858	21.80
	max	.874	22.20
D1	min	.783	19.90
	max	.791	20.10
E	min	.858	21.80
	max	.874	22.20
E1	min	.783	19.90
	max	.791	20.10
L	min	.018	0.45
	max	.030	0.75
B	min	.007	0.17
	max	.011	0.27
e	BSC.	.0197	0.50

Table 4: TQFP/144L Package Dimensions

Component Availability and Ordering Information

The following table lists the different package options, speed grades and operating temperature ranges that are currently available. Contact I-Cube Marketing for more up-to-date information on product availability.

Device	Speed Grade	Pins	
		144	144
	Package Type:	PQFP	TQFP
	Package Code:	PQ144	TQ144
LS101	NA	C	C

C = Commercial = 0° to +70° C

Figure 3:Current Component Availability