

High Speed CMOS Synchronous 4-Bit Binary Counters

Product Features

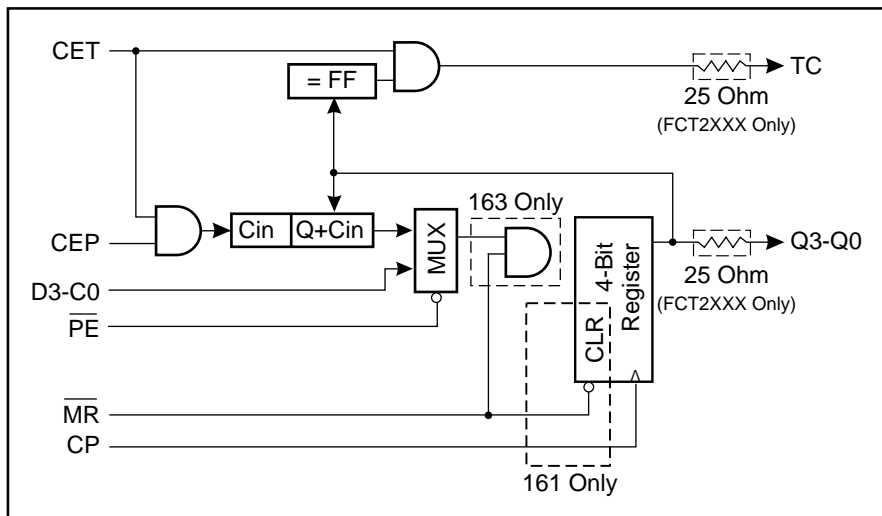
- PI74FCT161/163/2161/2163T are pin-compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs (25Ω series only)
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Packages available:
 - 16-pin 150 mil wide plastic QSOP (Q)
 - 16-pin 150 mil wide plastic SOIC (W)
 - 16-pin 300 mil wide plastic SOIC (S)

Product Description

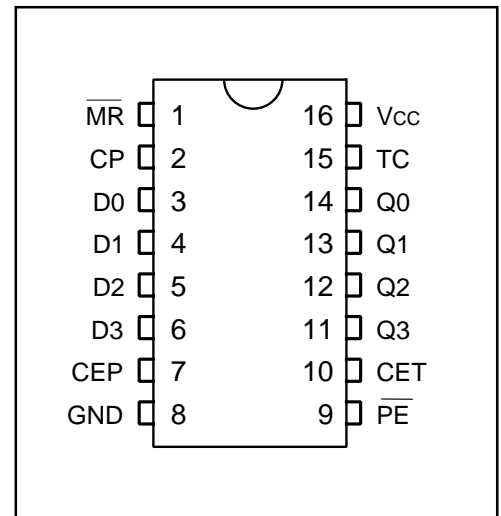
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25Ω series resistor on all outputs to reduce noise owing to reflections, thus eliminating an external terminating resistor.

The PI74FCT161T and PI74FCT163 are high speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear, the 163 has a clocked synchronous clear. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression.

Functional Block Diagram



Pin Configurations



Pin Description

Pin Name	I/O	Description
D3-D0	I	Data Inputs
Q3-Q0	O	Data Outputs
CP	I	Clock
$\overline{\text{MR}}$	I	Master Reset
CEP	I	Counter Enable
CET	I	Count and TC Enable
TC	O	Terminal Count
$\overline{\text{PE}}$	I	Parallel Load Enable

Function Table

Inputs						Outputs			Function
						Q3-Q0			
MR	PE	CP	CEP	CET	DI	161	163	TC	
L	X	X	X	X	X	L		L	Clear 161
L	X	↑	X	X	X		L	L	Clear 163
H	L	↑	X	X	D3-D0	D3-D0	D3-D0	X	Load Data
H	H	↑	H	H	X	Q+1	Q+1	X	Count
H	H	↑	L	X	X	Q	Q	X	Count Inhibit P
H	H	↑	X	L	X	Q	Q	X	Count Inhibit T
H	H	X	X	H	X	F	F	H	Count = 1111
H	H	X	X	H	X	0-E	0-E	L	Count ≠ 1111
H	H	X	X	L	X	X	X	L	TC Inhibit

Notes:

- H = High Voltage Level
 L = Low Voltage Level
 X = Don't Care
 Z = High Impedance
 ↑ = Low to High

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C, V_{CC} = 5.0V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15.0mA	2.4	3.0		V
V _{OL}	Output LOW Current	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48mA		0.3	0.50	V
V _{OL}	Output LOW Current	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12mA (25 Ohm Series)		0.3	0.50	V
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	μA
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	mA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current		V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA			-0.7	-1.2	μA
I _{OFF}	Power Down Disable	V _{CC} = GND., V _{OUT} = 4.5V		-	-	100	μA
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-120		mA
V _H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

Notes:

1. For Max. or Min. conditions, use the appropriate values specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max.	V _{IN} ≥ V _{HC} ; V _{IN} ≥ V _{LC} ;		0.1	500	μA
ΔI _{CCD}	Supply Current per Input @ TTL HIGH	V _{CC} =Max	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} =Max., Outputs Open OE = GND T/R = GND or V _{CC} One Bit Toggling, 50% Duty Cycle	V _{IN} = V _{CC} ; V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} =Max., Outputs Open f _i = 10 MHz, 50% Duty Cycle T/R = OE = GND One Bit Toggling	V _{IN} = V _{CC} ; V _{IN} = GND		2.0	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.3	5.0 ⁽⁵⁾	
		V _{CC} =Max., Outputs Open f _i = 10 MHz, 50% Duty Cycle T/R = OE = GND Eight Bit Toggling	V _{IN} = V _{CC} ; V _{IN} = GND		3.5	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.5	14.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics (Over Operating Range)

Symbol	Description ⁽¹⁾	Conditions	161T, 163T, 2161T, 2163T		161AT, 163AT, 2161AT, 2163AT		161CT, 163CT		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{CPQ}	Propagation Delay CP to Q _I (161/3)	C _L = 50pF R _L = 500 Ohm	2.0	9.5	2.0	6.2	2.0	5.6	ns
t _{CPQ}	Propagation Delay CP to Q _I (2161/3)	C _L = 50pF R _L = 500 Ohm	2.0	9.5	2.0	6.2			ns
t _{MRQ}	Propagation Delay MR to Q _I (161)	C _L = 50pF R _L = 500 Ohm	2.0	13	2.0	8.5	2.0	7.8	ns
t _{MRQ}	Propagation Delay MR to Q _I (2161)	C _L = 50pF R _L = 500 Ohm	2.0	14	2.0	9.1			ns
t _{CPTC}	Propagation Delay CP to TC	C _L = 50pF R _L = 500 Ohm	2.0	15	2.0	9.8	2.0	8.8	ns
t _{CETC}	Propagation Delay CET to TC	C _L = 50pF R _L = 500 Ohm	1.5	8.5	1.5	5.5	1.5	5.0	ns
t _{MRTC}	Propagation Delay MR to TC	C _L = 50pF R _L = 500 Ohm	1.5	11.5	1.5	7.5	1.5	6.8	ns

Notes:

1. Minimums Test Circuit and Waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. PI74FCT2161 is available only by minimum special order.

Timing Characteristics (Over Operating Range)

Symbol	Description	Conditions	161, 163, 2161, 2163		161A, 163A, 2161A ,2163A		161C, 163C, 2161C ,2163C		Units
			Min	Max	Min	Max	Min	Max	
t _S	Data Setup Time D _I to CP	C _L = 50pF R _L = 500 Ohm	5.0		4.0		3.5		ns
t _H	Data Hold Time D _I to CP		1.5		1.5		1.5		
t _{CH}	Count Enab. Setup Time CEP, CET to CP		11.5		9.5		8.5		
t _H	Count Enable Hold Time CEP, CET to CP		0		0		0		
t _{MRS} t _{PES}	Control Setup Time \overline{MR} , \overline{PE} to CP		11.5		9.5		8.5		
t _{MRH} t _{PEH}	Control Hold Time \overline{MR} , \overline{PE} to CP		1.5		1.5		1.5		
t _{CPW}	Clock Pulse Width ⁽¹⁾ HIGH or LOW		5.0		4.0		3.0		
t _{MRW}	\overline{MR} Reset Pulse Width ⁽¹⁾ (161, 2161)		5.0		4.0		3.0		
t _{MRW}	Reset Recovery Time ⁽¹⁾ \overline{MR} to CP, (161,2161)		6.0		5.0		4.0		

Notes:

1. See Test Circuit and Waveforms