1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 10-bit sampling analog-to-digital converter with parallel (AD7580) and byte (AD7579) output formats.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7579S(X)/883B
−2	AD7580S(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Pin LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C, unless otherwise noted)

V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V, V_{DD} +0.3 V
V_{IN}(+)A, V_{IN}(+)B to AGND (Figure 6)	−0.3 V, V_{DD} +0.3 V
V_{IN}(−)A, V_{IN}(−)B to AGND (Figure 6)	−0.3 V, V_{DD} +0.3 V
V_{IN}(+)A, to AGND (Figure 7)	−0.6 V, 2 V_{DD} +0.6 V
V_{IN}(−)A, AGND (Figure 7)	−0.6 V, 2 V_{DD} +0.6 V
V_{IN}(+)A, to AGND (Figure 8)	$-V_{REF}$ −0.6 V, 2 V_{DD} $-V_{REF}$ +0.6 V
V_{IN}(−)A, AGND (Figure 8)	$-V_{REF}$ −0.6 V, 2 V_{DD} $-V_{REF}$ +0.6 V
Digital Input Voltage to DGND	−0.3 V, V_{DD} +0.3 V
Digital Output Voltage to DGND	−0.3 V, V_{DD} +0.3 V
CLK Input Voltage to DGND	−0.3 V, V_{DD} +0.3 V
V_{REF} to AGND	−0.3 V, V_{DD}
Power Dissipation (to +75°C)	450 mW
Derates above +75°C	6 mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 120°C/W for Q-24 and E-28A

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AD7579/AD7580—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2,	10				Minimum Resolution for Which No Missing Codes Are Guaranteed	Bits
Integral Nonlinearity	INL	−1, 2	1	1	1			±LSB max
Differential Nonlinearity	DNL	−1, 2	0.9	0.9	0.9			±LSB max
Full-Scale Error	FSE	−1, 2	5	5	5			±LSB max
Zero Code Error	ZCE	−1, 2	2	2	2		Figure 6	±LSB max
Power Supply Rejection	PSR	−1, 2	0.5					±LSB max
Zero Code Error	ZCE	−1, 2	3	3	3		Figure 7 or Figure 8	±LSB max
Conversion Time	t_{CONV}	−1, 2	16.9	16.9	16.9			µs min
			18.5	18.5	18.5			µs max
Clock Range		−1, 2	250					kHz min
			2.5					MHz max
Signal-to-Noise Ratio	SNR	−1, 2	55	55	55			dB min
Total Harmonic Distortion	THD	−1, 2	−58	−58	−58			dB max
Attenuator Input Resistance		−1, 2	5	5	5			kΩ min
			15	15	15			kΩ max
Comparator Input Resistance		−1, 2	10	10	10		Figure 6	MΩ min
Reference Input Current	I_{REF}	−1, 2	1.5	1.5	1.5			mA max
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V max
Digital Input High Voltage	V_{IH}	−1, 2	2.4	2.4	2.4			V min
Input Current	I_{IN}	−1, 2	10	10	10		V_{IN} = 0 V or V_{DD}	±µA max
Input Capacitance	C_{IN}	−1, 2	10					pF max
Digital Output Low Voltage	V_{OL}	−1, 2	0.4	0.4	0.4		I_{SINK} = 1.6 mA	V max
Digital Output High Voltage	V_{OH}	−1, 2	4.0	4.0	4.0		I_{SOURCE} = 400 µA	V min
Floating State Leakage Current	I_{OUT}	−1, 2	10	10	10		V_{OUT} = 0 to V_{DD}	±µA max
Floating State Output Capacitance	C_{OUT}	−1, 2	10					pF max
Supply Current from V_{DD}	I_{DD}	−1, 2	10	10	10			mA max

NOTE
[1]V_{DD} = +5 V ± 5%, V_{REF} = +2.5 V, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz.

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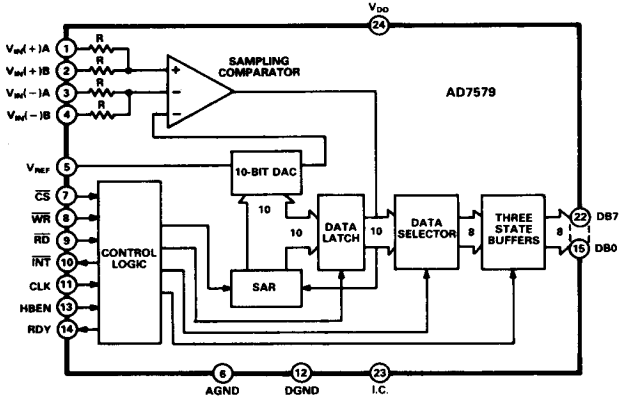
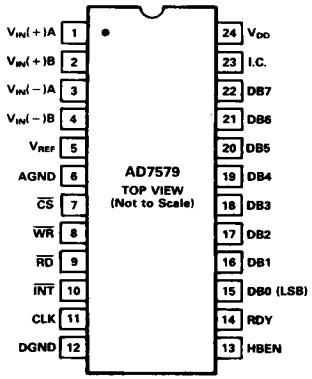
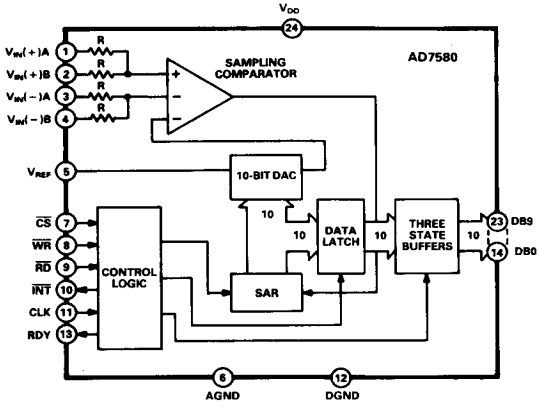
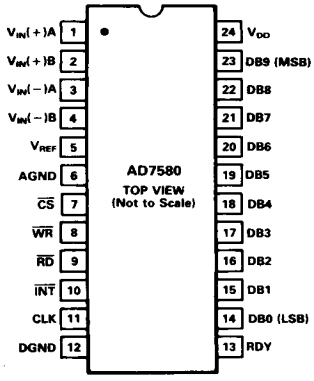
3.2.1 Functional Block Diagram and Terminal Assignments.



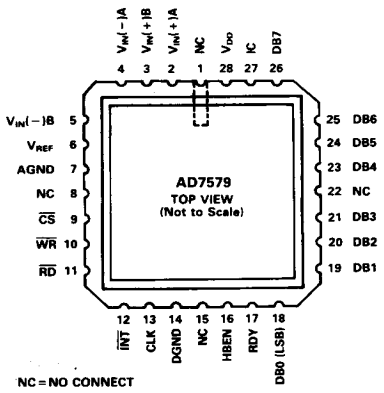
Q Package
(DIP)

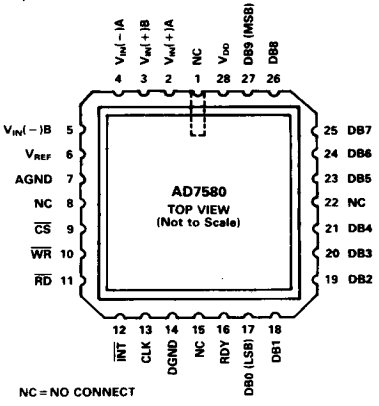






E Package
(LCC)





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3.2.4 Microcircuit Technology Group.

This microcircuit is covered by Technology Group (81).

AD7579/AD7580 TIMING[1]

Test	Symbol[2, 3, 4]	Device	Design Limit T_{min} to T_{max}	Units
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	−1, 2	0	ns min
$\overline{WR}$ Pulse Width	t_2	−1, 2	50	ns min
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_3	−1, 2	0	ns min
$\overline{WD}$ to $\overline{INT}$ Propagation Delay	t_4	−1, 2	120	ns max
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_5	−1, 2	0	ns min
$\overline{RD}$ Pulse Width	t_6	−1, 2	t_{12}	ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_7	−1, 2	0	ns min
HBEN to $\overline{RD}$ Setup Time	t_8	−1, 2	30	ns min
HBEN to $\overline{RD}$ Hold Time	t_9	−1, 2	10	ns min
RDY Access Time	t_{10}	−1, 2	150	ns min
$\overline{RD}$ to $\overline{INT}$ Propagation Delay	t_{11}	−1, 2	120	ns max
Data Access Time After $\overline{RD}$	t_{12}	−1, 2	150	ns max
Data Hold Time, RDY Hold Time	t_{13}	−1, 2	10	ns min
			90	ns max

NOTES

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_4, t_{10}, t_{11} and t_{12} are measured with the load circuits of Figures 3 and 5 and are defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_{13} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 4.

[4]$\overline{INT}$ and RDY are open-drain outputs and need 3 kΩ external pull-up resistors for operation.

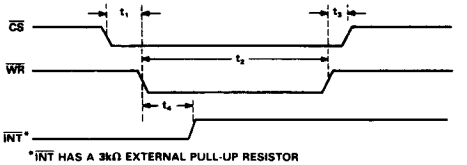


Figure 1. AD7579/AD7580 Start Cycle Timing

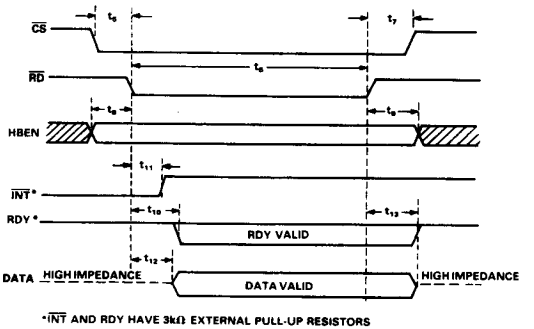
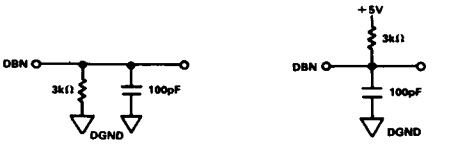
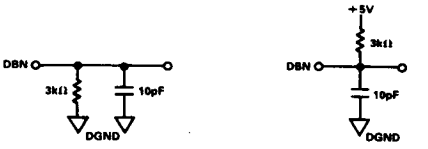


Figure 2. AD7579/AD7580 Read Cycle Timing



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Tests (t_{12})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay (t_{13})

a. High-Z to V_{OL} *b. V_{OL} to High-Z*

Figure 5. Load Circuits for $\overline{INT}$ Propagation Delays

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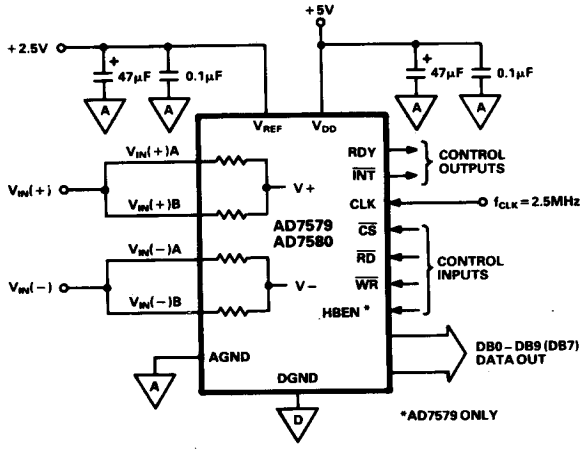
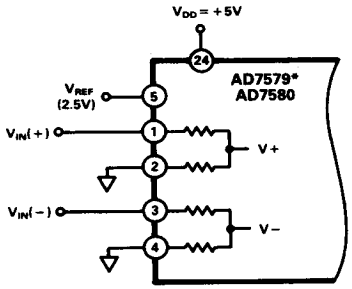


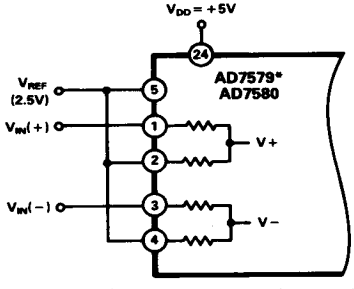
Figure 6. Unipolar 2.5 V Operational Diagram



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

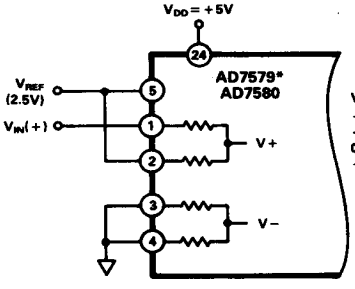
Figure 7. 5 V Span with 0 to 10 V CMR



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

Figure 8. 5 V Span with −2.5 V to +7.5 V CMR



*DECOUPLING CIRCUITRY AND CONTROL CIRCUITRY AS IN FIGURE 10

$V_{IN}(+)$	OUTPUT CODE
−2.500V	00 0000 0000
−2.49512V	00 0000 0001
0.00V	10 0000 0000
+2.49512V	11 1111 1111

Figure 9. Single-Ended Bipolar Operation, −2.5V to +2.5 V

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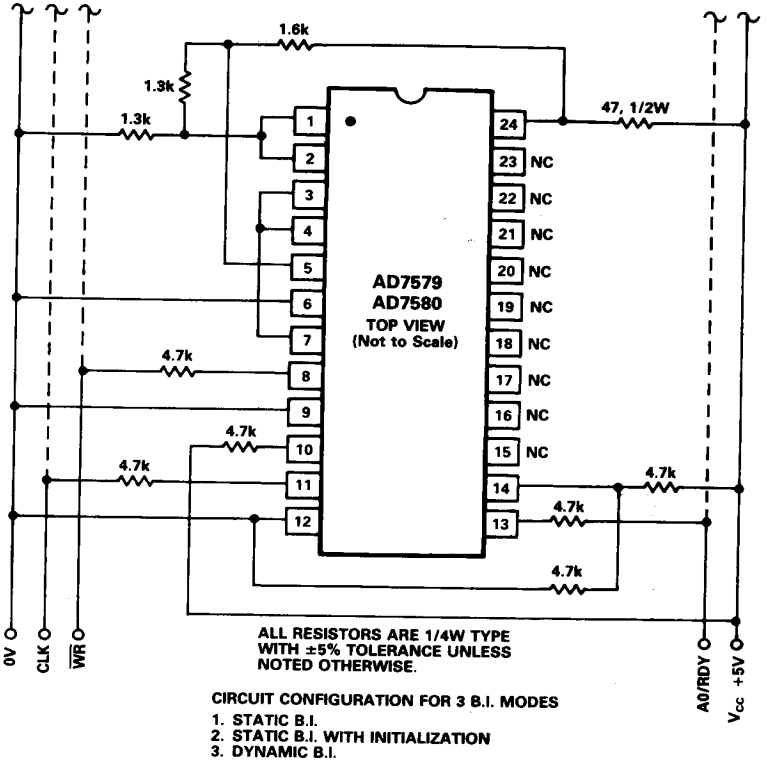
4.2.1 Life Test Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7579/AD7580 signals applied to V_{CC}, CLK $\overline{WR}$, A0/RDY.

1. Static Burn-In

SEQ	V_{CC}	CLK	$\overline{WR}$	A0/RDY
Power-Up	V	0 V	0 V	0 V
Burn-In	5 V	0 V	5 V	0 V

2. Static Burn-In with Initialization

SEQ	V_{CC}	CLK	$\overline{WR}$	A0/RDY
Power-Up Start Conversions Min of 16 CLK-Periods	5 V 5 V	0 V SQR-Wave FREQ = 20 kHz V_{LO} = 0 V V_{HI} = V_{CC}	0 V 0 V	0 V 0 V
	5 V	SQR-Wave	V_{CC}	0 V
Convert Min of 64 CLK Periods	5 V	SQR-Wave	V_{CC}	0 V
Burn-In	5 V	0 V	V_{CC}	0 V

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3. Dynamic Burn-In

SEQ	V_{CC}	CLK	$\overline{WR}$	A0/RDY
Power-Up	5 V	0 V	0 V	0 VC
Burn-In	5 V	SQR-Wave FREQ = 20 kHz V_{LO} = 0 V V_{HI} = V_{CC}	SQR-Wave FREQ = 20/128 kHz V_{LO} = 0 V V_{HI} = V_{CC}	SQR-Wave FREQ = 20/256 kHz V_{LO} = 0 V V_{HI} = V_{CC}

NOTES
$\overline{WR}$ signal = CLK divided by 128, TRIG on rising edge of CLK.
A0/RDY signal = CLK divided by 256 TRIG on rising edge of CLK.

6.0 Differential Applications.

Figure 10 shows the AD7579/AD7580 connected in the standard unipolar mode. Figure 11 and Table 2 show the ideal input/output transfer characteristics and the input/output code table, respectively. Code transitions occur between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The output code is straight binary with 1 LSB = FS/1024 = 2.5/1024 V = 2.4 mV. The input voltage span is 2.5 V and the common mode range is 0 V to + 5 V, when V_{DD} = 5 V. This means that the lowest voltage which can be tolerated at any of the analog inputs is 0 V, and the highest voltage which can be tolerated is +5 V.

Figures 7 and 8 show the input attenuators on the AD7579/AD7580 configured to change the basic range of the device. A 5 V range can be configured by grounding one end of each attenuator and applying the

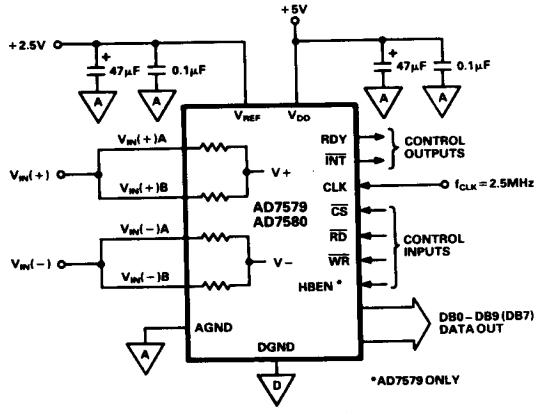

Figure 10. Unipolar 2.5 V Operational Diagram

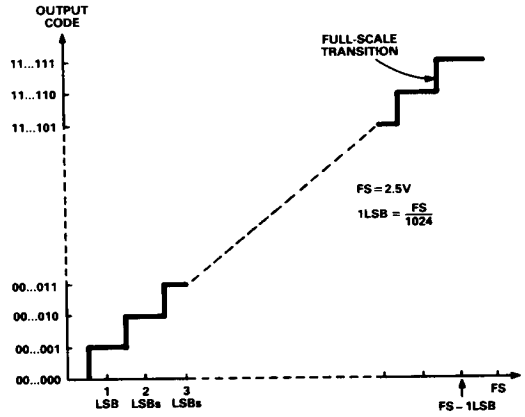

Figure 11. Ideal Input/Output Transfer Characteristics

Table 2. Input/Output Code Table for Figure 10

Differential Analog Input, Volts	Digital Output DB9 DB0
+0.000	00 0000 0000
+0.00244	00 0000 0001
+1.24756	01 1111 1111
+1.25	10 0000 0000
+1.25244	10 0000 0001
+2.49512	11 1111 1110
+2.49756	11 1111 1111

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differential input to the other ends. This is shown in Figure 7. The span is 5 V and the common mode range is 0 to +10 V. In Figure 8, one end of each attenuator is tied to V_{REF} (2.5 V), and this allows each of the other legs to go to −2.5 V without causing the comparator input to go negative. Assuming V_{REF} is 2.5 V, the span of this circuit is 5 V and the common mode range is −2.5 V to +7.5 V. Note that reducing V_{DD} below 5 volts causes a corresponding reduction in CMR. See Specifications page for full details.

6.1 Single-Ended Applications.

In many cases, users of the AD7579/AD7580 will want to measure single-ended input voltages (i.e., ground referred signals). The circuits of Figures 6, 7 and 8 can be easily adapted to accept such signals. If $V_{IN}(-)$ in Figure 6 is tied to AGND, then the analog input range is 0 V to +2.5 V. By connecting $V_{IN}(-)$ of Figure 7 to AGND, the analog input range becomes 0 V to +5 V. Figure 8 can be modified as in Figure 9 to accept input voltages in the range −2.5 V to +2.5 V. Each of these circuits are special cases of the differential input circuits and are achieved by making the negative input to the internal comparator equal to AGND.

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