# Am26L02/96L02

## Low Power Dual Retriggerable Resettable Monostable Multivibrators

**Distinctive Characteristics:**

- One-fourth the power of the equivalent Am2602/9602 dual single shots.
- 50 ns typical propagation delay.
- Fan-out of 3 with standard TTL circuits.
- Guaranteed pulse width variation versus temperature.
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.

### FUNCTIONAL DESCRIPTION

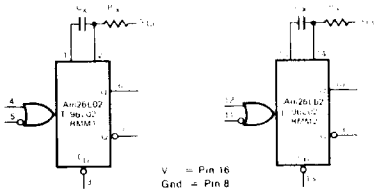
The Am 26L02 and 96L02 are low-power dual DC-level sensitive resettable retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output from the OR trigger gate goes from a FALSE (LOW) to TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

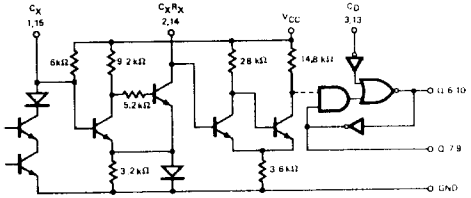
The direct clear facility allows a tuning cycle to be terminated at any time during the cycle. A LOW signal on the $\overline{C}_D$ input resets the monostable independent of other conditions.

The Am26L02 has a guaranteed pulse width variation versus temperature of only 1% over the temperature range 0°C to +75°C

### LOGIC DIAGRAM




### INTERNAL TIMING CIRCUITRY

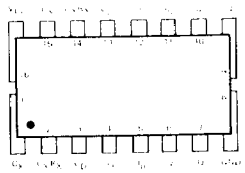



### ORDERING INFORMATION

| Part Number | Package Type | Temperature Range | Order Number |
|---|---|---|---|
| Am26L02 | Molded DIP | 0°C to +75°C | Am26L0259A |
| Am26L02 | Hermetic DIP | 0°C to +75°C | Am26L0259E |
| Am26L02 | Hermetic DIP | −55°C to +125°C | Am26L0251E |
| Am26L02 | Hermetic Flat Pak | −55°C to +125°C | Am26L0251N |
| Am26L02 | Dice | Note | Am26L02XXD |
| Am96L02 | Molded DIP | 0°C to +75°C | U6M96L0259X |
| Am96L02 | Hermetic DIP | 0°C to +75°C | U7B96L0259X |
| Am96L02 | Hermetic DIP | −55°C to +125°C | U7B96L0251X |
| Am96L02 | Hermetic Flat Pak | −55°C to +125°C | U4L96L0251X |
| Am96L02 | Dice | Note | UXX96L02XXD |

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature range.

### CONNECTION DIAGRAM
Top View



**MAXIMUM ...IGS** (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Tempe... ...re | −65°C to +150 |
| Temperature (Ambient) Under Bias | −55°C to +125 |
| Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous | −0.5 V to +7 |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ m |
| DC Input Voltage | −0.5 V to +5.5 |
| Output Current Into Outputs When Output is LOW | 30 r |
| DC Input Current | −30 mA to +5 r |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am96L0256X/26L0256X $T_A$ = 0°C to +75°C $V_{CC}$ = 4.75 V to 5.25 V
Am96L0251X/26L0851X $T_A$ = −55°C to +125°C $V_{CC}$ = 4.50 V to 5.50 V

| Parameters | Description | Test Conditions (Note 1) | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −0.36 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | 2.4 | 3.6 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 4.92 mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 0.15 | 0.3 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | 0.7 | Volts |
| $I_{IL}$ (Note 2) | 93L Unit Load Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.3 V | | −0.25 | −0.4 | mA |
| $I_{IH}$ (Note 2) | 93L Unit Load Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.4 V | | 2.0 | 20 | µA |
| | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5 V | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX., $V_{OUT}$ = 1.0 V | −2.0 | | −13 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | 10 | 16 | mA |

Notes: 1: Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
2: Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

## Switching Characteristics ($T_A$ = 25°C)

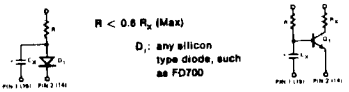
| Parameters | | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{pd+}$ | Turn Off Delay Negative Trigger Input to True Output | Am26/96L0251X | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF<br>$R_X$ = 20 kΩ, $C_X$ = 0 pF | | 55 | 75 | ns |
| | | Am26/96L0259X | | | 55 | 80 | |
| $t_{pd-}$ | Turn On Delay Negative Trigger Input to False Output | | | | 42 | 62 | ns |
| $t_{pw}$ (min) | Minimum True Output Pulse Width | | | | 110 | | ns |
| T | Pulse Width at True Output | | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF<br>$R_X$ = 39 kΩ, $C_X$ = 1000 pF | 12.4 | 13.8 | 15.2 | µs |
| $R_X$ | Timing Resistor (Note 2) | Am26/96L0251X | | 20 | | 200 | kΩ |
| | | Am26/96L0259X | | 16 | | 220 | |
| $t_{pd-}$ ($\overline{C_D}$) | Delay from $\overline{C_D}$ to Q output LOW | | | | 27 | 40 | ns |
| ΔT | Maximum Change in Pulse Width True Output over operating temperature range | Am96L0259X | $V_{CC}$ = 5.0 V, $C_L$ = 15 pF<br>$R_X$ = 39 kΩ, $C_X$ = 1000 pF | 0 | 0.3 | 1.6 | % |
| | | Am96L0251X | | 0 | 1.3 | | |
| | | Am26L0259X | | 0 | 0.3 | 1.0 | |
| | | Am26L0251X | | 0 | 1.0 | 4.0 | |

Notes: 1. Tests are conducted with a 39 kΩ resistor placed between Pin 2 (14) and $V_{CC}$ unless otherwise noted.
2. Maximum permissible $R_x$ when used below 0°C is 100 kΩ.

## OPERATION RULES

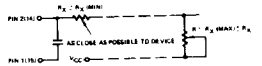
1. An external resistor $R_x$ and an external capacitor $C_x$ are required as shown in the logic diagram. The values of $R_x$ may vary from 20 kΩ to 200 kΩ for 0°C to +75°C operation and 20 kΩ to 100 kΩ for −55°C to +125°C operation. $C_x$ may vary from 0 to any value necessary and obtainable.
2. If a fixed value of $R_x$ is used, the following values are recommended: $R_x$ = 120 kΩ for 0°C to +75°C operation; $R_x$ = 39 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.33\, R_x C_x \left[1 + \frac{3.0}{R_x}\right]$ (For $C_x$ greater than 10³ pF) Where: $R_x$ is in kΩ, $C_x$ is in pF, T is in ns. For $C_x$ < 10³ pF see Fig. 3.
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended.

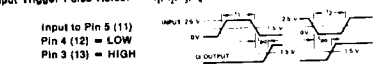



   Both circuits prevent reverse voltage across $C_x$. The pulse width T for the circuits is defined as follows:

   $T \approx 0.30\, RC_x \left[1 + \frac{3.0}{R}\right]$ Where: R is in kΩ, $C_x$ is in pF, T is in ns.
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended.




6. Under any operating condition, $C_x$ and $R_x$ (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 60$ ns.




8. The retriggerable pulse width is calculated as shown below:

   $t_w = t_{pw} + t_{pd+} = 0.33\, R_x C_x \left(1 + \frac{3.0}{R_x}\right) + t_{pd+}$

   The retrigger pulse width is equal to the pulse width $t_{pw}$ plus a delay time.
   For pulse widths greater than 500 ns, $t_w$ can be approximated as $t_{pw}$.

   NOTE: Retriggering will not occur if the retrigger pulse comes within $0.33\, R_x C_x \left(\frac{3.0}{R_x}\right)$ ns after the initial trigger pulse.
9. Reset Operation — The Am26L02/96L02 have an active LOW reset facility. By applying a low to the reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.

## DEFINITION OF TERMS

### SUBSCRIPT TERMS:

**H** HIGH, applying to a HIGH logic level or when used with $V_{CC}$ to indicate high $V_{CC}$ value.

**I** Input.

**L** LOW, applying to LOW logic level or when used with $V_{CC}$ to indicate low $V_{CC}$ value.

**O** Output.

### OPERATIONAL TERMS:

**$I_{IL}$** Forward input load current.

**$I_{OH}$** Output HIGH current, forced out of output in $V_{OH}$ test.

**$I_{OL}$** Output LOW current, forced into the output in $V_{OL}$ test.

**$I_{IH}$** Reverse input load current.

**Negative Current** Current flowing out of the device.

**Positive Current** Current flowing into the device.

**$V_{IH}$** Minimum logic HIGH input voltage. Refer to figure 2.

**$V_{IL}$** Maximum logic LOW input voltage. Refer to figure 2.

**$V_{OH}$** Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

**$V_{OL}$** Maximum logic LOW output voltage with output LOW current $I_{OL}$ into output.

### FUNCTIONAL TERMS:

**$\overline{C}_0$** The asynchronous direct clear input. A LOW on this input resets the monostable independent of other conditions.

**Fan-Out** The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

**$\overline{I}_0$** The active LOW input of the monostables. With input $I_1$ LOW a HIGH to LOW transition on $\overline{I}_0$ will cause triggering.

**$I_1$** The active HIGH input of the monostables. With $\overline{I}_0$ HIGH a LOW to HIGH transition on $I_1$ will cause triggering.

**Input Unit Load** One T²L gate input load.

**Q** The TRUE output of the monostables.

**$\overline{Q}$** The FALSE output of the monostables.

**Triggering** The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

### SWITCHING TERMS:

**$t_{pd+}$** The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the true (Q) output LOW to HIGH transition.

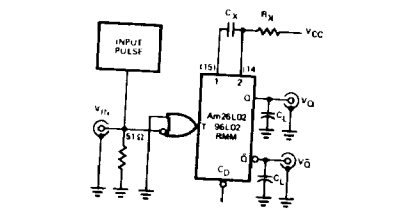
**$t_{pd-}$** The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the false ($\overline{Q}$) output HIGH to LOW transition.

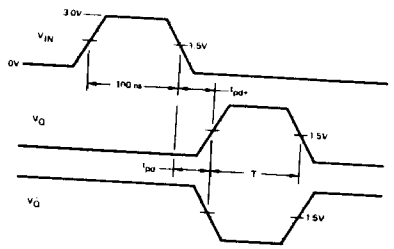
**$t_{pw}$ (min)** The minimum true (Q) output pulse width with $R_x$ = 20 kΩ, $C_x$ = 0 pF.

**T** The pulse width obtained with $R_x$ = 39 kΩ, $C_x$ = 1000 pF.

**ΔT** The maximum percentage change in pulse width of the true (Q) output over the temperature range from the pulse width at 25°C.

## SWITCHI... TIME TEST CIRCUIT AND WAVEFORMS




INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns

Figure 1

## TRUTH TABLE

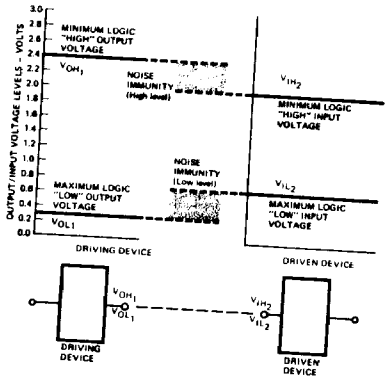
**Am26L02/96L02**
**For Each Monostable**

| $\bar{I}_0$ | $I_1$ | $\bar{C}_D$ | Operation |
|---|---|---|---|
| H→L | L | H | Trigger |
| H | L→H | H | Trigger |
| X | X | L | Reset |

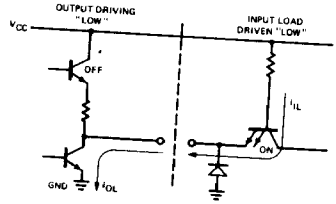
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

## INPUT/OUTPUT INTERFACE CONDITIONS

### Voltage Interface Conditions — LOW & HIGH




### Current Interface Conditions — LOW




### Current Interface Conditions — HIGH

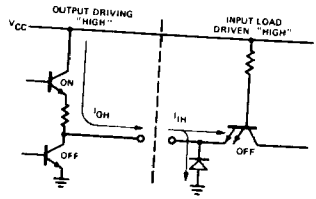



Figure 2

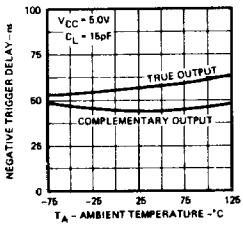
## Am26L02/96L02 LOADING RULES

| Input/Output | Pin No.'s | 93L00 SERIES UNIT LOADS: Input Unit Load | Fanout: Output HIGH | Fanout: Output LOW | 9300 SERIES UNIT LOADS: Input Unit Load: Input HIGH | Input Unit Load: Input LOW | Fanout: Output HIGH | Fanout: Output LOW |
|---|---|---|---|---|---|---|---|---|
| Monostable 1 $C_X$ | 1 | — | — | — | — | — | — | — |
| $C_XR_X$ | 2 | — | — | — | — | — | — | — |
| $\overline{C}_D$ | 3 | 1 | — | — | 0.5 | 0.25 | — | — |
| $I_1$ | 4 | 1 | — | — | 0.5 | 0.25 | — | — |
| $\overline{I}_0$ | 5 | 1 | — | — | 0.5 | 0.25 | — | — |
| Q | 6 | — | 12 | 12 | — | — | 6 | 3 |
| $\overline{Q}$ | 7 | — | 12 | 12 | — | — | 6 | 3 |
| GND | 8 | — | — | — | — | — | — | — |
| Monostable 2 $\overline{Q}$ | 9 | — | 12 | 12 | — | — | 6 | 3 |
| Q | 10 | — | 12 | 12 | — | — | 6 | 3 |
| $\overline{I}_0$ | 11 | 1 | — | — | 0.5 | 0.25 | — | — |
| $I_1$ | 12 | 1 | — | — | 0.5 | 0.25 | — | — |
| $\overline{C}_D$ | 13 | 1 | — | — | 0.5 | 0.25 | — | — |
| $C_XR_X$ | 14 | — | — | — | — | — | — | — |
| $C_X$ | 15 | — | — | — | — | — | — | — |
| $V_{CC}$ | 16 | — | — | — | — | — | — | — |

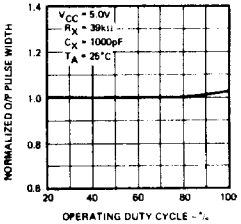
Table I

## Typical Pulse Characteristics

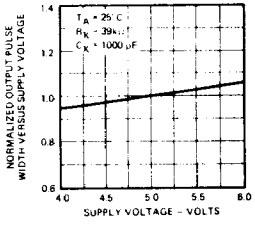
**Negative Trigger Delay Time Versus Ambient Temperature**



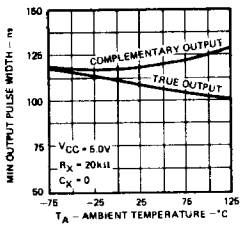

**Normalized Output Pulse Width Versus Operating Duty Cycle**



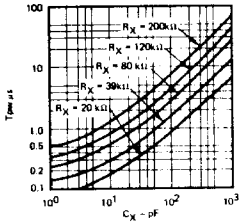

**Normalized Output Pulse Width Versus Supply Voltage**




**Min. Output Pulse Width Versus Ambient Temperature**




**Output Pulse Width T Using Low Values Of $C_x$**




**Normalized Output Pulse Width Versus Ambient Temperature**

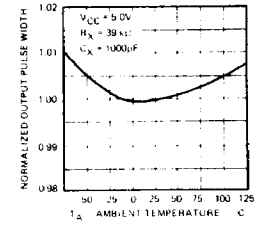
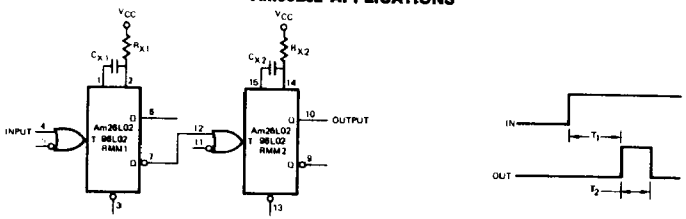



Figure 3

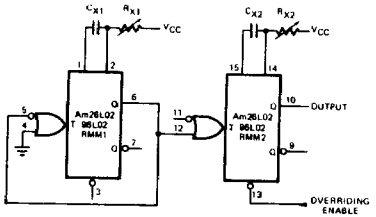
## Am96L02 APPLICATIONS




**Delayed Pulse Generation**

The first monostable determines the time $T_1$ before the initiation of the output pulse. The second monostable determines $T_2$, the output pulse width.

Figure 5




**Pulse Generator**

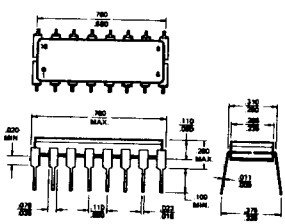
The output frequency produced with the above configuration is determined by $C_{X1}$ and $R_{X1}$, while the pulse width is determined by $C_{X2}$ and $R_{X2}$. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 110 ns, while monostable 2 extends the pulse width to the required value.

Figure 6

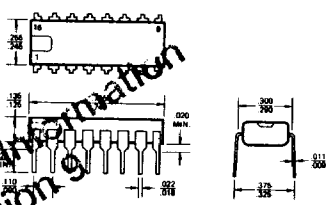
## PHYSICAL DIMENSIONS

**Dual-In-Line**

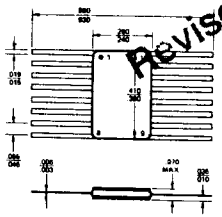
**Hermetic**



**Molded**



**Flat Package**





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MICR
DEVICES IN
901 Thompson Pla
Sunnyva
California 940
(408) 732-24
TWX: 910-339-92
TELEX: 34-63

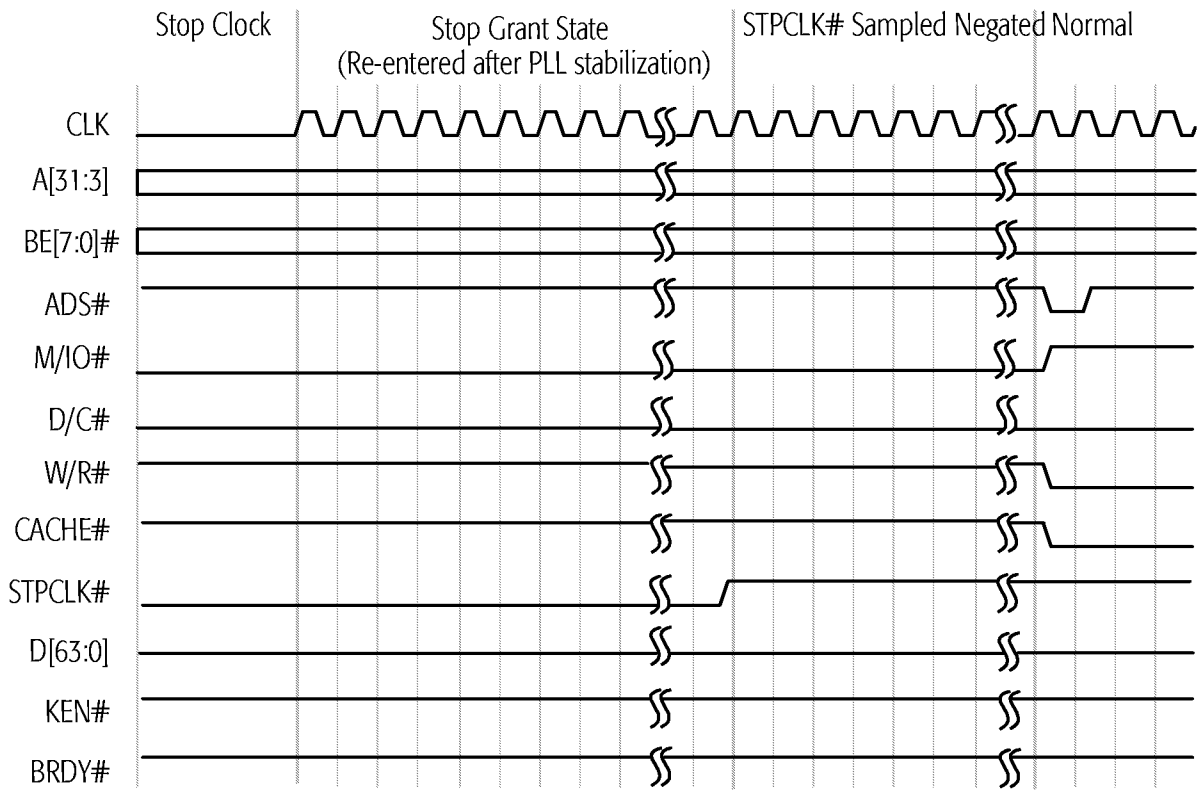


**Figure 75. Stop Grant and Stop Clock Modes, Part 2**

### INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

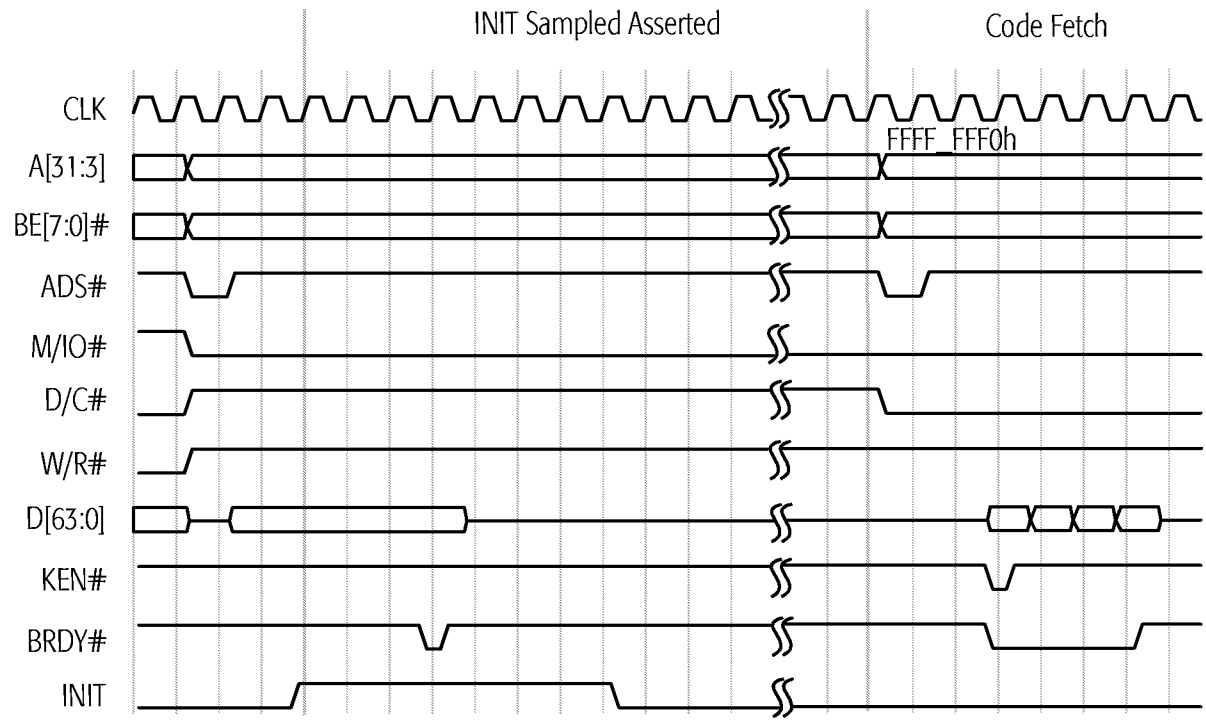


**Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode**

# 6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

## 6.1 Signals Sampled During the Falling Transition of RESET

**FLUSH#** FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

**BF[2:0]** The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

**BRDYC#** BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

## 6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and $V_{CC}$ reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for $V_{CC}$ specifications.)

During a warm reset while CLK and $V_{CC}$ are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

## 6.3 State of Processor After RESET

### Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

**Table 31. Output Signal State After RESET**

| Signal | State | Signal | State |
|---|---|---|---|
| A[31:3], AP | Floating | LOCK# | High |
| ADS#, ADSC# | High | M/IO# | Low |
| APCHK# | High | PCD | Low |
| BE[7:0]# | Floating | PCHK# | High |
| BREQ | Low | PWT | Low |
| CACHE# | High | SCYC | Low |
| D/C# | Low | SMIACT# | High |
| D[63:0], DP[7:0] | Floating | TDO | Floating |
| FERR# | High | VCC2DET | Low |
| HIT# | High | VCC2H/L# | Low |
| HITM# | High | W/R# | Low |
| HLDA | Low | – | – |

### Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.