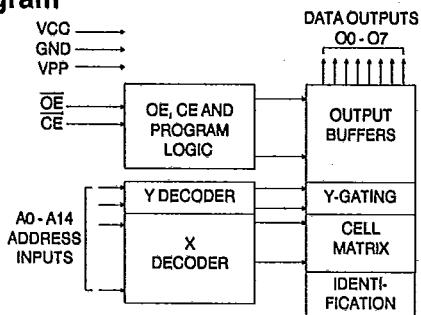


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Features

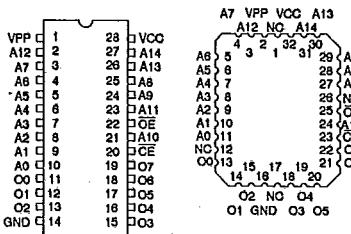
- Bipolar Speed in JEDEC Standard EPROM Pinout
 - Read Access Time - 55ns
 - 28-Lead 800 mil CERDIP and OTP Plastic DIP
 - 32-Pad LCC
 - 32-Lead JLCC and OTP PLCC
- Low Power CMOS Operation
 - 100 μ A max. Standby
 - 75 mA max. Active at 10 MHz
- High Output Drive Capability
- High Reliability Latch-Up Resistant CMOS Technology
- Fast Programming - 4ms/byte (typical)
- Two-Line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

Block Diagram**Description**

The AT27HC256/256L chip family is a high speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. The AT27HC256 is suited for very high speed applications, while the AT27HC256L features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 55ns on the AT27HC256, making this part compatible with high performance systems. Power consumption is typically only 50mA in Active Mode on both parts and less than 10 μ A in Standby on the AT27HC256L. Atmel's 1.5-micron, high speed CMOS technology provides optimum speed, low-power and high noise immunity. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
OE	Chip Enable
OE	Output Enable
NC	No Connect
Q0-Q7	Outputs



Note: PLCC package pins 1 and 17 are DON'T CONNECT.





Description (Continued)

The AT27HC256/256L come in a choice of industry standard JEDEC-approved packages including: 28-pin DIP ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC), or OTP plastic (PLCC) J-leaded chip carrier. The device features two-line control (\overline{CE} , \overline{OE}) to give designers the flexibility to prevent bus contention.

With a storage capacity of 32K bytes, Atmel's 27HC256 / 256L allow firmware to be stored reliably and to be accessed at very high speeds. The AT27HC256/256L have exceptional output drive capability - source 4mA and sink 16mA per output.

The AT27HC256/256L have additional features to ensure high quality and efficient production use. The fast programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC256/256L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using $12,000\text{mJ}/\text{W}\cdot\text{cm}^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15\text{W}\cdot\text{sec}/\text{cm}^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
Integrated UV Erase Dose.....	7258 $\text{W}\cdot\text{sec}/\text{cm}^2$

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC}+0.75\text{V}$ dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	\overline{CE}	\overline{OE}	A1	V _{PP}	V _{CC}	Outputs
Read	V _{IL}	V _{IL}	A1	V _{CC}	V _{CC}	D _{OUT}
Output Disable	V _{IL}	V _{IH}	X ⁽¹⁾	V _{CC}	V _{CC}	High Z
Standby	V _{IH}	X	X	V _{CC}	V _{CC}	High Z
Fast Program ⁽²⁾	V _{IL}	V _{IH}	A1	V _{PP}	V _{CC}	D _{IN}
PGM Verify ⁽²⁾	X	V _{IL}	A1	V _{PP}	V _{CC}	D _{OUT}
Optional PGM Verify ⁽²⁾	V _{IL}	V _{IL}	A1	V _{CC}	V _{CC}	D _{OUT}
PGM Inhibit ⁽²⁾	V _{IH}	V _{IH}	X	V _{PP}	V _{CC}	High Z
Product Identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1-A14 = V _{IL}	V _{CC}	V _{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.

2. Refer to Programming characteristics.

3. V_H = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All A1 inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

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D.C. and A.C. Operating Conditions for Read Operation

		AT27HC256	AT27HC256 / AT27HC256L			
		-55	-70	-90	-12	
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.		-55°C - 125°C ⁽¹⁾	-55°C - 125°C	-55°C - 125°C	
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	

Notes: 1. AT27HC256 only.

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I _L	Input Load Current	V _{IN} = -0.1V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{OUT} = -0.1V to V _{CC} + 0.1V		10	μA
I _{PP} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = 3.8 to V _{CC} + 0.3V		20	μA
I _{SB1} /I _{SB2}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS) CE = V _{CC} -0.3 to V _{CC} +1.0V	AT27HC256L		
		Com. Ind., Mil.	0.1/2 0.2/3		mA
I _{SB2}		I _{SB2} (TTL) CE = 2.0 to V _{CC} +1.0V	AT27HC256		
		Com. Ind., Mil.	40/40 45/45		mA
I _{CC}	V _{CC} Active Current	f = 10MHz, I _{OUT} = 0mA, CE = V _{IL}	Com. Ind., Mil.	75 90	mA
V _{IL}	Input Low Voltage			-0.6	0.8
V _{IH}	Input High Voltage			2.0	V _{CC} + 1
V _{OL}	Output Low Voltage	I _{OL} = 16mA		.45	V
V _{OH}	Output High Voltage	I _{OH} = -100μA	V _{CC} -0.3		V
		I _{OH} = -2.5mA	3.5		V
		I _{OH} = -4.0mA	2.4		V
V _{PP}	V _{PP} Read Voltage	V _{CC} = 5 ± 0.5V		3.8	V _{CC} + 0.3

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

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A.C. Characteristics for Read Operation

Symbol	Parameter	Condition	AT27HC256		AT27HC256 / AT27HC256L				Units
			-55	-70	-90	-12			
t _{ACC} ⁽⁴⁾	Address to Output Delay	CE = OE = V _{IL}	55	70	90		120		ns
		Mil.		70 ⁽¹⁾	90		120		ns
t _{CE} ⁽³⁾	CE to Output Delay	OE = V _{IL}	55	70	90		120		ns
t _{OE} ^(3,4)	OE to Output Delay	CE = V _{IL}	25	30	30		35		ns
t _{DFF} ^(2,5)	OE or CE High to Output Float	CE = V _{IL}	25	30	30		35		ns
t _{OH}	Output Hold from Address, CE or OE, whichever occurred first	CE = OE = V _{IL}	0	0	0		0		ns

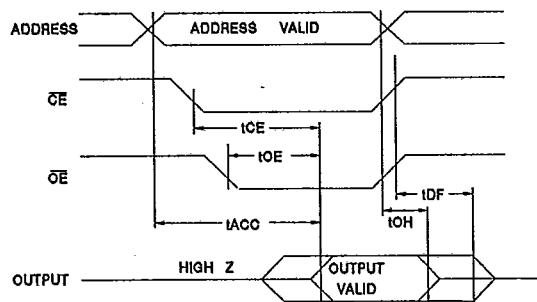
Notes: 1. AT27HC256 only.

2, 3, 4, 5. - see AC Waveforms for Read Operation.





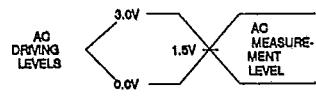
A.C. Waveforms for Read Operation ⁽¹⁾



Notes:

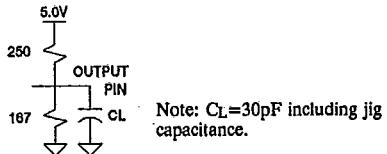
- Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
 $C_L = 30\text{pF}$, add 10ns for $C_L = 100\text{pF}$.
- t_{DP} is specified from \overline{OE} or \overline{CE} , whichever occurs first. t_{DP} is measured at $V_{OH}-0.5\text{V}$ or $V_{OL}+0.5\text{V}$ with $C_L=5\text{pF}$.
- OE may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
- OE may be delayed up to $t_{ACC}-t_{OE}$ after the address is valid without impact on t_{ACC} .
- This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



$t_R, t_F < 5\text{ns}$ (10% to 90%)

Output Test Load



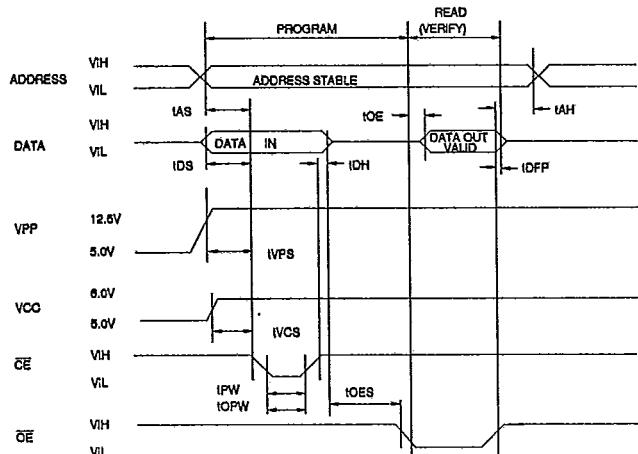
Note: $C_L=30\text{pF}$ including jig capacitance.

Pin Capacitance ($f=1\text{MHz}$ $T=25^\circ\text{C}$) ⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\text{V}$
C_{OUT}	8	12	pF	$V_{OUT} = 0\text{V}$

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms ⁽¹⁾



Notes:

- The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH} .
- t_{OE} and t_{DP} are characteristics of the device but must be accommodated by the programmer.
- When programming the AT27HC256/256L a $0.1\mu\text{F}$ capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

TA=25±5°C, VCC=6.0±0.25V, VPP=12.5±0.5V

Sym- bol	Parameter	Test Conditions	Limits		
		Min	Max	Units	
I _L	Input Load Current	V _{IN} =V _{IL} , V _{IH}	10	μA	
V _{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V _{IH}	Input High Level		2.0	V _{CC} +1	V
V _{OL}	Output Low Volt.	I _{OL} =16mA	.45	V	
V _{OH}	Output High Volt.	I _{OH} =-4.0mA	2.4	V	
I _{CC2}	V _{CC} Supply Current (Program and Verify)		80	mA	
I _{PP2}	V _{PP} Supply Current	CE=V _{IL}	30	mA	
V _{ID}	A9 Product Iden- tification Voltage		11.5	12.5	V

A.C. Programming Characteristics

TA=25±5°C, VCC=6.0±0.25V, VPP=12.5±0.5V

Sym- bol	Parameter	Test Conditions	Limits		
		(see Note 1)	Min	Max	Units
t _{AS}	Address Setup Time		2		μs
t _{OES}	OE Setup Time		2		μs
t _{DS}	Data Setup Time		2		μs
t _{AH}	Address Hold Time		0		μs
t _{DH}	Data Hold Time		2		μs
t _{OPF}	OE High to Out- put Float Delay (Note 2)		0	130	ns
t _{VPS}	V _{PP} Setup Time		2		μs
t _{VCS}	V _{CC} Setup Time		2		μs
t _{PW}	CE Initial Pro- gram Pulse Width (Note 3)		0.95	1.05	ms
t _{OPW}	CE Overprogram Pulse Width (Note 4)		2.85	78.75	ms
t _{OE}	Data Valid from OE		150		ns

*A.C. Conditions of Test:

- 1. Input Rise and Fall Times (10% to 90%) 5ns
- 2. Input Pulse Levels 0.0V to 3.0V
- 3. Input Timing Reference Level 1.5V
- 4. Output Timing Reference Level 1.5V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested.
3. Output Float is defined as the point where data is no longer driven — see timing diagram.
4. Initial Program Pulse width tolerance is 1msec±5%.
5. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

**Atmel's 27HC256/L Integrated
Product Identification Code:**

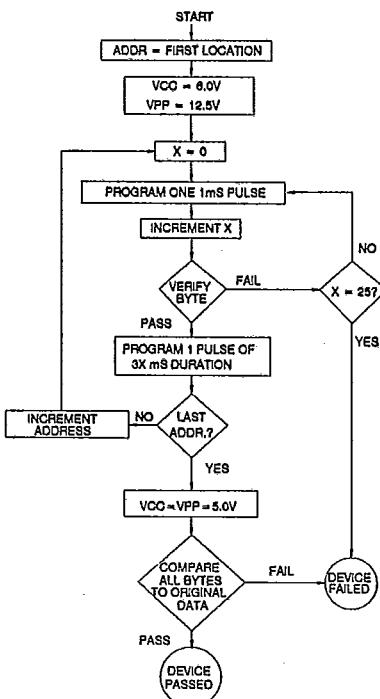
Codes	Pins								Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	
Manufacturer	0	0	0	0	1	1	1	1	1F
Device Type	1	1	0	0	1	0	1	0	94

Fast Programming Algorithm

Two CE pulse widths are used to program; initial and over-program. Ai are set to address the desired byte. V_{CC} is raised to 6.0V. The first CE pulse is 1ms. The programmed byte is then verified. If the byte programmed successfully, then an overprogram CE pulse is applied for 3ms. If the byte fails to program after the first 1ms pulse, then up to 25 successive 1ms pulses are applied with a verification after each pulse. When the byte passes verification, the overprogram pulse width is 3X (times) the number of 1ms pulses required earlier (75ms max).

If the part fails to verify after 25 1ms pulses have been applied, it is considered as failed. After the first byte is programmed, the Ai are set to the next address repeating the algorithm until all required addresses are programmed. Then V_{CC} is lowered to 5.0V. All bytes subsequently are read to compare with the original data to determine if the device passes or fails.

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Ordering Information

ATMEL CORP

29E D

t _{ACC} (ns)	I _{CO} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	75	40	AT27HC256-55DC AT27HC256-55KC AT27HC256-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	90	45	AT27HC256-55DI AT27HC256-55KI AT27HC256-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	75	40	AT27HC256-70DC AT27HC256-70JC AT27HC256-70KC AT27HC256-70LC AT27HC256-70PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
70	90	45	AT27HC256-70DI AT27HC256-70JI AT27HC256-70KI AT27HC256-70LI AT27HC256-70PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256-70DM AT27HC256-70KM AT27HC256-70LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256-70DM/883 AT27HC256-70KM/883 AT27HC256-70LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	75	40	AT27HC256-90DC AT27HC256-90JC AT27HC256-90KC AT27HC256-90LC AT27HC256-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	90	45	AT27HC256-90DI AT27HC256-90JI AT27HC256-90KI AT27HC256-90LI AT27HC256-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256-90DM AT27HC256-90KM AT27HC256-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256-90DM/883 AT27HC256-90KM/883 AT27HC256-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	75	40	AT27HC256-12DC AT27HC256-12JC AT27HC256-12KC AT27HC256-12LC AT27HC256-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)

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Ordering Information

t _{ACO} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	90	45	AT27HC256-12DI	28DW6	Industrial (-40°C to 85°C)
			AT27HC256-12JI	32J	
			AT27HC256-12KI	32KW	
70	90	45	AT27HC256-12LI	32LW	Military (-55°C to 125°C)
			AT27HC256-12PI	28P6	
			AT27HC256-12DM	28DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	90	45	AT27HC256-12KM	32KW	
			AT27HC256-12LM	32LW	
			AT27HC256-12DM/883	28DW6	
70	90	45	AT27HC256-12KM/883	32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT27HC256-12LM/883	32LW	
			5962-86063 08 XX	28DW6	
70	90	45	5962-86063 08 YX	32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type

28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)





Ordering Information

ATMEL CORP

29E D

t _{ACC} (ns)	I _{cc} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	75	0.1	AT27HC256L-70DC AT27HC256L-70KC AT27HC256L-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	90	0.2	AT27HC256L-70DI AT27HC256L-70KI AT27HC256L-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
90	75	0.1	AT27HC256L-90DC AT27HC256L-90JC AT27HC256L-90KC AT27HC256L-90LC AT27HC256L-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	90	0.2	AT27HC256L-90DI AT27HC256L-90JI AT27HC256L-90KI AT27HC256L-90LI AT27HC256L-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256L-90DM AT27HC256L-90KM AT27HC256L-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256L-90DM/883 AT27HC256L-90KM/883 AT27HC256L-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	75	0.1	AT27HC256L-12DC AT27HC256L-12JC AT27HC256L-12KC AT27HC256L-12LC AT27HC256L-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
120	90	0.2	AT27HC256L-12DI AT27HC256L-12JI AT27HC256L-12KI AT27HC256L-12LI AT27HC256L-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256L-12DM AT27HC256L-12KM AT27HC256L-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256L-12DM/883 AT27HC256L-12KM/883 AT27HC256L-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	0.2	5962-86063 07 XX 5962-86063 07 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	90	0.2	5962-86063 06 XX 5962-86063 06 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Ordering Information

Package Type	
28DW8	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P8	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

4



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