gazelle

GA23SV8/GA23S8

High-Performance Logic Device
Gallium Arsenide

T-46-13-47

General Description

Gazelle's GA23SV8/GA23S8 are TTL-compatible high-performance logic sequencers. Based on the familiar programmable array logic architecture, they provide highest performance and maximum flexibility in a 20-pin package. They are user-configurable to satisfy specific applications.

The GA23SV8/GA23S8 provide twenty-three array inputs, eight outputs, and six Buried Registers (BRs). Nine of the inputs are direct from dedicated inputs, six from BRs, and eight from bidirectional output structures. The GA23SV8 features eight Output Logic Macrocells (OLMs), which can be configured as "registered" or "combinatorial" and active-HIGH or active-LOW. The OLMs also allow for bidirectional operation at the output pins. The GA23S8 contains four OLMs and four output registers.

In addition to the eight output registers, the GA23SV8/GA23S8 feature six buried registers. They allow high-speed feedback (166 MHz) to the AND-OR array without sacrificing I/O pins. This powerful combination of I/O economy, fourteen on-chip registers, and 166 MHz capability makes these devices ideal for high-speed sequencer and control applications. Because the buried registers are also accessible at the output pins, the devices are easy to design with and convenient to debug.

For even greater design flexibility, the GA23SV8/GA23S8 feature programmable product terms for synchronous PRESET and asynchronous RESET. Additionally, all fourteen registers may be PRELOADed, creating a broad range of test capabilities.

The GA23SV8/GA23S8 are fabricated using Gazelle's One-Up™ gallium arsenide technology to achieve both superior performance and full TTL compatibility. This makes it a natural companion to CMOS gate arrays and all popular microprocessors, including the 80386, 80486, 68030, 68040, and RISC processors, as well as those designed for controller applications.

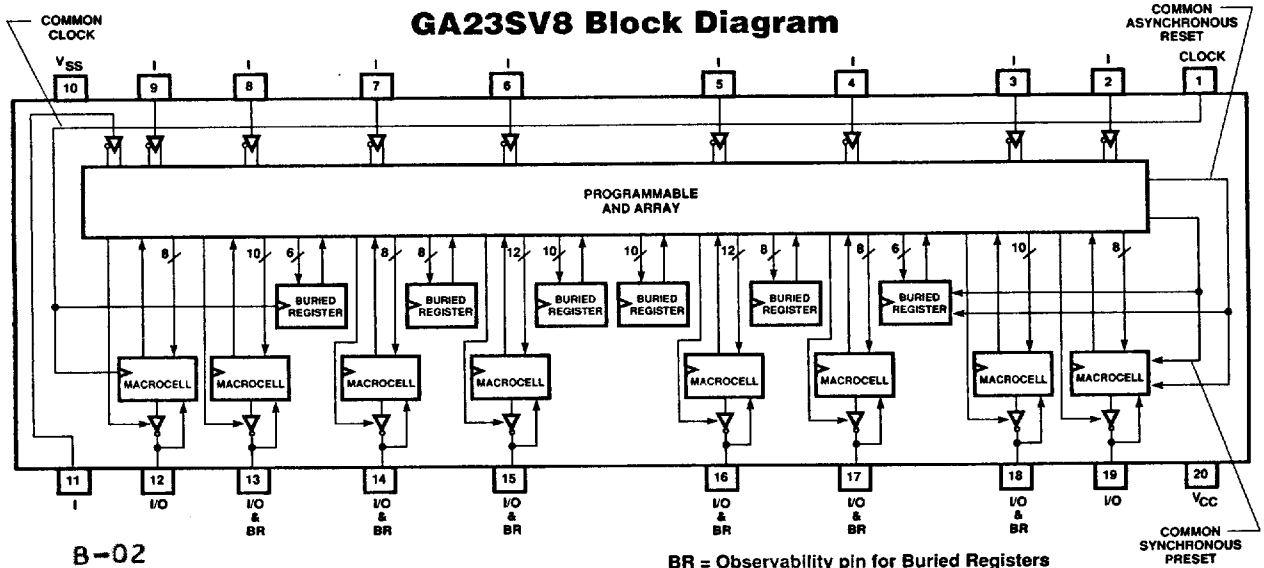
These devices are factory configured by Gazelle's Quick-Turn™ laser technology and are tested for 100% functional and parametric compliance, over temperature and voltage, AFTER programming.

Features

Commercial	t_{PD}	t_S	f_{MAX1}	f_{MAX2}
GA23SV8/GA23S8	7.5 ns	4 ns	95 MHz	166 MHz
GA23SV8/GA23S8	10 ns	4.5 ns	83 MHz	153 MHz
Military				
GA23SV8/GA23S8	12 ns	6.5 ns	62 MHz	105 MHz

- World's Fastest Sequencer
- 166 MHz clock capability yields 6 ns resolution for controlling output timing
- 4 ns setup time (t_S) allows for immediate response to required changes in system timing sequences
- Architecture similar to popular 22V10
  - — Up to 12 product terms per output
  - — 135 total product terms; twice the number of any high-speed 20-pin PLD
- 14 registered bits of state
- 6 "buried" registers allow for internal state machine logic without sacrificing I/O pins
- 8 full-feature Output Logic Macrocells (OLMs) on GA23SV8 allow for total flexibility of output signal generation
- Fully functional and pin compatible with silicon 23S8s
- Advanced I/O structure
  - — Up to 23 array inputs
  - — Up to 17 pin inputs
  - — Up to 8 outputs
- Individually configurable Output Enable product terms with polarity control
- Quick-Turn factory laser programming
- 100% functional and parametric testing AFTER programming
- Packaging
  - — 20-pin ceramic side-brazed DIP
  - — 28-pin ceramic J-Leaded Chip Carrier

GA23SV8 Block Diagram



BR = Observability pin for Buried Registers

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Functional Description

The GA23SV8/GA23S8 are high-performance user-configurable sequencers. Based on the familiar sum-of-products (AND-OR) array structure, they can be specified by the user to satisfy specific applications.

The GA23S8 consists of twenty-three array inputs, eight outputs, and six Buried Registers. The twenty-three array inputs are comprised of nine dedicated inputs and fourteen feedback inputs from the outputs and buried registers. These twenty-three array inputs are connected to a configurable AND array containing 135 product terms. The outputs of the AND gates are connected to fixed OR gates. The eight outputs consist of four registered outputs and four OLMs.

The GA23SV8 is an enhanced version of the popular 23S8 architecture. It expands on the 23S8 by adding full output flexibility. All eight of the outputs of the GA23SV8 are Output Logic Macrocells (OLMs). This allows any and all output pins to be configured as registered or combinatorial, active-HIGH or active-LOW, and registered feedback or I/O (off-chip) feedback.

These devices are ideal for complex, very high speed, state machine, sequencer, and controller applications. The fourteen bits of information in on-chip registers allow for 16,384 possible states.

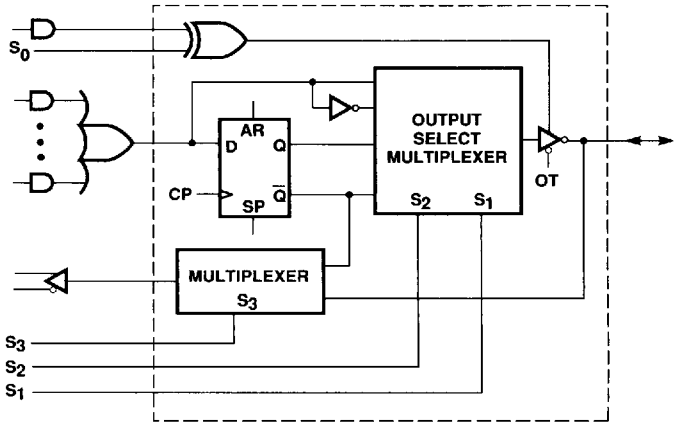
Variable Product Term Distribution

The number of AND gates assigned to an OR gate varies as shown in Figure 3. The number varies from eight to twelve AND gates. This facilitates the implementation of up to twelve product term logical functions in a single clock cycle, even without the feedback activated. For Buried Registers, the number of associated AND gates varies from six to ten. The variable product term distribution allows for easy implementation of varying complexity logical functions.

Output Logic Macrocells (OLMs)

The Output Logic Macrocells (OLMs) provide the capability to individually define the architecture of each output. As shown in Figure 1, each OLM contains four programming inputs: S_0, S_1, S_2, and S_3. The S_0 programming input specifies the polarity of the Output Enable (OE) signal for the individual output as shown. Depending on the configuration of the S_1, S_2, and S_3 programming inputs, an individual output will operate in one of eight modes outlined in Figure 1. The resulting increase in I/O configuration flexibility enables the designer to optimize the device for precise application requirements. Figures 2a through 2h show all eight possible configurations of the OLM outlined in Figure 1.

Output Logic Macrocell



CP = CLOCK INPUT
AR = ASYNCHRONOUS RESET
SP = SYNCHRONOUS PRESET
OT = OBSERVABILITY TERM

Figure 1

Output Enable Polarity Configuration

S_0	OUTPUT ENABLE POLARITY
0	Enabled HIGH
1	Enabled LOW

Configuration Table

S_1	S_2	S_3	FEEDBACK	OUTPUT CONFIGURATION	ACTIVE
0	0	0	Register	Registered	LOW
0	0	1	I/O	Registered	LOW
0	1	0	Register	Combinatorial	LOW
0	1	1	I/O	Combinatorial	LOW
1	0	0	Register	Registered	HIGH
1	0	1	I/O	Registered	HIGH
1	1	0	Register	Combinatorial	HIGH
1	1	1	I/O	Combinatorial	HIGH

Note: 0 = unblown fuse, 1 = blown fuse.

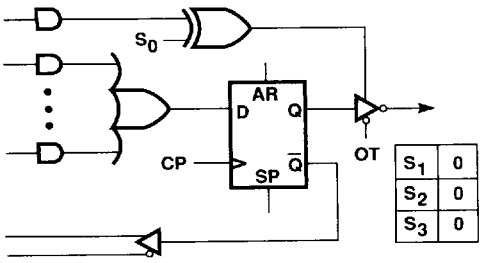


Figure 2a. Registered Feedback, Registered Output, Active-LOW Output

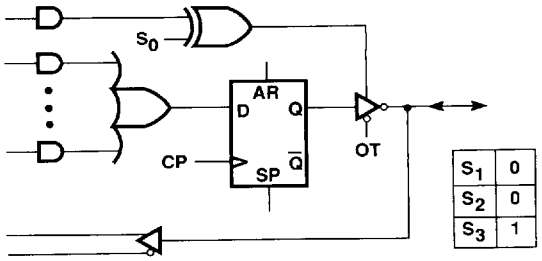


Figure 2b. I/O Feedback, Registered Output, Active-LOW Output

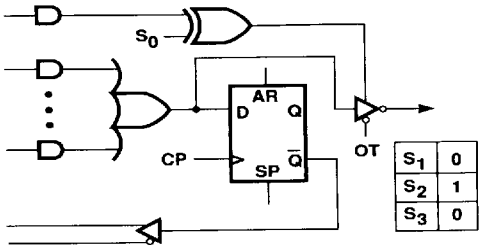


Figure 2c. Registered Feedback, Combinatorial Output, Active-LOW Output

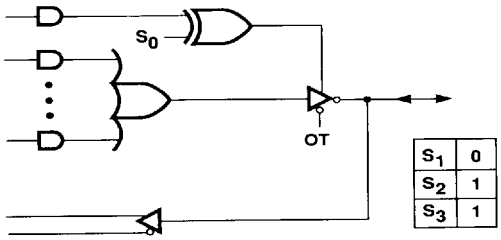


Figure 2d. I/O Feedback, Combinatorial Output, Active-LOW Output

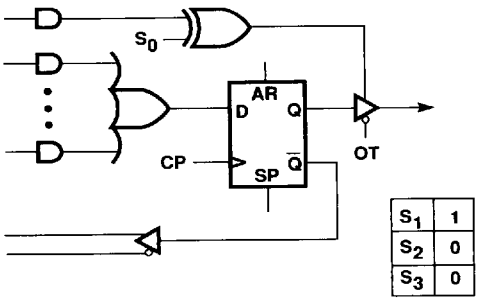


Figure 2e. Registered Feedback, Registered Output, Active-HIGH Output

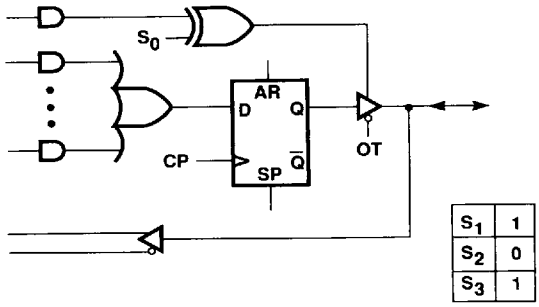


Figure 2f. I/O Feedback, Registered Output, Active-HIGH Output

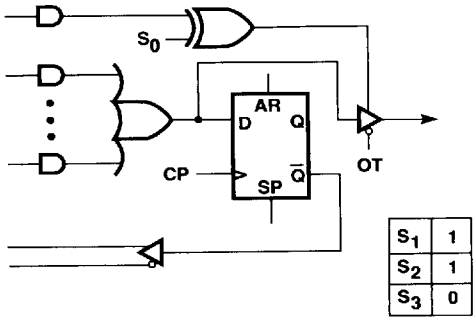


Figure 2g. Registered Feedback, Combinatorial Output, Active-HIGH Output

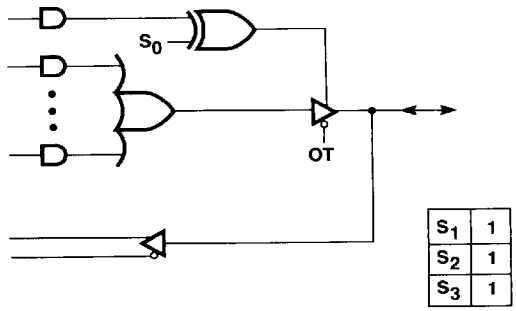


Figure 2h. I/O Feedback, Combinatorial Output, Active-HIGH Output

Figure 2.

Functional Logic Diagram GA23SV8/GA23S8 (Note 1)

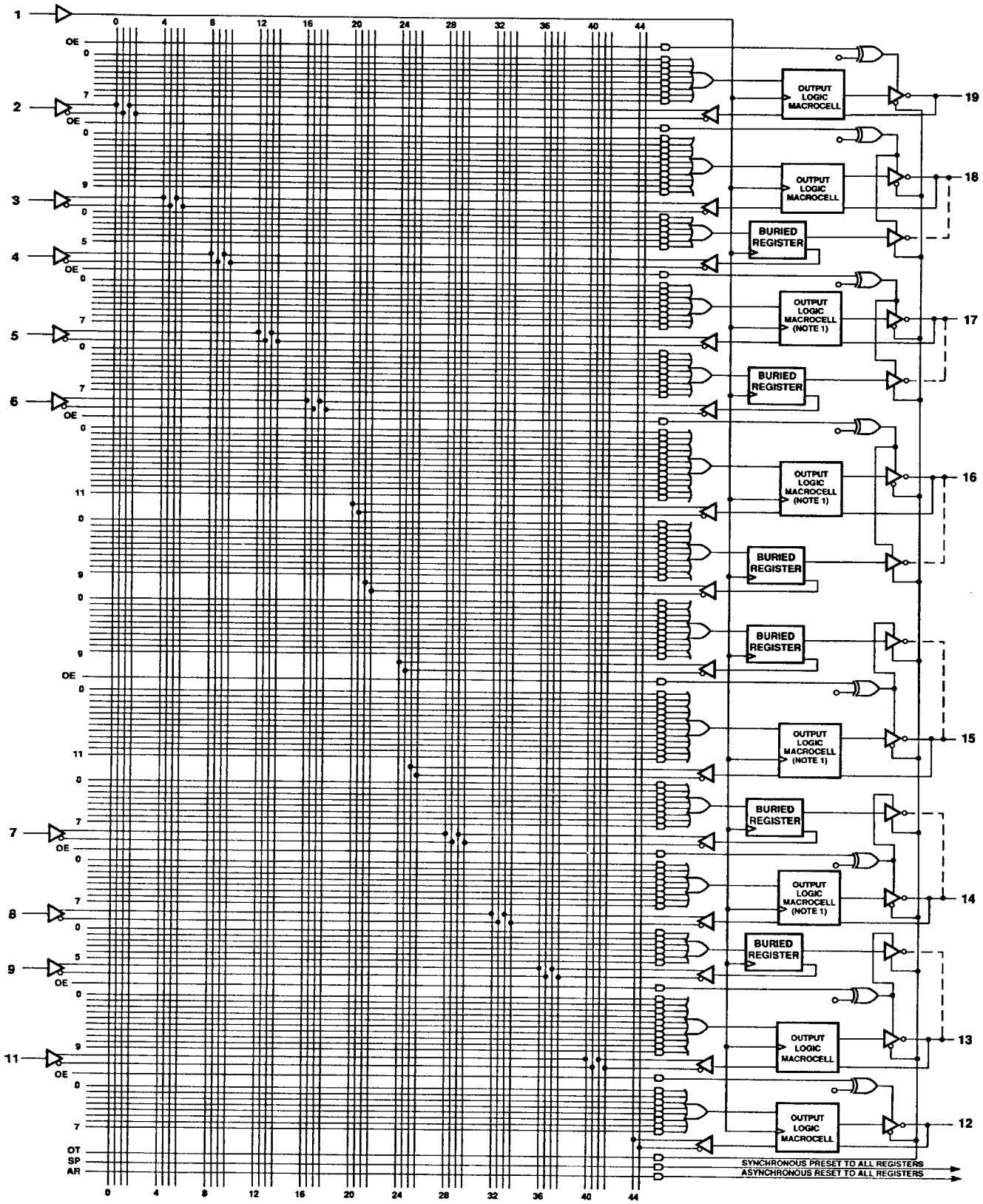


Figure 3.

Note 1: Pins 14, 15, 16, and 17 are Output Registers rather than Macrocells on the GA23S8. Pinout shown is for DIPs only.

Output Registers

On the GA23S8, four of the of eight outputs (pins 14, 15, 16, and 17) contain output registers with individual configurable OE polarity control, S_0. Also, the output of the register can be configured as active-HIGH or active-LOW with the use of the S_1 programmable input. The data on the output register can be fed back to the array, or when the output is disabled, the pin may be used as an external input into the array. Figure 4 shows the output register with configurable OE and active output polarity controls.

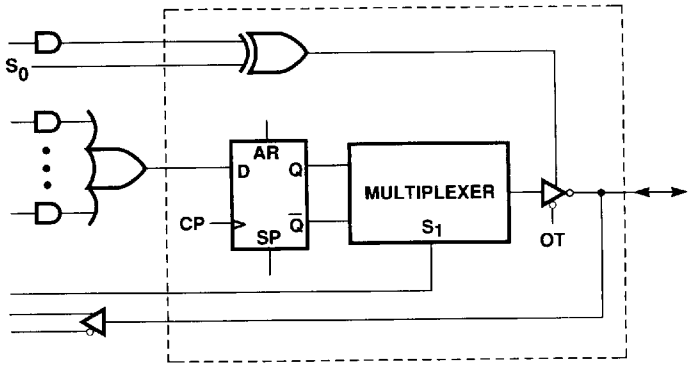


Figure 4. Output register

S_0	OUTPUT ENABLE POLARITY
0	Enabled HIGH
1	Enabled LOW

S_1	OUTPUT CONFIGURATION
0	Active LOW
1	Active HIGH

Programmable Output Polarity

To further enhance the flexibility of the device, each output has a programmable input which specifies the polarity of the active state. By providing this option, the user no longer has the need to DeMorganize equations to fit a device. This option increases both the efficiency of the design time as well as device utilization. Also, each output has an individual OE control signal which can be specified to either polarity active state.

Buried Registers

The key architectural optimization to create a more efficient state machine out of a generic PLD structure is the buried registers. By offering registers which are directly fed back to the AND array without having to drive or use up outputs, the GA23SV8/GA23S8 sequencers enjoy increased performance as well as more effective I/O utilization. To increase testability, each buried register can be accessed, via a user-configurable observability product term (OT), through an associated output. Figure 5 shows the details of the buried register.

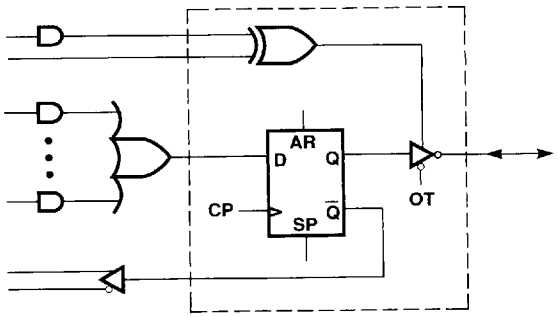


Figure 5. Buried register

Synchronous PRESET and Asynchronous RESET

For added ease of use, both devices have a Synchronous PRESET and Asynchronous RESET which control all registers. Useful, especially in system power-up or reset procedures, these inputs allow complete control of the device by the system. When the Synchronous PRESET is asserted (HIGH), all registers are loaded with a logical "1" on the next LOW-to-HIGH clock transition. Activating the Asynchronous RESET signal (HIGH) will reset all registers to a logical "0" level immediately, independent of the clock.

Observability

The Observability feature allows access to the buried registers. When the observability product term (OT) is selected, it disables the Output Registers and Macrocell buffers, and enables the buried registers buffers onto the output pins associated with them, pins 13 through 18. When the observability product term is not selected, the Output Registers and Macrocell buffers are enabled and the buried registers buffers are disabled. When observability product term is not selected, the data from the buried registers will not be visible on the output pins.

Preload

Testing of state machines is a difficult task unless there are ways to force the registers to desired states for functional verification of the logic after the feedback. To address this concern, the GA23SV8/GA23S8 offer the PRELOAD function in which all registers, including buried registers, can be preloaded from external pins. OLM and output registers are loaded in a separate cycle from the buried registers, since buried registers share an output pin with them.

By using the PRELOAD procedures, desired "present state" values can be loaded into the registers to perform logic verification sequences. This ability significantly shortens the verification procedures, allowing the user to test all possible state sequences without substantial penalties in testing time and costs.

Output Register and Buried Register Preload

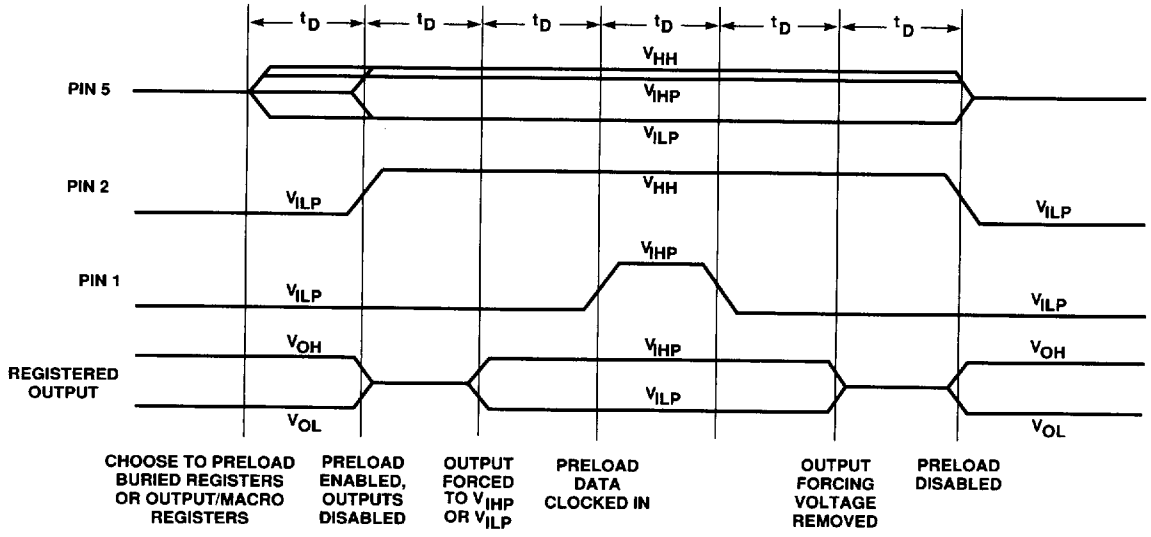
The output registers and buried registers are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. The output registers and buried registers are loaded independently to allow different values to be loaded into each set. This feature will simplify testing since any state can be loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below.

LEVEL FORCED ON REGISTERED OUTPUT PIN DURING PRELOAD CYCLE	REGISTER Q OUTPUT STATE AFTER CYCLE
V_{IHP}	HIGH
V_{ILP}	LOW

Preload Parameters (T_A = 25°C)

SYMBOL	PARAMETER DESCRIPTION	MIN	MAX	UNIT
V_{HH}	Control pin extra HIGH level	10	12	V
V_{IHP}	Input HIGH level during preload	2.4	5.5	V
V_{ILP}	Input LOW level during preload	0.0	0.5	V
t_D	Delays between various level changes	100	15,000	ns



REGISTER SELECTION	PIN 5
Buried	V_{HH}
Output/Macro	≤ V_{IHP}

Absolute Maximum Ratings beyond which the useful life of the device may be impaired

Storage temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +125°C
Supply voltage to ground potential (Pin 20 to Pin 10)	-0.5 V to +7.0 V
DC voltage applied to outputs in high Z state	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V_{CC}+0.5 V)
DC input current	-30 mA to +5 mA
DC voltage applied during preload	12.0 V

Operating Range

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +75°C	5 V ± 5%
Military*	-55°C to +125°C	5 V ±10%

*Maximum operating case temperature +125°C

Operating range defines those limits between which the functionality of the device is guaranteed.

DC Characteristics Over operating range unless otherwise specified

SYMBOL	DESCRIPTION	TEST CONDITIONS	LIMITS[1] MIN	TYP	MAX	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}, I_{OH} = -3.2 mA	2.4	3.2		V
V_{OL}	Output LOW voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}, I_{OL} = 16 mA		0.3	0.5	V
V_{IH}[2]	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}[2]	Input LOW level	Guaranteed input logical LOW voltage for all inputs			0.8	V
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.40 V		-150	-400	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7 V			25	µA
I_I	Input HIGH current	V_{CC} = Max, V_{IN} = 5.5 V			1	mA
I_{SC}[3]	Output short-circuit current	V_{CC} = Max, V_{OUT} = 0.5 V	-30	-60	-120	mA
I_{CC}	Power supply current	V_{CC} = Max		180	220	mA
V_I	Input clamp voltage	V_{CC} = Min, I_{IN} = -18mA			-1.2	V
I_{OZH}[4]	Output leakage current HIGH	V_{CC} = Max, V_{IH} = 2.0 V, V_{IL} = 0.8 V, V_{OUT} = 2.7 V			100	µA
I_{OZL}[4]	Output leakage current LOW	V_{CC} = Max, V_{IH} = 2.0 V, V_{IL} = 0.8 V, V_{OUT} = 0.4 V			-100	µA

Capacitance[5]

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz		6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz		9		pF

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second. V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_X (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

Switching Characteristics

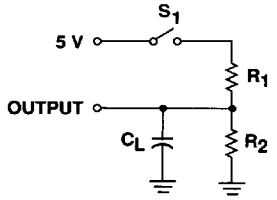
SYMBOL	DESCRIPTION		COMMERCIAL -7 MIN	COMMERCIAL -7 MAX	COMMERCIAL -10 MIN	COMMERCIAL -10 MAX	MILITARY -12 MIN	MILITARY -12 MAX	UNIT
t_{PD}	Input or feedback to non-registered output		3	7.5	3	10	3	12	ns
t_S	Input or feedback setup time		4		4.5		6.5		ns
t_{CO1}	Clock to output		3	6.5	3	7.5	3	9.5	ns
f_{MAX}	Maximum frequency[4]	External	95		83		62		MHz
		Internal[3]	166		153		105		
t_{CO2}	Registered feedback through array to combinational output, relative to external clock			10.5		12		18	ns
t_{CF}	Clock to feedback[5]			2		2		3	ns
t_{EA}	Input to output enable		3	7.5	3	10	3	12	ns
t_{ER}	Input to output disable		3	7.5	3	10	3	12	ns
t_H	Hold time		0		0		0		ns
t_W	Clock width (LOW or HIGH)		3		3		3		ns
t_{AW}	Asynchronous reset width		7.5		10		12		ns
t_{AR}	Asynchronous reset recovery time		4		6		7		ns
t_{AP}	Asynchronous reset to registered output reset			9		12		14	ns

The highlighted specifications represent substantial performance improvements over other state machine and sequencer products.

Notes: 1. t_{PD} is tested with switch S_1 closed and C_L = 50 pF

2. Output enable times are tested with C_L = 50 pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} -0.5 V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.
3. The internal maximum frequency is limited by the quality of the clock input signal.
4. These parameters are not 100% tested but are calculated at initial characterization, and at any time the design is modified where frequency may be affected.
5. Calculated from measured f_{MAX} internal.

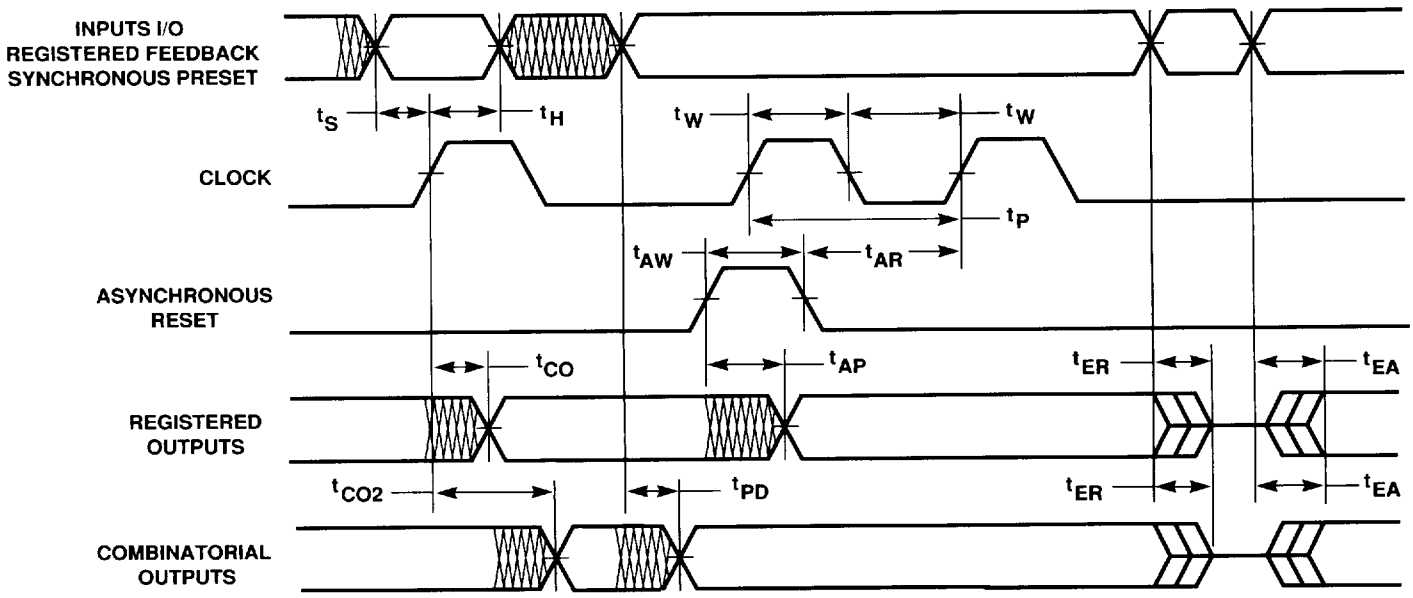
Switching Test Circuit



Test Conditions

	COMMERCIAL	MILITARY	UNIT
R_1	300	390	Ω
R_2	390	750	Ω
C_L	50	50	pF

Switching Waveform



Design-Aid Software

Design-Aid software tools are commercially available to assist with the design-in of Gazelle's GA23SV8/GA23S8. The packages mentioned in the table below operate on multiple hardware platforms and provide different levels of design integration. The main function of the design-aid software is to translate custom logic design specifications into a JEDEC programming file. These software packages are capable of accepting many types of design entry including: net lists, state diagrams, Boolean equations and truth tables. These packages are also capable of providing many types of logic functions such as simulation, logic minimization, and automatic test vector generation. The final output is a JEDEC file. Gazelle's GA23SV8/GA23S8 are capable of accepting any industry-standard JEDEC file regardless of the manufacturer it was created for.

Please contact Gazelle with any questions pertaining to compatibility.

Design-Aid Software for GA23SV8/GA23S8

SOFTWARE VENDOR	SOFTWARE PACKAGE	HARDWARE PLATFORM
Data I/O Corp. 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Rev 3.0 – GA23S8 Rev 3.2 – GA23SV8	IBM PC™ or compatible DEC VAX (VMS, UNIX) Apollo (Aegis) Sun Microsystems (UNIX)
Isdata GmbH Haid-und-Neu-Str. 7 D-7500 Karlsruhe 1 West Germany 0721-693092	LOG/iC™ Rev 3.2 – GA23S8	IBM PC or compatible DEC VAX (VMS, UNIX) Apollo (Aegis) Sun Microsystems (386i) Hewlett-Packard (9000)
Logical Devices Inc. 1201 N.W. 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Rev 3.0	IBM PC or compatible DEC VAX (VMS, UNIX)

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Programming Procedure

The final phase of the design process incorporates device programming. Gazelle's GA23SV8/GA23S8 are factory programmed using a proven laser technology. Metal lines are physically removed versus electrically fusing or writing to EPROM cells. The only customer input required is your programming information in the form of an industry-standard JEDEC file or two identically-programmed silicon devices (23S8 only) with intact (unblown) security fuses. The programming information is then automatically converted to a laser map that indicates which metal links need to be removed. Simultaneously, test vectors are generated and stored until the device is ready for final test. At final test, 100% of the devices are functionally and parametrically tested using the test vectors that have been generated.

The Programming Input can be accepted in the following formats:

A. 5-1/4 inch diskette, 1.2M or 360K (IBM format)

B. 3-1/2 inch diskette, 720K (IBM format)

C. 3-1/2 inch diskette, 800K or 400K (Apple Macintosh format)

D. Programmed silicon (23S8 only).

The diskette protocol must be IBM, Apple Macintosh or 100% compatible. Each file must have a backup. Please identify the backup file by inserting (BKU) after the original file name.

When using programmed silicon 23S8s to transfer programming information, please send two identically programmed 23S8s, ensure that the security fuses are intact (unblown) and include the fuse checksum.

Mark the programming information (diskette or programmed silicon devices) with a code number that identifies the contents. Gazelle will assign a "C" number to this code and mark all devices manufactured to this code with the "C" number assigned.

Please contact Gazelle with any questions pertaining to programming procedures.

GaAs-Pack

To facilitate the delivery of prototype samples, Gazelle has developed the GaAs-Pack. The GaAs-Pack contains everything necessary to obtain one programmed and fully-tested device, within five working days or less.

To use the GaAs-Pack, all you have to do is fill out the enclosed order form, sign the GaAs-Pack certificate and enclose the order form and the certificate with your programming information (diskette or two programmed silicon devices) in the prepaid preaddressed Federal Express envelope.

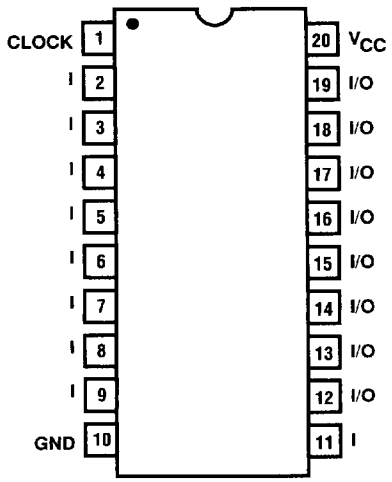
Gazelle will return one programmed and fully-tested device via Federal Express, within five working days or less.

The GaAs-Packs can be purchased in quantity in advance for later use. To order your supply of GaAs-Packs, please follow the ordering instructions on page 11.

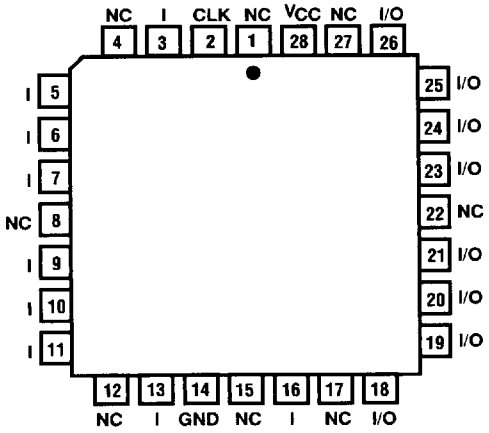
Connection Diagram

Top View

20-Pin Ceramic
Side-Brazed DIP



28-Pin Ceramic
J-Leaded Chip Carrier



Ordering Information

Gazelle's products are available in several speeds, packages and operating ranges. The order number (valid combinations) is listed below:

GA - ____ ____ ____ ____

TYPE OF ORDER
BLANK = IC Devices
GP = GaAs-Pack

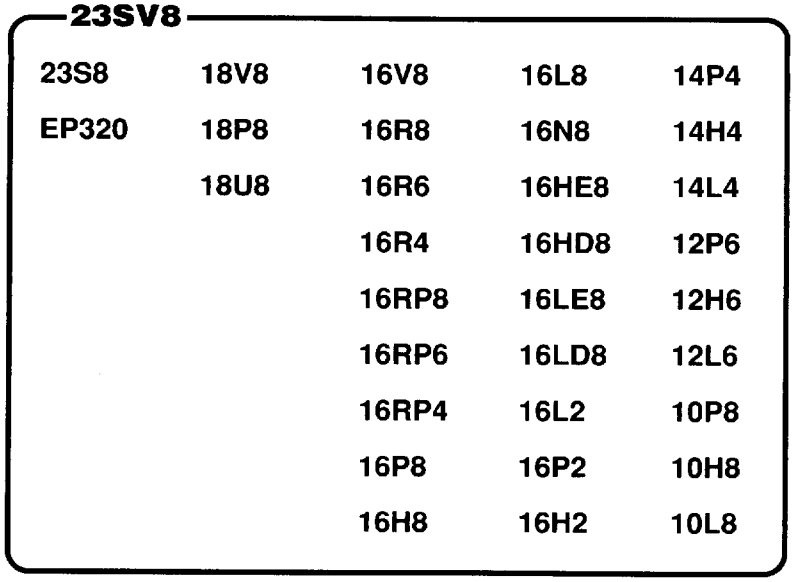
TEMPERATURE RANGE
C = Commercial (0°C to +75°C)
M = Military (–55°C to +125°C)

PACKAGE TYPE
S = 20-Pin Side Brazed DIP
C = 28-Pin Ceramic J-Leaded Chip Carrier

SPEED
–7 = 7.5 ns t_{PD}
–10 = 10 ns t_{PD}
–12 = 12 ns t_{PD} (Military Only)

DEVICE NUMBER/DESCRIPTION
GA23SV8
GA23S8

20-Pin PLDs Superset Diagram



The GA23SV8 is a functional superset of 32 PLDs

	Array Inputs	Registers	Dedicated Inputs	Dedicated Outputs	Bidirectional I/O	Product Terms	GA23SV8 Superset	
							Functional	Pin Compatible
23SV8	23	14	9	0	8	135	✓	✓
23S8	23	14	9	0	8	135	✓	✓
18V8	18	8	10*	0	8	72	✓	(1)
18P8	18	0	10*	0	8	72	✓	(1)
16V8	17	8	10*	0	8	64	✓	(1)
16R8	16	8	8	8	0	64	✓	✓
16R6	16	6	8	6	2	64	✓	✓
16R4	16	4	8	4	4	64	✓	✓
16L8	16	0	10	2	6	64	✓	(1)

* Pin 1 Doubles as an input or a clock pin

Note (1) Difference in Pin 1 only. Pin compatible superset when one or more registers are used

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