

SANYO**LC78641E****Compact Disk Player DSP****Preliminary****Overview**

The LC78641E is a CMOS IC that integrates servo control for audio CDs, EFM signal processing, and audio signal processing on one chip, enabling the configuration of systems with a small number of peripheral components. The servo control block performs A/D conversion of FE, TE, and RFENV signals from the head amplifier (LA9235M), digitally performs focus, tracking, sled, and spindle servo processing required for the CD servo, and performs D/A conversion and output of control signals to each actuator.

The EFM signal processing block has EFM signal demodulation and sync detection/protection/interpolation, deinterleave, and error detection and correction functions.

The audio signal processing block has data interpolation/muting functions used according to the error correction status, an 8× over sampling digital filters, a 1-bit DAC, and LPF (operational amplifier). The status and characteristics of each function block can be set and its data can be read via the microcontroller interface.

Playback function

- Audio CD playback (normal speed, 2× speed)
- Jitter free playback (VCEC)

Servo control block

- Digital processing of tracking, focus, sled, and spindle servos
- Automatic adjustment functions: focus gain, focus offset, focus bias, tracking gain, tracking offset, tracking balance
- Quantity of light, scratch, shock, jitter detection
- Track jump through speed control

EFM processing block

- Error detection, correction (dual C1 puls dual C2 correction)
- Jitter margin ± 4 frames
- EFM signal sync detection, protection, interpolation

Audio processing block

- Interpolation (Quadruple interpolation)
- Digital attenuator
- Built-in deemphasis filter
- 1-bit DAC (third-order noise shaper method)

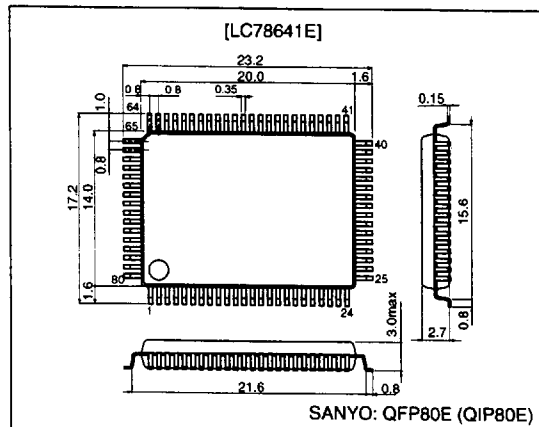
- Built-in audio output LPF
- Fade-out function
- Bilingual function
- Built-in 8× audio sampling digital filter

Supply voltage and package dimensions

- Package: 80-pin plastic package
- Supply voltage 3.3 V
- (5-V interface with microcontroller possible)

Package Dimensions

unit: mm

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Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VDD3max		VSS – 0.3 to VSS + 4.6	V
	VDD5max		VSS – 0.3 to VSS + 6.0	V
Input voltage	VIN3		VSS – 0.3 to VDD3 + 0.3	V
	VIN5		VSS – 0.3 to VDD5 + 0.3	V
Output voltage	VOUT3		VSS – 0.3 to VDD3 + 0.3	V
	VOUT5		VSS – 0.3 to VDD5 + 0.3	V
Allowable power dissipation	Pdmax		300	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Range at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Pin Name	Ratings			Unit
			min	typ	max	
Supply voltage	VDD3	VDD, XVDD, LVDD, RVDD, VVDD, ADAVD0	3.0	3.3	3.6	V
	VDD5	VDD5V	3.0		5.5	V
High-level input voltage	VIH3(1)	HFL, FG, CONT1 to 5, TEST, EMPH, ASLRCK, ASDATA, ASDFIN, SBCK, DEFECT	0.7 VDD3		VDD3	V
	VIH3(2)	EFMIN	0.6 VDD3		VDD3	V
	VIH5(1)	CE, CL, DI, *RES	0.8 VDD5		VDD5	V
	VIH5(2)	CONT6 to 7	0.7 VDD5		VDD5	V
Low-level input voltage	VIL3(1)	HFL, FG, CONT1 to 5, TEST, EMPH, ASLRCK, ASDATA, ASDFIN, SBCK, DEFECT	0		0.2 VDD3	V
	VIL3(2)	EFMIN	0		0.4 VDD3	V
	VIL5(1)	CE, CL, DI, *RES	0		0.2 VDD5	V
	VIL5(2)	CONT6 to 7	0		0.3 VDD5	V
Data/CE set up time	tSU	CL, DI, CE	400			ns
Data/CE hold time	tHD	CL, DI, CE	400			ns
High-level clock pulse width	tWH	SBCK, CL	400			ns
Low-level clock pulse width	tWL	SBCK, CL	400			ns
Data read access time	tRAC	DO, PW	0		400	ns
Command transfer time	tCE	CE	1000			ns
Subcode read cycle time	tSC	SFSY		136		μs
Subcode read enable time	tSF	SFSY	400			ns
Port input data setup time	tCSU	CONT1 to CONT7, CL	400			ns
Port input data hold time	tCHD	CONT1 to CONT7, CL	400			ns
Port output data delay time	tCDD	CONT1 to CONT7, CE			1200	ns
Operating frequency range	fOP	EFMIN			10	MHz
Xtal oscillation frequency	fX	XIN, XOUT		16.9344		MHz

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Electrical Characteristics at Ta = 25°C, VDD = 3.3 V, VSS = 0 V

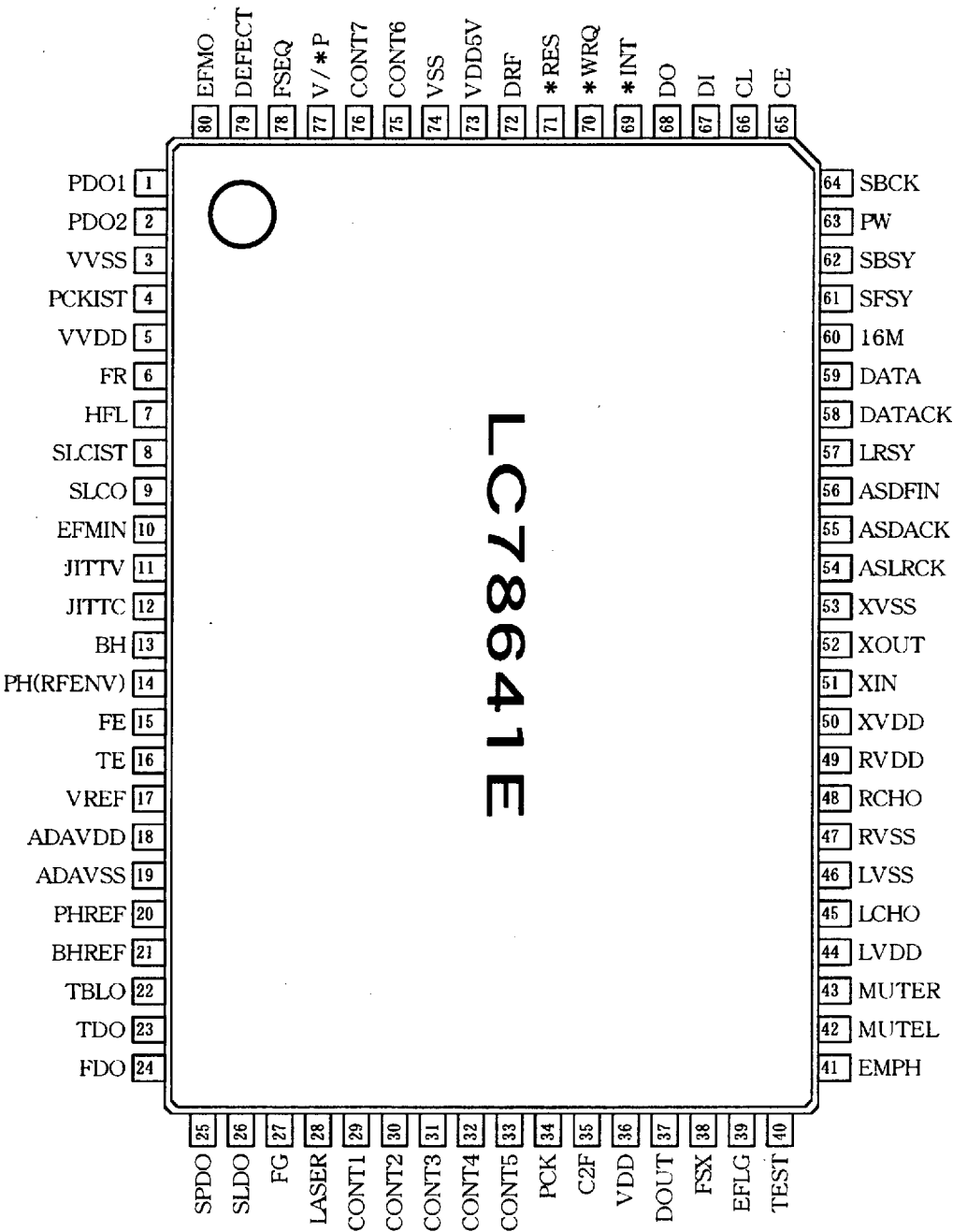
Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Current drain	IDD	VDD, XVDD, LVDD, RVDD, VVDD, ADAVD, VDD5V	Normal speed		30	45	mA
High-level input current	I _{IH3}	HFL, FG, CONT1 to 5, TEST, EMPH, ASLRCK, ASDATA, ASDFIN, SBCK, DEFECT	V _{IN} = 3.6 V			10	μA
	I _{IH5}	CE, CL, DI, *RES, CONT6 to 7	V _{IN} = VDD5V = 5.5 V			10	μA
Low-level input current	I _{IL3}	HFL, FG, CONT1 to 5, TEST, EMPH, ASLRCK, ASDATA, ASDFIN, SBCK, DEFECT	V _{IN} = 0 V	-10			μA
	I _{IL5}	CE, CL, DI, *RES, CONT6 to 7	V _{IN} = 0 V	-10			μA
High-level output current	V _{OH3}	LASER, CONT1 to 5, PCK, C2F, FSX, EFLG, EMPH, MUTEL, MUTER, LRSY, DATA, DATA, 16M, SFSY, SBSY, PW, V/*P, FSEQ, EFMO, DEFECT, DOUT	I _{OH} = -4 mA	VDD3 - 0.8			V
	V _{OH5}	DO, *INT, *WRQ, DRF, CONT6 to 7	I _{OH} = -4 mA	VDD5 - 2.1			V
Low-level output current	V _{OL3}	LASER, CONT1 to 5, PCK, C2F, FSX, EFLG, EMPH, MUTEL, MUTER, LRSY, DATA, DATA, 16M, SFSY, SBSY, PW, V/*P, FSEQ, EFMO, DEFECT, DOUT	I _{OL} = 4 mA			0.4	V
	V _{OL5}	DO, *INT, *WRQ, DRF, CONT6 to 7	I _{OL} = 4 mA			0.4	V
Charge pump output current	I _{PDOH}	PDO	R _{ISSET} = 2.7 kΩ	36	45	54	μA
	I _{PDOL}	PDO	R _{ISSET} = 2.7 kΩ	-54	-45	-36	μA

Analog Characteristics of 1-Bit DAC Block at Ta = 25°C, VDD = LVDD = RVDD = 3.3 V, VSS = LVSS = RVSS = 0 V

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Total harmonic distortion	THD+N	LCHO, RCHO	1 KHz: 0 dB data input, 20 KHz-LPF use (AD725 built in)	—	—	—	%
D range	DR	LCHO, RCHO	1 KHz: -60 dB data input, 20 KHz-LPF, A filter use (AD725D built in)	—	—	—	dB
Signal-to-noise ratio	S/N	LCHO, RCHO	1 KHz: 0 dB data input, 20 KHz-LPF, A filter use (AD725D built in)	—	—	—	dB
Crosstalk	CT	LCHO, RCHO	1 KHz: 0 dB data input, 20 KHz-LPF use (AD725D built in)	—	—	—	dB

Note: * Measured in normal playback mode with Sanyo's 1-bit DAC block reference circuit.

Pin Assignment



Top view

Block Diagram

