MUSIC SEMICONDUCTORS

MU9C7201, MU9C7202 MU9C7203, MU9C7204 512 X 9, 1K X 9, 2K X 9, AND 4K X 9 CMOS FIFOs

PRELIMINARY SPECIFICATION

DISTINCTIVE CHARACTERISTICS

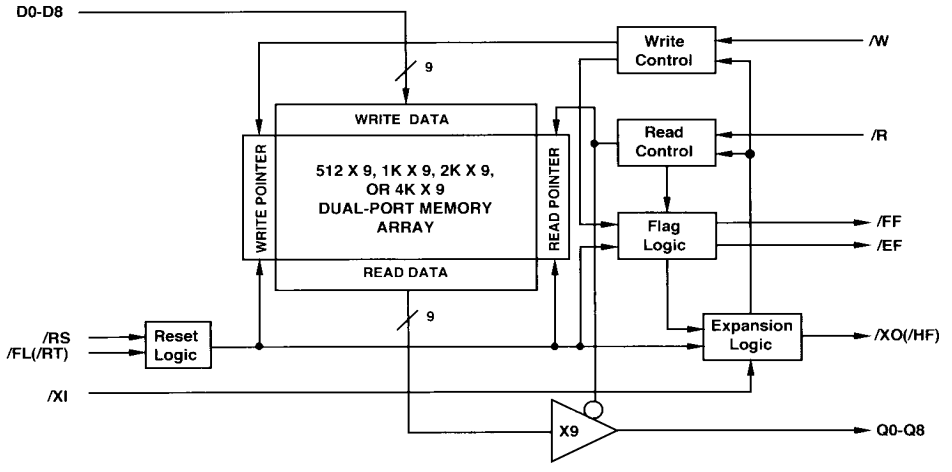
- **High-speed First-in, First-out buffers**
- **50 ns Access time, 65 ns Cycle time (15.4 MHz)**
- **512 x 9, 1K X 9, 2K X 9, and 4K X 9 organizations**
- **Asynchronous/simultaneous operation on both Read and Write Ports**
- **Expandable in depth and width with minimal external logic**
- **Full, Half-full, Empty Flags**
- **Retransmit capability**
- **Industry-standard pinouts, packages (0.3-inch and 0.6-inch 28-pin PDIPs and 32-pin PLDCC)**

GENERAL DESCRIPTION

The MU9C7201-MU9C7204 are high-density CMOS First-in, First-out (FIFO) Memories with capacities of 512, 1024, 2048, and 4096 nine-bit words, respectively. The nine-bit-word configuration facilitates passing parity information through the FIFOs. The depths of these FIFOs make them ideal for applications which need significant bandwidth elasticity such as between systems that transfer data at significantly different data rates. Because no address lines are needed for FIFOs, these devices offer both upward and downward pin compatibility. Due to their architecture, these devices offer very high performance and simultaneous and asynchronous operation of the Read and Write ports. These FIFOs are easily expanded in both width and depth with little or no external logic and without any degradation in performance compared to single-device operation. Each FIFO offers a flexible flag architecture with Full, Empty and Half-full flags.

MUSIC Semiconductors offers the MU9C7201-MU9C7204 in industry-standard pin configurations in narrow-width (0.3 inches) and standard-width (0.6 inches) 28-pin DIP and 32-pin PLDCC packages with operation guaranteed over the commercial temperature range (0 - 70 °C).

BLOCK DIAGRAM



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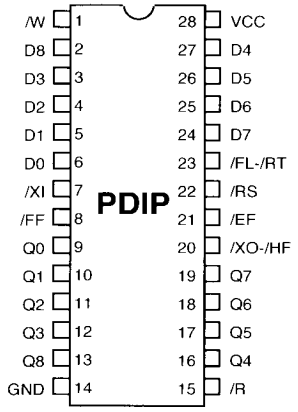
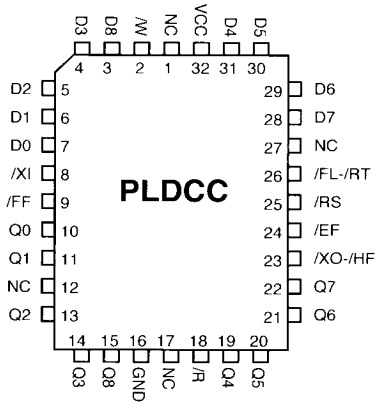
PINOUT DIAGRAMS





PIN DESCRIPTIONS

D0-D8 (Data Inputs, TTL-Compatible)

Data are input on D0-D8 during Write cycles, where the signals on D0-D8 must meet set-up and hold times relative to the rising (trailing) edge of /W.

/W (Write, Active-LOW Input, TTL-Compatible)

The falling edge of /W initiates a Write cycle (assuming a not-full and selected FIFO). The Write data on D0-D8 are captured on the rising edge of /W. If the FIFO is full (/FF LOW), then the Write cycle is inhibited until a Read cycle makes room for new data. If a FIFO is deselected by the Expansion logic, the Write signal is ignored, and the selected FIFO in the chain responds to the Write operation.

Q0-Q8 (Data Outputs, Three-state TTL-Compatible Outputs)

Read port output data pins Q0-Q8 are high-impedance except during Read cycles, which are controlled by /R when /EF is HIGH and /XI is LOW in the Single-device mode, or in the Depth Expansion mode the device is selected for reads. When /EF is LOW at the start of a Read cycle, the data requested will not be valid until a Write cycle is executed. If the FIFO is not selected for Read cycles while in the Depth Expansion mode, Q0-Q8 remain in the high impedance state.

/R (Read, Active-LOW Input, TTL-Compatible)

/R is used to control Read cycles on the Read port, provided /EF is HIGH, and in the Depth Expansion mode the device is selected for Read operations. If the Read cycle returns the last remaining data word, /EF goes LOW. If /FF is LOW prior to the read, /FF will go HIGH after the trailing edge of /R. If the FIFO is deselected in the Depth Expansion mode, /R is ignored.

/RS (Reset, Active-LOW Input, TTL-Compatible)

Whenever the system is initialized, /RS must be pulsed LOW to place the FIFO in a known state. After /RS goes HIGH, the Read and Write pointers address memory location "0." /FF and /HF go HIGH and /EF goes LOW due to the status of the Read and Write pointers. /RS is normally controlled by the system assigned to the FIFO's Write port.

/XI (Expansion Input, Active-LOW, CMOS)

/XI is grounded for the Single Device mode and connected to the previous device's /XO output in the Depth Expansion mode. The /XI pin is pulsed LOW to show that the prior device in the daisy chain is at the last memory location for either Read or Write cycles, causing this next device to begin responding to Read or Write cycle requests. If a FIFO is the first device (with /FL-/RT LOW), /XI is connected to the last device's /XO.

/FL-/RT (First-Load or Retransmit, Active-LOW Inputs, TTL-Compatible)

/FL (Depth-Expansion Mode Only)

In the Depth Expansion mode the first device's /FL pin is grounded to indicate that it is the first device to be selected for both Read and Write operations. The remaining devices' /FL pins are tied to VCC. When selected for Read or Write operations, the FIFO will respond to the proper control signals for the selected Read or Write cycles. If deselected for the Read or Write cycles, the deselected cycle will be ignored.

PIN DESCRIPTIONS (CON'D)

/RT (Single-Device Mode Only)

The /RT signal is pulsed LOW to initialize the Read pointer to the first memory location. The Write pointer is not changed. /R must be inactive during the Retransmit cycle. The contents of the FIFO may be re-read after a Retransmit cycle.

/FF (Full Flag, Active-LOW Output, TTL-Compatible)

The /FF (Full Flag) signal indicates when the FIFO is full and also inhibits Write operations when active. /FF becomes set (LOW) after the falling edge of /W which caused the FIFO to become full. /FF goes HIGH after the rising edge of /R in the first valid (selected) Read cycle after the FIFO became full. /FF goes HIGH after the Reset function.

/EF (Empty Flag, Active-LOW Output, TTL-Compatible)

The /EF (Empty Flag) is used to indicate when the FIFO is empty. /EF goes LOW during the Reset function and after the falling edge of /R which caused the FIFO to become empty. /EF goes HIGH after the rising edge of /W during the first valid (selected) Write cycle into an empty FIFO.

VCC (+5-volt Power Supply)

/XO-/HF (Expansion Out or Half-Full Flag, Active-LOW Output, TTL/CMOS-Compatible)

/XO (Expansion Output, Depth-Expansion Mode Only)

The /XO (Expansion Out) pin is tied to /XI of the following device in the Depth Expansion mode. /XO is used to indicate to the next FIFO that the Read or Write pointer has reached the last memory location. Multiple FIFO devices operated in the Depth Expansion mode operate as a circular ring buffer, with the Read pointer following the Write pointer across device boundaries. /XO indicates that first the Write pointer, then the Read pointer proceeds to the next device in the ring.

/HF (Half-Full Flag, Single-Device Mode Only)

The /HF (Half Full) Flag is used in the Single Device mode. to indicate when more than half of the available space is used. /HF is set LOW after the falling edge of /W that causes the FIFO to become half full. /HF is reset HIGH after the rising edge of /R that causes the FIFO to no longer be half full.

GND (Ground Reference Power Supply)

FUNCTIONAL DESCRIPTION

These FIFO buffers have two operational modes. The first is the Single Device mode, invoked by connecting the /XI signal to ground (LOW). In this mode the /XO-/HF flag is interpreted as the Half-full Flag (/HF), which goes LOW when the FIFO is half full. In the Single Device mode the /FL-/RT signal implements the Retransmit function, which resets the Read pointer to the first address in the array and is invoked by pulsing the /RT signal LOW while /R is inactive.

Depth Expansion is the second mode. The /XI pin of each device is connected to the /XO pin of the preceding device in the chain in a circular fashion. The /FL (First Load) pin of the first device in the chain is grounded (LOW). The /FL pins of all the other devices in the chain are connected to VCC. Data are written into the first device in the chain until the last write location is reached at which time the /XO signal of that device pulses LOW. This event causes the second device in the chain to respond to subsequent Write cycles, and so forth around the chain until the first device begins to fill again. Likewise, when the first device has reached its last read location, its /XO signal pulses LOW again to indicate that the second device in the chain is to respond to subsequent Read cycles. External logic combines the individual Full and Empty flags to produce system Full and Empty flags.

The state of the /XI and /FL inputs to a given FIFO during a Reset cycle determines how the Depth Expansion logic is configured and initialized. The three possibilities are Single Device Mode, Depth Expansion mode (first device) and Depth Expansion mode (not first device). Expansion in both the depth and width dimensions is very simple for these FIFOs as shown in Figures 1 and 2. Further, the synthesis of system flags is also easily accomplished as indicated in Figure 2.

The Reset cycle is performed by pulsing the /RS input LOW. The device must not be performing an active Read or Write cycle when a Reset pulse occurs. After Reset, the FIFO is empty, and both the Read and Write internal pointers are set to the first memory location. The /EF output will go LOW, and the /FF output will go HIGH during a Reset cycle. If the FIFO is in the Single Device mode, the /HF output will go HIGH.

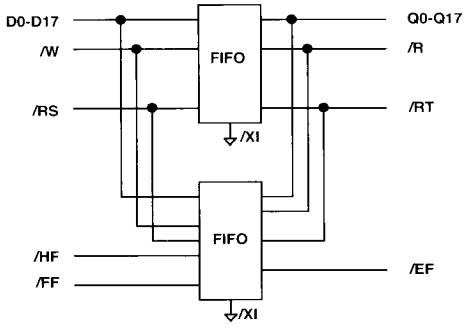


Figure 1: Width Expansion (512, 1K, 2K, or 4K) X 18 FIFO

FUNCTIONAL DESCRIPTION (CON'D)

A Write cycle is initiated when the /W input goes LOW provided the FIFO is selected by the Expansion logic or is in the Single Device mode and is not full. A Write cycle writes the data present on the D0-D8 inputs into the device at the address pointed to by the internal Write pointer if the data input signals meet the set-up and hold time requirements relative to the rising edge of /W. If the /FF output is LOW prior to the falling edge of /W, the Write cycle is inhibited and must be delayed until after a Read cycle occurs and /FF goes HIGH. If a particular Write cycle takes the last available FIFO location, the /FF output goes LOW after the falling edge of /W. The /FF output may be sampled prior to a Write cycle or used as a wait-state control. The /EF output from an empty FIFO will go HIGH after the rising edge of /W in a Write cycle. The /HF output of a FIFO in the Single Device mode will go LOW after the falling edge of the /W signal that caused the FIFO to be half full.

A Read cycle is initiated when the /R input goes LOW if the FIFO is selected by the Expansion logic or is in the Single Device mode and is not empty. A Read cycle causes the data from the location in the array pointed to by the internal Read pointer to be placed on the Q0-Q8 outputs after the access time has elapsed from the falling edge of /R.

If the /EF output is LOW prior to the falling edge of /R, the Read cycle will be inhibited until a Write cycle causes /EF to go HIGH. If the FIFO is full, the rising edge of /R will cause the /FF output to go HIGH since a Read cycle will cause the FIFO to no longer be full. The /HF output of a FIFO in the Single Device mode will go HIGH after the rising edge of the /R signal that causes the FIFO to be less than half full.

A Retransmit cycle is initiated by pulsing the /RT input LOW while the /R input is inactive in the Single Device mode. A Retransmit cycle causes the internal Read pointer to be reset to the starting location in the FIFO. This function is especially useful where a system error has occurred and the data in the FIFO needs to be reread.

Since these FIFOs are high-performance CMOS devices, care must be taken in the system design using them. As in the case of any high-speed memory, the power supply pins should be capacitively bypassed to prevent high-frequency noise generated by the system or by the FIFOs from causing data errors. The short rise and fall times of each of the nine outputs makes this bypassing especially important. MUSIC™ Semiconductors recommends the use of 0.01-microfarad capacitors connected between VCC and GND with minimum lead lengths to minimize lead inductance. An additional 100-picofarad capacitor also connected between VCC and GND will provide additional beneficial bypassing.

High-speed input signals to the FIFOs may need to be terminated with an impedance that matches the transmission line characteristics of the printed circuit board on which the FIFOs are used. The specifications for these devices allow a negative voltage undershoot whose amplitude is allowed to be up to 1.0 volt with a duration of 10 ns at the 50% amplitude point. Correct operation is not guaranteed if this specification is violated.

Since the two ports of a FIFO operate asynchronously relative to each other, Flag output metastability or oscillation is possible at or near the boundary conditions affecting the Flags (empty, full or half full). The MUSIC™ Semiconductors family of FIFOs has been designed to minimize this effect.

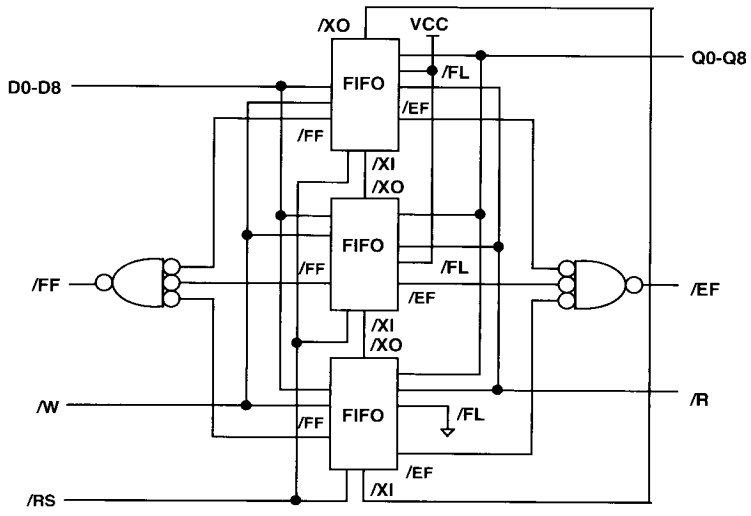


Figure 2: Depth Expansion Mode 3 X (512, 1K, 2K, or 4K) X 9 FIFO

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-3.0 Volts for 10 ns, measured at the 50% point)*
Temperature Under Bias	-10°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	1.0W
DC Output Current	50 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.
All voltages are referenced to GND.

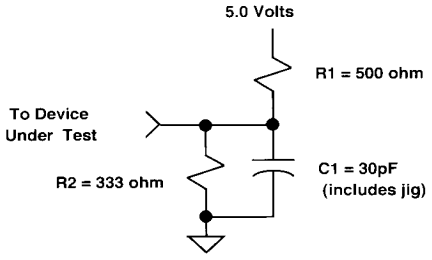
OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1"	2.2		VCC+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured at 50% amplitude*
$V_{IL(XI)}$	Input LOW Voltage (/XI)			1.5	Volts	
$V_{IH(XI)}$	Input HIGH Voltage (/XI)	3.5			Volts	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

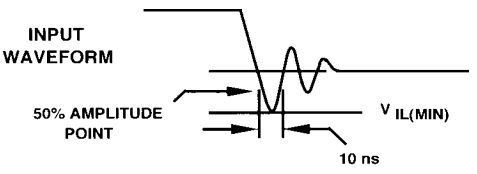
ELECTRICAL CHARACTERISTICS (over the Operating Temperature and Voltage ranges)

Symbol	Parameter	Min	Max	Units	Notes
I_{CC}	Average Power Supply Current		80 8 0.5	mA mA mA	/R, /W @ min. cycle time /R=/W=/RS=/FL-RT≥V_{IH} 0.2v≥V_{IN}≥V_{CC}-0.2v
V_{OH1}	Output Voltage Logic "1"	2.4		Volts	I_{OH} = -4.0 mA
V_{OH2}	Output Voltage Logic "1" (CMOS)	V_{CC}-0.1		Volts	I_{OH} = -100 µA
V_{OL}	Output Voltage Logic "0"		0.4	Volts	I_{OL} = 8.0 mA
I_{ILK}	Input Leakage Current	-1	1	µA	V_{GND} ≤ V_{IN} ≤ V_{CC}
I_{OLK}	Output Leakage Current (Q0-Q8)	-10	10	µA	V_{GND} ≤ V_{OUT} ≤ V_{CC}, /R ≥ V_{IH}(min)
C_{IN}	Input Capacitance		5	pF	1
C_{OUT}	Output Capacitance		7	pF	1

AC TEST LOAD



*INPUT SIGNAL WAVEFORM



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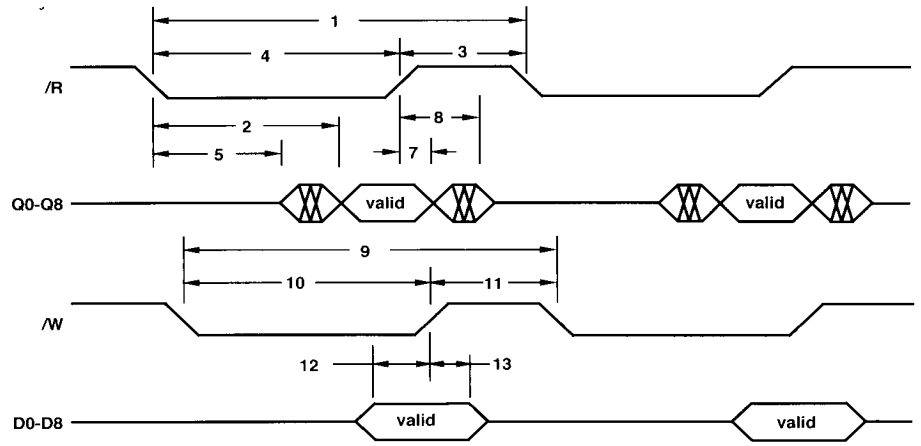
SWITCHING CHARACTERISTICS (Note 2)

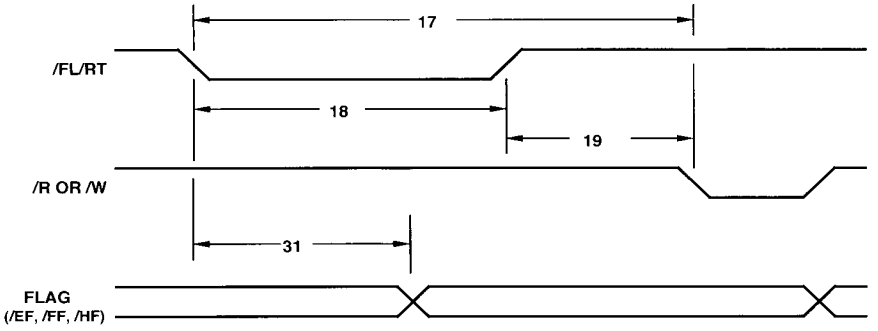
No.	Symbol	Parameter	-50		-65		-80		Units	Notes
			Min	Max	Min	Max	Min	Max		
1	tRLRL	Read Cycle Time	65		80		100		ns	
2	tRLQV	Access Time		50		65		80	ns	
3	tRHRL	Read Recovery Time	15		15		20		ns	
4	tRLRH	Read Pulse Width	50		65		80		ns	
5	tRLQX	Read LOW to Data-out Active	5		5		5		ns	3
6	tWHQX	Write HIGH to Data-out Active	10		10		12		ns	3
7	tRHQX	Data-out Hold Time	5		5		5		ns	3
8	tRHQZ	Read HIGH to Data-out High Impedance		30		30		30	ns	
9	tWLWL	Write Cycle Time	65		80		100		ns	
10	tWLWH	Write Pulse Width	50		65		80		ns	
11	tWHWL	Write Recovery Time	15		15		20		ns	
12	tDVWH	Data-in Set-up Time	30		30		40		ns	
13	tWHDX	Data-in Hold Time	5		10		10		ns	
14	tRSLWL	Reset Cycle Time	65		80		100		ns	
15	tRSLRSH	Reset Pulse Width	50		65		80		ns	
16	tRSHWL	Reset Recovery Time	15		15		20		ns	
17	tRTLWL	Retransmit Cycle Time	65		80		100		ns	
18	tRTLRTH	Retransmit Pulse Width	50		65		80		ns	
19	tRTHRL	Retransmit Recovery Time	15		15		20		ns	
20	tRSLFV	Reset LOW to Flag Valid Delay		65		80		100	ns	
21	tRLEFL	Read LOW to Empty LOW Delay		45		60		60	ns	
22	tRHFFH	Read HIGH to Full HIGH Delay	5	45	5	60	5	60	ns	
23	tEFHRH	Empty HIGH to Read HIGH Delay	50		65		80		ns	
24	tWHEFH	Write HIGH to Empty HIGH Delay	5	45	5	60	5	60	ns	
25	tWLFFL	Write LOW to Full LOW Delay		45		60		60	ns	
26	tWLHFL	Write LOW to Half-full LOW		65		80		100	ns	
27	tFFHWH	Full HIGH to Write HIGH Delay	50		65		80		ns	
28	tRHHFH	Read HIGH to Half-full HIGH		50		65		80	ns	
29	tWLXOL tRLXOL	Read or Write LOW to /XO LOW		50		65		80	ns	
30	tWHXOH tRHXOH	Read or Write HIGH to /XO HIGH		50		65		80	ns	
31	tRTLFV	Retransmit LOW to Flag Valid		65		80		100	ns	
32	tFFHFFL	Full Flag HIGH Pulse Width	5		5		5		ns	
33	tEFHEFL	Empty Flag HIGH Pulse Width	5		5		5		ns	

TIMING DIAGRAMS

ASYNCHRONOUS READ AND WRITE CYCLES TIMING DIAGRAM



RETRANSMIT TIMING

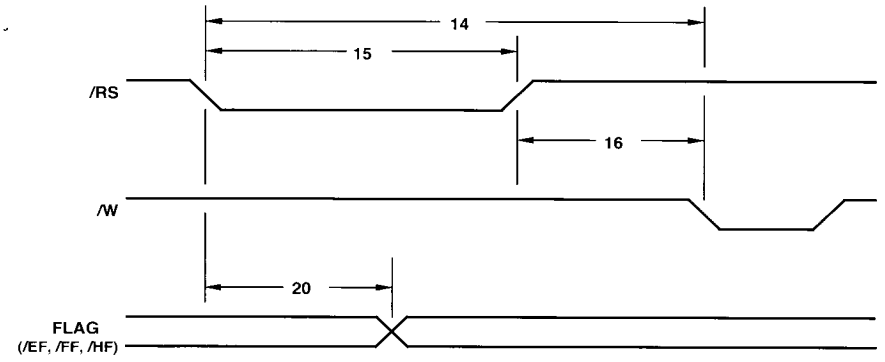


NOTES

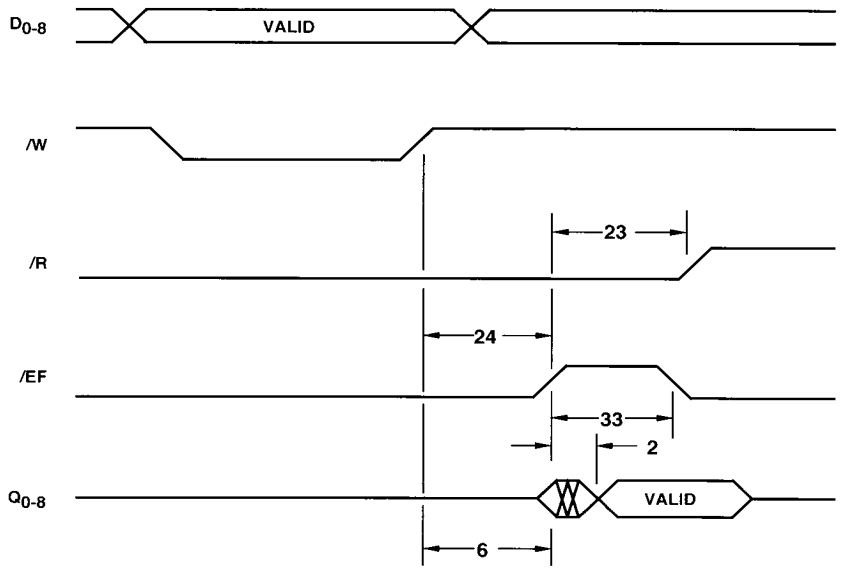
1. This parameter is not 100% tested, but is guaranteed by design.
2. Input voltage waveforms swing between 0 and 3 volts for Switching Characteristics testing. The input and output timing reference levels are at 1.5 volts. Switching Characteristics are specified over the operating temperature and voltage ranges.
3. Substitute C1= 5 pF for this parameter in the AC TEST LOAD diagram.

TIMING DIAGRAMS (CON'D)

RESET CYCLE TIMING DIAGRAM



READ DATA FLOW-THROUGH TIMING DIAGRAM



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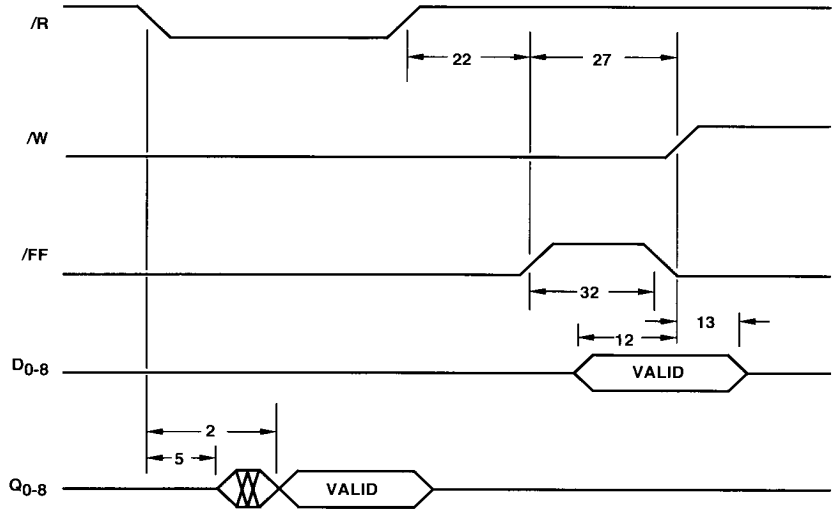
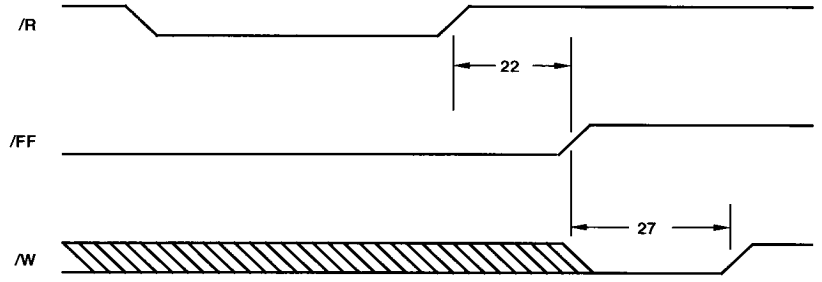
TIMING DIAGRAMS (CON'D)

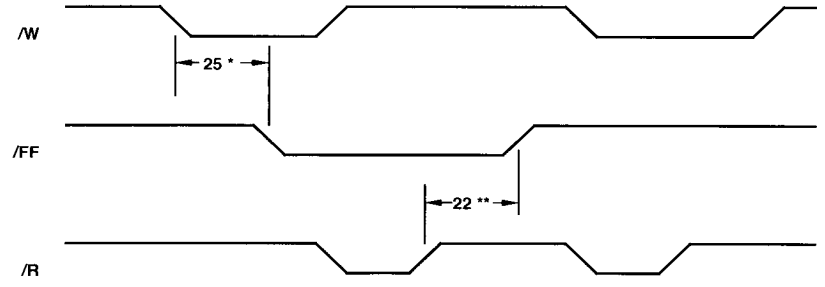
WRITE DATA FLOW-THROUGH TIMING DIAGRAM



FULL FLAG TIMING



a) FIRST WRITE AFTER FIFO CEASES TO BE FULL



b) FIRST READ AFTER FIFO BECOMES FULL

NOTES: * Last write - Data written to last free space in the FIFO.
** First read - Data read from full FIFO.

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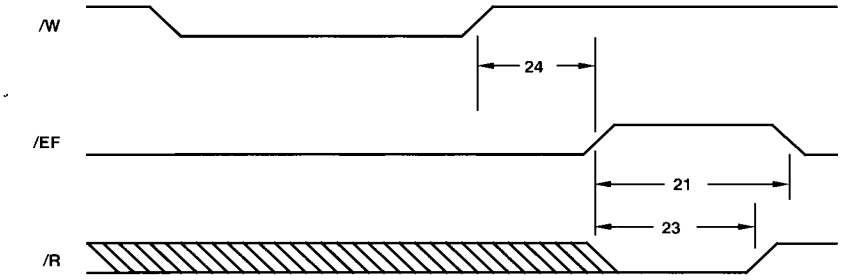
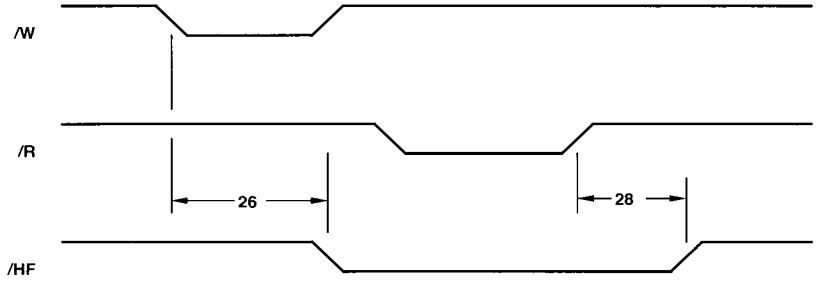
TIMING DIAGRAMS (CON'D)

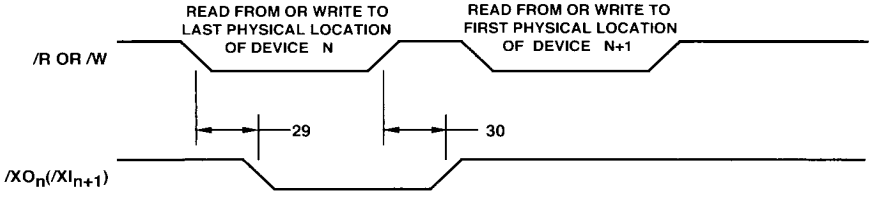
EMPTY FLAG TIMING



HALF-FULL FLAG TIMING

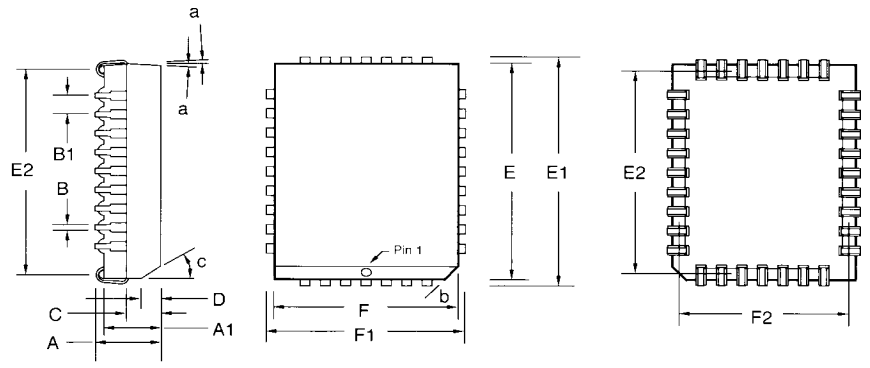


EXPANSION TIMING DIAGRAM



PACKAGE OUTLINES

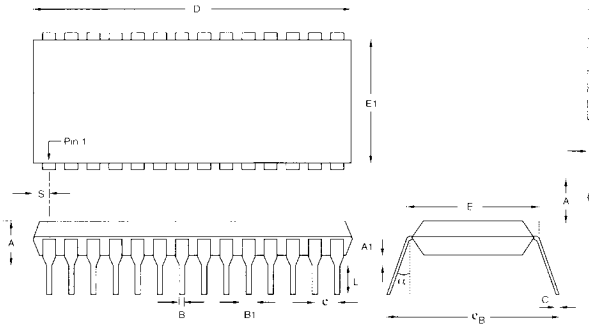
PLASTIC LEADED CHIP CARRIER



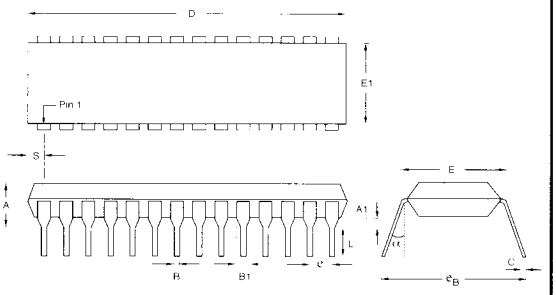
Lead Count	Dim. A	Dim. A1	Dim. B	Dim. B1	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. E2	Dim. F	Dim. F1	Dim. F2	Dim. a	Dim. b	Dim. c
32	.130 typ	.110 typ	.018 typ	.050 typ	.050 typ	.026 typ	.547 typ	.584 .596	.505 .525	.447 typ	.485 .495	.405 .425	7° typ	45° typ	60° typ

PLASTIC 600-MIL DIP

0.6-INCH PDIP



0.3-INCH PDIP



Lead Count	Dim. A	Dim. A1	Dim. B	Dim. B1	Dim. C	Dim. D	Dim. E	Dim. E1	Dim e	Dim. e_B	Dim. L	Dim. S	Dim. α
28 (0.3-in)	.155 typ	.310 max	.016 typ	.055 .065	.008 .013	1.345 1.360	.300 .325	.270 .290	.090 .110	.310 .370	.130 typ	.020 .040	5° 7°

Lead Count	Dim. A	Dim. A1	Dim. B	Dim. B1	Dim. C	Dim. D	Dim. E	Dim. E1	Dim e	Dim. e_B	Dim. L	Dim. S	Dim. α
28 (0.6-in)	.155 typ	.310 max	.016 typ	.055 .065	.008 .013	1.460 typ	.590 .610	.540 .560	.090 .110	.590 typ	.130 typ	.025 .070	5° 7°

All dimensions are in inches and degrees and are min/max except where noted.

Rev. 2

MU9C7201, MU9C7202, MU9C7203, MU9C7204

ORDERING INFORMATION

PART NUMBER	SIZE	ACCESS TIME	PACKAGE	TEMPERATURE RANGE
MU9C7201-**XX**Y**C**	512 X 9			0-70°C
MU9C7202-**XX**Y**C**	1K X 9			0-70°C
MU9C7203-**XX**Y**C**	2K X 9			0-70°C
MU9C7204-**XX**Y**C**	4K X 9			0-70°C
XX = 50		50ns		
XX = 65		65ns		
XX = 80		80ns		
Y = P			28-PIN PDIP (0.6-inch)	
Y = S			28-PIN PDIP (0.3-inch)	
Y = E			32-PIN PLDCC	

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