SINGLE CHIP FAST ETHERNET NIC CONTROLLER

1. FEATURES

- A single chip solution integrates 100/10 Base-T fast Ethernet MAC, PHY and PMD
- Fully comply to IEEE 802.3u specification
- Operates over 100 meters of STP and category 5 UTP cable
- Support full and half duplex operation in both 100 Base-TX and 10 Base-T mode
- Fully comply to PCI spec. 2.1 with bus clock ranges from 16MHz to 33MHz
- Fully comply to Advanced Configuration and Power Interface (ACPI) Rev 1.0
- Fully comply to PCI Bus Power Management Interface spec. Rev 1.0
- Magic Packet TM mode to support Remote-Power On and Remote-Wake-Up.
- 100/10 Base-T NWAY auto negotiation function
- Large on chip FIFOs for both transmit and receive operations without external local memory
- Bus master architecture with linked host buffers delivers the most optimized performance
- 32-bit bus master DMA channel provides ultra low CPU utilization
- Proprietary Adaptive Network Throughput Control (ANTC) technology to optimize data integrity and throughput
- Support up to 256K bytes boot ROM and FLASH interface
- Three levels of loopback diagnostic capability
- Support a variety of flexible address filtering modes with 16 CAM address and 512 bits hash
- MicroWire interface to EEPROM for customer's IDs and configuration data
- Single +5.0V power supply, standard CMOS technology, 160 pin PQFP package

(Magic Packet technology is a trademark of Advanced Micro Device Corp.)

2. GENERAL DESCRIPTIONS

The MX98725, second generation of 100/10 Base-T single chip MAC controller, is designed specifically to meet future demand on Fast Ethernet networking system. Different from MX98715/715a3, MX98725 additionally supports ACPI, Remote-Wake-Up, Remote-Power-On, and up to 256K Bytes Flash interface to enhance product's added-on value.

The MX9725 controller is an IEEE802.3u compliant single chip 32-bit full duplex, 10/100Mbps highly integrated Fast Ethernet combo solution, designed to address high performance local area networking (LAN) system application requirements.

The bus master architecture delivers the performance needed for today high speed and powerful processors technology. In other words, the MX98725 not only keeps CPU utilization low while maximizing data throughput, but it also optimizes the PCI bandwidth providing the highest PCI bandwidth utilization. To further reduce ownership costs the MX98725 uses drivers that are backward-compatible with the original MXIC MX98713 series controllers.

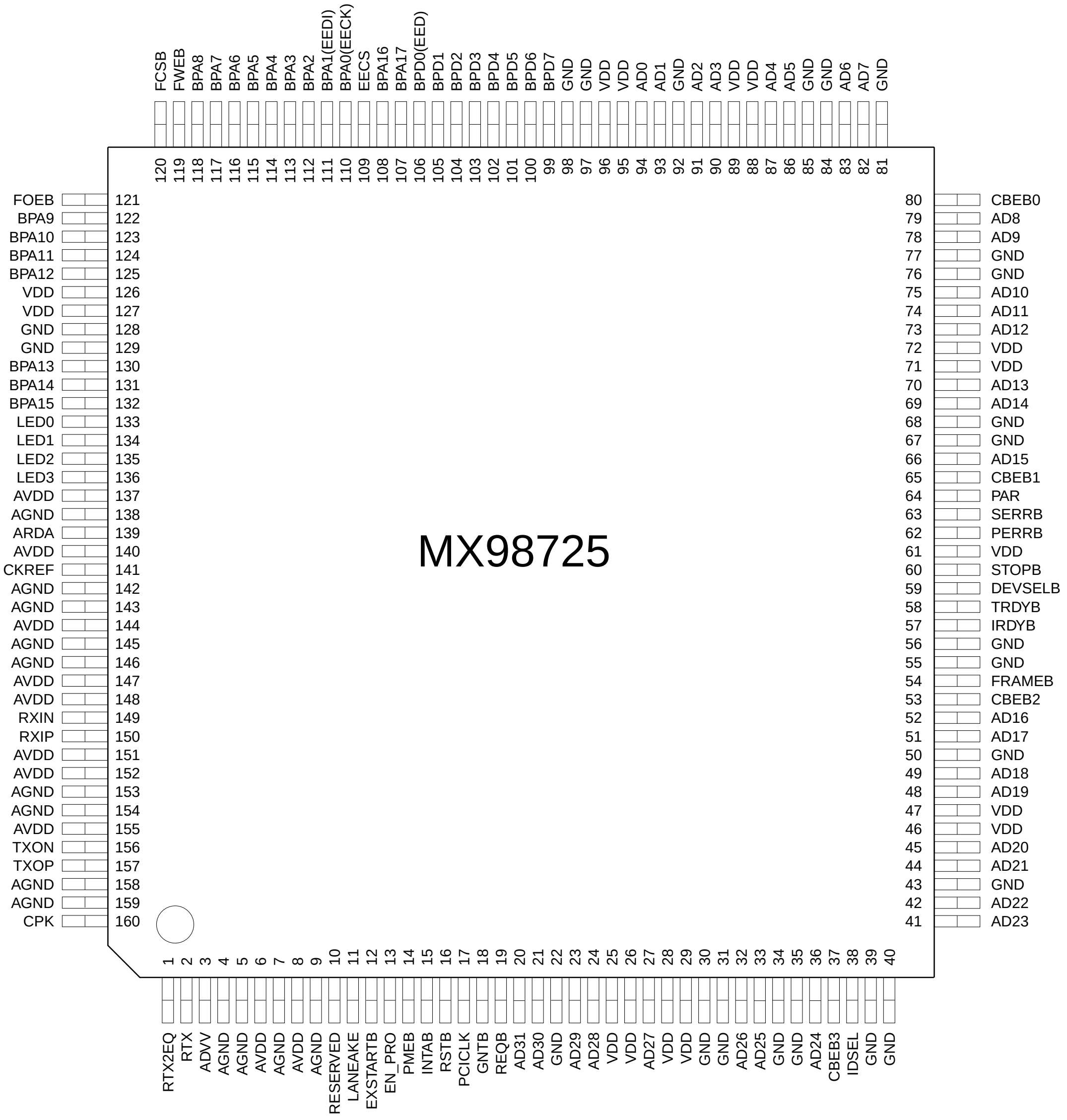
The MX98725 contains a PCI local bus glueless interface, a Direct Memory Access (DMA) buffer management unit, an IEEE802.3u-compliant Media Access Controller (MAC), large Transmit and Receive FIFOs, and an on-chip 10 Base-T and 100 Base-TX transceiver simplifying system design and improving high speed signal quality. Full-duplex operation are supported in both 10 Base-T and 100 Base-TX modes that increases the controller's operating bandwidth up to 200Mbps. Equipped with intelligent IEEE802.3u-compliant auto-negotiation, the MX98725-based adapter allows a single RJ-45 connector to link with the other IEEE802.3u-compliant device completely without any need to set configuration.

In MX98725, an innovative and proprietary design "Adaptive Network Throughput Control" (ANTC) is built-in to configure itself automatically by MXIC's driver based on the PCI burst throughput of different PCs. With this proprietary design, MX98725 can always optimize its operating bandwidth, network data integrity and throughput for different PCs.

MXIC MX98725 features Remore-Wake-Up capability and is compliant with the Advanced Configuration and Power Interface (ACPI). This support enables a wide range of wake-up capabilities, including the ability to customize which network packets the PC responds to, even when it is in a low-power state. PCs and workstations designed to take advantage of these capabilities can be turned on remotely and serviced simultaneiously over the network from one central server, helping organizations reduce their total cost of ownership of high-performance business PCs. With its on-chip support for both little and big endian byte alignment, this controller can also address non-PC applications.

For diskless applications of networking, remotely booting up is a necessary process. To update or modify the code is such a complex process that network venders or owners must provide a new EPROM, replace the existing EPROM on the network adaptor and then reboot the computer. Thanks to the development of Flash memory, MX98725 successfully incorporated Flash interface to provide remotely boot code update service and that means network maintenance becomes effortless.

3. PIN CONFIGURATIONS


MX98725
FCSB 120
FWEB 119
BPA8 118
BPA7 117
BPA6 116
BPA5 115
BPA4 114
BPA3 113
BPA2 112
BPA1(EEDI) 111
BPA0(EECK) 110
EECS 109
BPA16 108
BPA17 107
BPD0(EED) 106
BPD1 105
BPD2 104
BPD3 103
BPD4 102
BPD5 101
BPD6 100
BPD7 99
GND 98
GND 97
VDD 96
VDD 95
AD0 94
AD1 93
GND 92
AD2 91
AD3 90
VDD 89
VDD 88
AD4 87
AD5 86
GND 85
GND 84
AD6 83
AD7 82
GND 81
FOEB 121
BPA9 122
BPA10 123
BPA11 124
BPA12 125
VDD 126
VDD 127
GND 128
GND 129
BPA13 130
BPA14 131
BPA15 132
LED0 133
LED1 134
LED2 135
LED3 136
AVDD 137
AGND 138
ARDA 139
AVDD 140
CKREF 141
AGND 142
AGND 143
AVDD 144
AGND 145
AGND 146
AVDD 147
AVDD 148
RXIN 149
RXIP 150
AVDD 151
AVDD 152
AGND 153
AGND 154
AVDD 155
TXON 156
TXOP 157
AGND 158
AGND 159
CPK 160
80 CBEB0
79 AD8
78 AD9
77 GND
76 GND
75 AD10
74 AD11
73 AD12
72 VDD
71 VDD
70 AD13
69 AD14
68 GND
67 GND
66 AD15
65 CBEB1
64 PAR
63 SERRB
62 PERRB
61 VDD
60 STOPB
59 DEVSELB
58 TRDYB
57 IRDYB
56 GND
55 GND
54 FRAMEB
53 CBEB2
52 AD16
51 AD17
50 GND
49 AD18
48 AD19
47 VDD
46 VDD
45 AD20
44 AD21
43 GND
42 AD22
41 AD23
1 RTX2EQ
2 RTX
3 ADVV
4 AGND
5 AGND
6 AVDD
7 AGND
8 AVDD
9 AGND
10 RESERVED
11 LANEAKE
12 EXSTARTB
13 EN_PRO
14 PMEB
15 INTAB
16 RSTB
17 PCICLK
18 GNTB
19 REQB
20 AD31
21 AD30
22 GND
23 AD29
24 AD28
25 VDD
26 VDD
27 AD27
28 VDD
29 VDD
30 GND
31 GND
32 AD26
33 AD25
34 GND
35 GND
36 AD24
37 CBEB3
38 IDSEL
39 GND
40 GND

4. PIN DESCRIPTION (160 PIN PQFP)

(T/S : tri-state, S/T/S : sustended tri-state, I : input, O : output, O/D : open drain)

Pin Name	Type	Pin No.	160 Pin Function and Driver
AD[31:0]	T/S	20,21,23,24, 27,32,33,36, 41,37,38,42, 44,45,48,49, 51,52,66,69, 70,73,74,75, 78,79,82,83, 86,87,90,91, 93,94	PCI address/data bus: shared PCI address/data bus lines. Little or big endian byte ordering are supported.
CBEB[3:0]	T/S	37,53 65,80	PCI command and byte enable bus: shared PCI bus command and byte enable bus, during the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable.
FRAMEB	S/T/S	54	PCI FRAMEB signal: shared PCI cycle start signal, asserted to indicate the beginning of a bus transaction. As long as FRAMEB is asserted, data transfers continue.
TRDYB	S/T/S	58	PCI Target ready: issued by the target agent, a data phase is completed on the rising edge of PCICLK when both IRDYB and TRDYB are asserted.
IRDYB	S/T/S	57	PCI Master ready: indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of PCICLK when both IRDYB and TRDYB are asserted.
DEVSELB	S/T/S	59	PCI slave device select: asserted by the target of the current bus access. When MX98725 is the initiator of current bus access, the target must assert DEVSELB within 5 bus cycles, otherwise cycle is aborted.
IDSEL	I	38	PCI initialization device select: target specific device select signal for configuration cycles issued by host.
PCICLK	I	17	PCI bus clock input: PCI bus clock range from 16MHz to 33MHz.
RSTB	I	16	PCI bus reset: host system hardware reset.
INTAB	O/D	15	PCI bus interrupt request signal: wired to INTAB line.
SERRB	O/D	63	PCI bus system error signal: If an address parity error is detected and CFCS bit 8 is enabled, SERRB and CFCS’s bit 30 will be asserted.
PERRB	S/T/S	62	PCI bus data error signal: As a bus master, when a data parity error is detected and CFCS bit 8 is enabled, CFCS bit 24 and CSR5 bit 13 will be asserted. As a bus target, a data parity error will cause PERRB to be asserted.

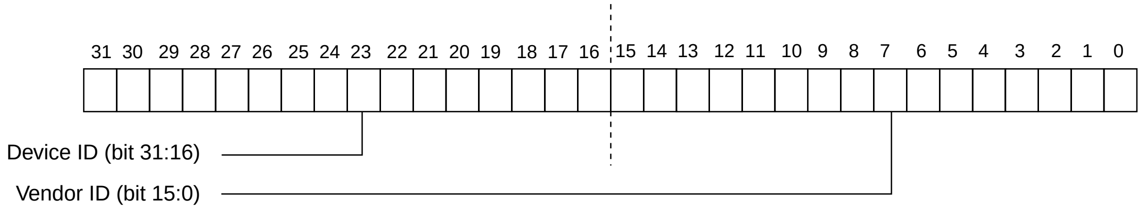
Pin Name	Type	Pin No.	160 Pin Function and Driver
PAR	T/S	64	PCI bus parity bit: shared PCI bus even parity bit for 32 bits AD bus and CBE bus.
STOPB	S/T/S	60	PCI Target requested transfer stop signal: as bus master, assertion of STOPB cause MX98725 either to retry, disconnect, or abort.
REQB	T/S	19	PCI bus request signal: to initiate a bus master cycle request
GNTB	I	18	PCI bus grant acknowledge signal: host asserts to inform MX98725 that access to the bus is granted
PMEB	O/D	14	Power Management Event: asserts low when Magic Packet is received.
EXSTARTB	O/D	12	Start externel circuit signal: asserts low to enable system's power supply when Magic Packet is detected. Normally tri-stated.
LANWAKE	O	11	LAN wake up signal: asserts high to indicate a magic packet has been detected in Magic Packet enable mode.
EN_RPO	I	13	Enable On-Chip Power-On-Reset : normally unconnected.
BPA1 (EEDI)	O	111	Boot PROM address bit 1(EECS=0): together with BPA[17:0] to access external boot PROM up to 256KB. EEPROM data in(EECS=1): EEPROM serial data input pin.
BPA0 (EECK)	O	110	Boot PROM address bit 0(EECS=0): together with BPA[17:0] to access external boot PROM or FLASH up to 256KB. EEPROM clock(EECS=1): EEPROM clock input pin
BPA[17:0]	O	107,108 110-118 123-125 130-132	Boot PROM address lines:
BPD0 (EEDO)	T/S	106	Boot PROM data line 0(EECS=0): boot ROM or flash data line 0. (EEPROM data out(EECS=1): EEPROM serial data out pin(during reset initialization.)
BPD[7:0]	T/S	99-106	Boot PROM data lines: boot ROM or FLASH data lines 7-0.
EECS	O	109	EEPROM chip select.
FWEB	O	119	FLASH Write Enable
FOEB	O	121	FLASH ROM Output Enable
FCSB	O	120	FLASH Chip Select pin
RDA	O	139	Connecting an external resistor to ground. See application note.
RTX	O	2	Connecting an external resistor to ground. See application note.
RTX2EQ	O	1	Connecting an external resistor to ground. See application note.
CPK	I	160	Connecting an external capacitor. See application note.
RXIP	I	150	Twisted pair receive differential input: Support both 10Base-T and 100 Base-TX differential receive input.
RXIN	I	149	Twisted pair receive differential input: Support both 10Base-T and 100 Base-TX receive differential input

Pin Name	Type	Pin No.	160 Pin Function and Driver
TXOP	O	157	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
TXON	O	156	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
CKREF	I	141	Reference clock: 25MHz oscillator clock input
LED0	O	133	Programmable LED pin 0: CSR9.28=1 Set the LED as Link Speed (10/100) LED. CSR9.28=0 Set the LED as Activity LED. Default is Activity LED after reset.
LED1	O	134	Programmable LED pin 1: CSR9.29=1 Set the LED as Link/Activity LED. CSR9.29=0 Set the LED as Good Link LED. Default is RX LED after reset.
LED2	O	135	Programmable LED pin 2: CSR9.30=1 Set the LED as Collision LED. CSR9.30=0 Set the LED as TX LED. Default is TX LED after reset.
LED3	O	136	Programmable LED pin 3: CSR9.31=1 Set the LED as Full/Half Duplex LED. CSR9.31=0 Set the LED as RX LED. Default is RX LED after reset.
RESERVED	I	10	Reserved pin.
VDD	I	25,26,28,29, 30,46,47,61, 71,72,88,89, 95,96,126,127	Digital Power pins.
GND	I	22,30,31,34, 35,39,40,43, 50,55,56,67, 68,76,77,81, 84,85,92,97, 98,128,129	Digital Ground pins.
AVDD	I	3,6,8,137, 140,144,147, 148,151,152, 155	Analog Power pins.
AGND	I	4,5,7,9,138, 142,143,145, 146,153,154, 158,159	Analog Ground pins.

5. PROGRAMMING INTERFACE

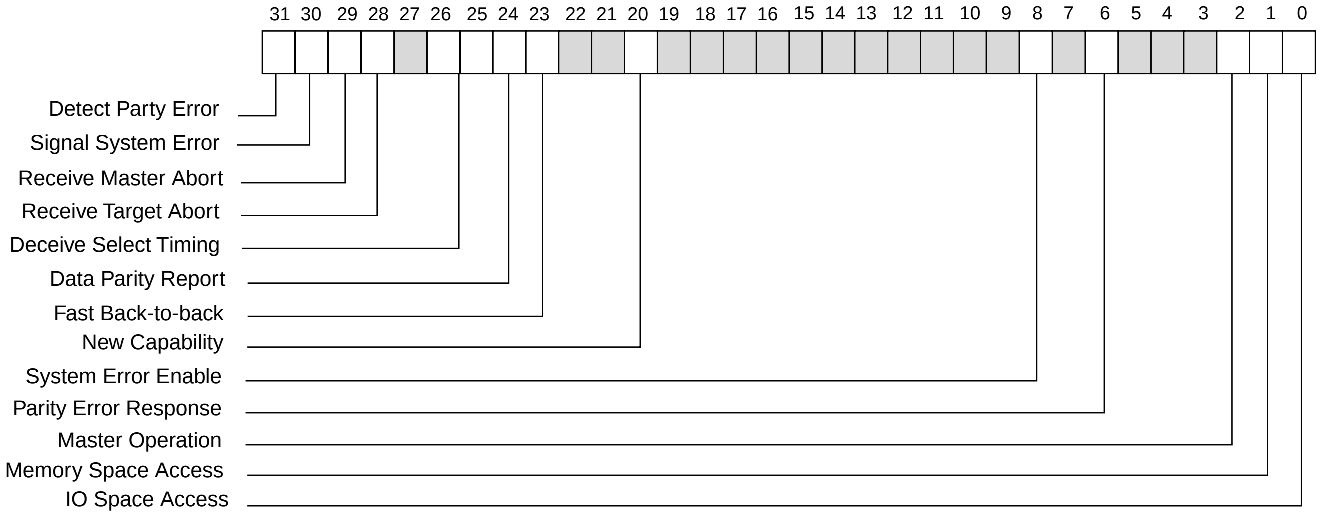
5.1 PCI CONFIGURATION REGISTERS :

5.1.1 PCI ID REGISTER (PFID) (Offset 03h-00h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Device ID (bit 31:16)
Vendor ID (bit 15:0)

This register can be loaded from external serial EEPROM or use a MXIC preset value of "0D9" and "0531" for vendor ID and device ID respectively. Word location 3Eh and 3Dh in serial EEPROM are used to configure customer's vendor ID and device ID respectively. If location 3Eh contains"FFFF" value then MXIC's vendor ID and device ID will be set in this register, otherwise both 3Eh and 3Dh will be loaded into this register from serial EEPROM.

5.1.2 PCI COMMAND AND STATUS REGISTER (PFCS) (Offset 07h-04h)

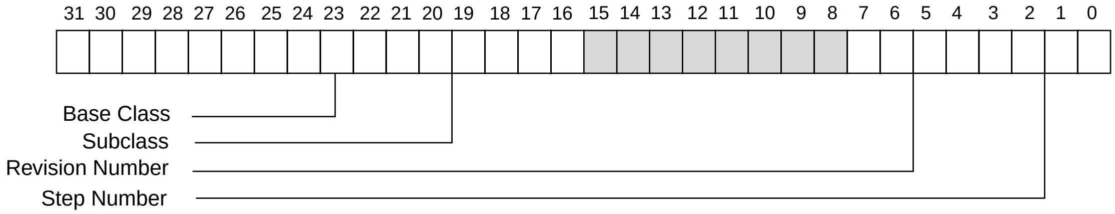

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Detect Party Error
Signal System Error
Receive Master Abort
Receive Target Abort
Deceive Select Timing
Data Parity Report
Fast Back-to-back
New Capability
System Error Enable
Parity Error Response
Master Operation
Memory Space Access
IO Space Access

The bit content will be reset to 0 when a 1 is written to the corresponding bit location.

bit 0 : IO Space Access, set to 1 enable IO access
bit 1 : Memory Space Access, set to 1 to enable memory access
bit 2 : Master Operation, set to 1 to support bus master mode
bit 5-3 : not used
bit 6 : Parity Error Response, set to 1 to enable assertion of CSR<13> bit if parity error detected.
bit 7 : not used
bit 8 : System Error Enable, set to 1 to enable SERR# when parity error is detected on address lines and CBE[3:0].
bit 20 : New capability. Set to support PCI power management.
bit 22-bit19 : not used
bit 23 : Fast Back-to back, always set to accept fast back-to-back transactions that are not sent to the same bus device.

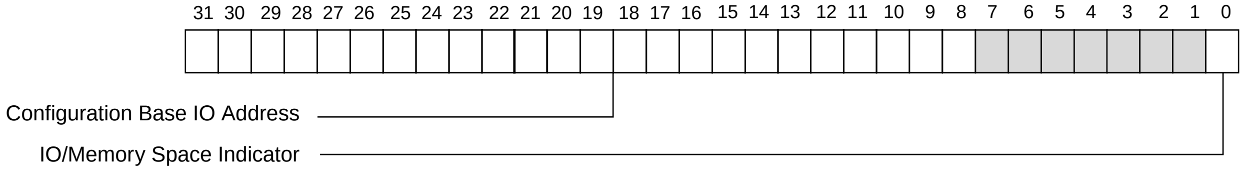
bit 24:Data parity Report, is set to 1 only if PERR# active and PFCS<6> is also set.
bit 26-25:Device Select Timing of DEVSELB pin.
bit 27:not used
bit 28:Receive Target Abort, is set to indicate a transaction is terminated by a target abort.
bit 29:Receive Master Abort, is set to indicate a master transaction with Master abort.
bit 30:Signal System Error, is set to indicate assertion of SERR#.
bit 31:Detected Parity Error, is set whenever a parity error detected regardless of PFCS<6>.

5.1.3 PCI REVISION REGISTER (PFRV) (Offset 0Bh-08h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Base Class
Subclass
Revision Number
Step Number

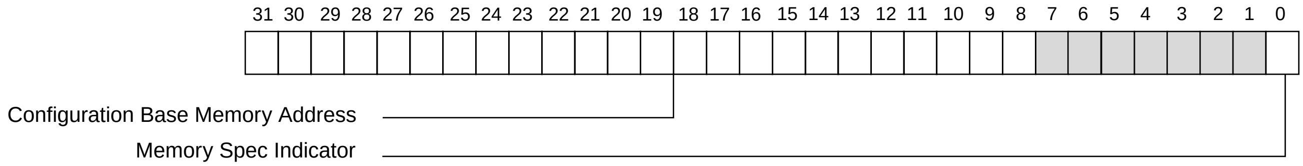
bit 3 - 0 : Step Number, range from 0 to Fh.
bit 7 - 4 : Revision Number, fixed to 3h for MX98725
bit 15 - 8 : not used
bit 23 - 16 : Subclass, fixed to 0h.
bit 31 - 24 : Base Class, fixed to 2h.

5.1.4 PCI BASE IO ADDRESS REGISTER (PBIO) (Offset 13h-10h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Configuration Base IO Address
IO/Memory Space Indicator

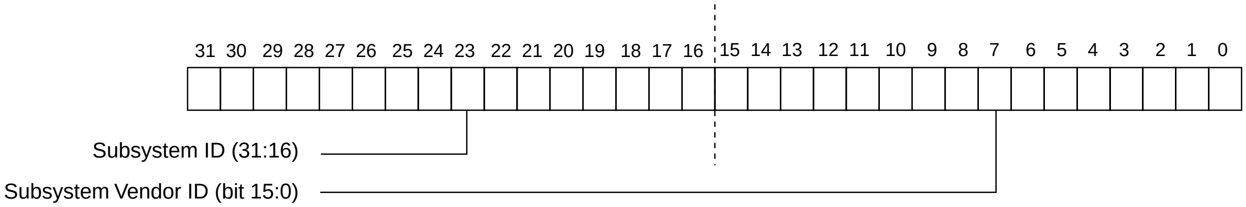
bit 0 : IO/Memory Space Indicator, fixed to 1 in this field will map into the IO space. This is a read only field.
bit 7 - 1 : not used, all 0 when read
bit 31 - 8 : Defines the address assignment mapping of MX98725 CSR registers.

5.1.5 PCI BASE MEMORY ADDRESS REGISTER (PBMA) (Offset 17h-14h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Configuration Base Memory Address
Memory Spec Indicator

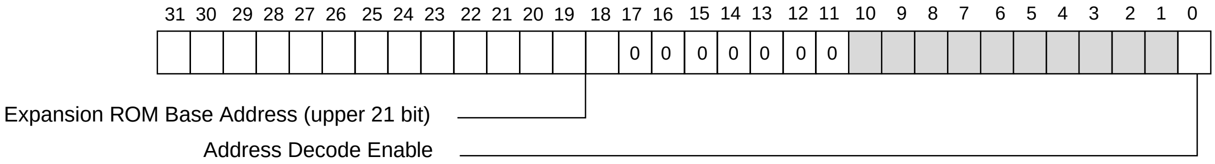
bit 0 : Memory Space Indicator, fixed to 0 in this field will map into the memory space. This is a read only field.
bit 6 - 1 : not used, all 0 when read
bit 31 - 7 : Defines the address assignment mapping of MX98725 CSR registers.

5.1.6 PCI SUBSYSTEM ID REGISTER (PSID) (Offset 2Ch-2Fh)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Subsystem ID (31:16)
Subsystem Vendor ID (bit 15:0)

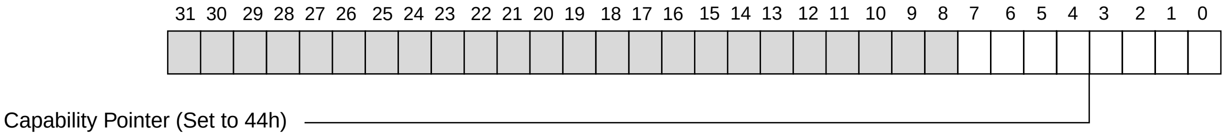
This register is used to uniquely identify the add-on board or subsystem where the NIC controller resides. Values in this register are loaded directly from external serial EEPROM after system reset automatically. Word location 36h of EEPROM is subsystem vendor ID and location 35h is sub-system ID.

5.1.7 PCI BASE EXPANSION ROM ADDRESS REGISTER (PBER) (Offset 33h-30h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 0
Expansion ROM Base Address (upper 21 bit)
Address Decode Enable

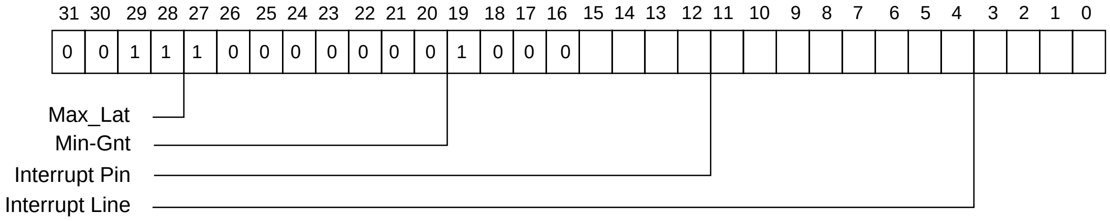
bit 0 : Address Decode Enable, decoding will be enabled if only both enable bit in PFCS<1> and this expansion ROM register are 1.
bit 10 - 1 : not use
bit 31 - 11 : Defines the upper 21 bits of expansion ROM base address.

5.1.8 PCI CAPABILITY POINTER REGISTER (PFCP) (Offset 37h-34h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Capability Pointer (Set to 44h)

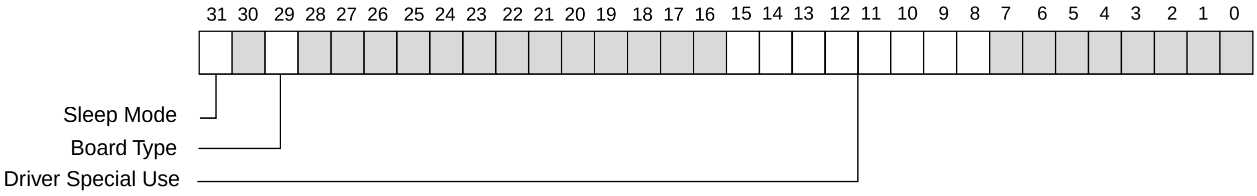
bit 7- 0 : Capability pointer (Cap_Ptr) is set to 44h if PMEB is connected to PCI bus, otherwise 00.
bit 31- 8 : reserved

5.1.9 INTERRUPT REGISTER (PFIT) (Offset 3Fh-3Ch)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 1 1 1 0 0 0 0 0 0 0 1 0 0 0
Max_Lat
Min-Gnt
Interrupt Pin
Interrupt Line

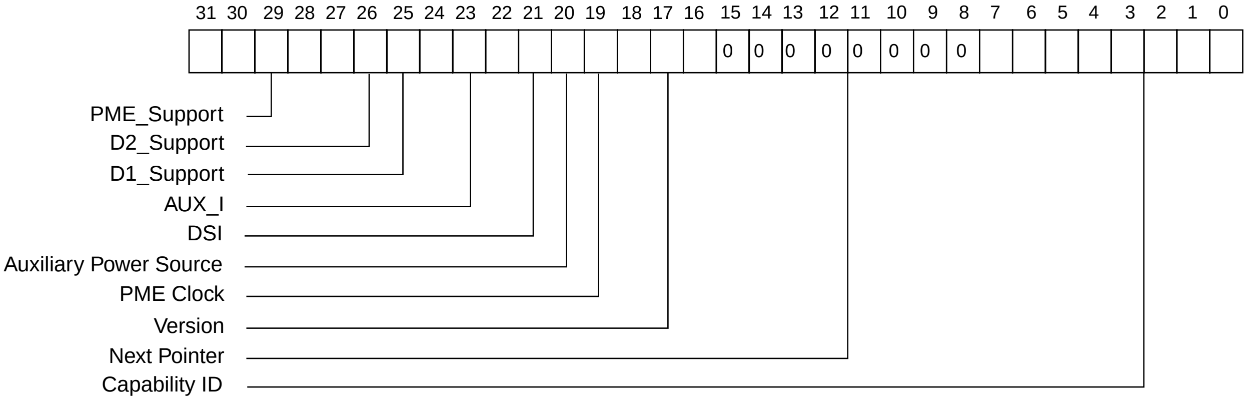
bit 7 - 0 : Interrupt Line, system BIOS will writes the routing information into this field, driver can use this information to determine priority and interrupt vector.
bit 15 - 8 : Interrupt Pin, fixed to 01h which use INTA#.
bit 31 - 24 : Max_Lat which is a maximum period for a access to PCI bus.
bit 23 - 16 : Min_Gnt which is the maximum period that MX98725 needs to finish a brust PCI cycle.

5.1.10 PCI DRIVER AREA REGISTER (PFDA) (43h-40h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Sleep Mode
Board Type
Driver Special Use

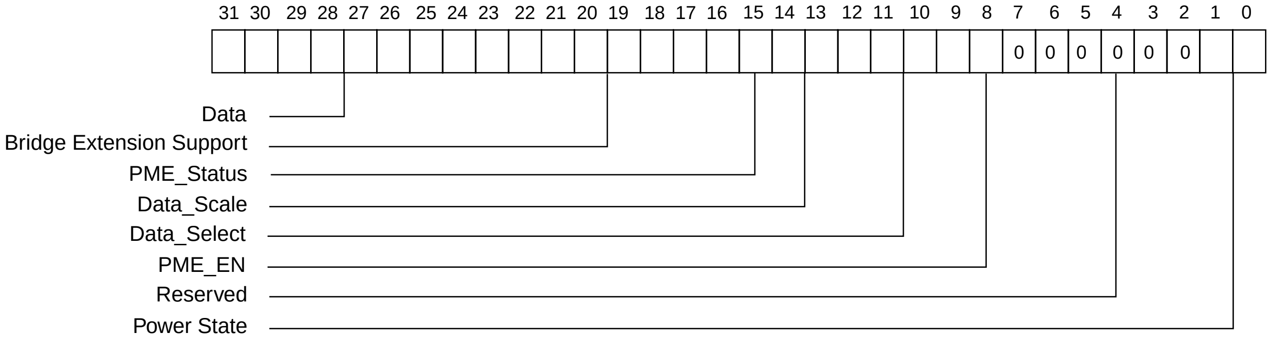
bit 31 : Sleep Mode, set to sleep mode which allows access to PCI configuration space, a hardwarreset or reset to this bit can exit from sleep mode. Magic packet can be received under sleep mode if CSR16<21> (Magic Packet Enable) is set.
bit 30 : not used
bit 29 : board type
bit 15 - 8 : driver is free to read and write this field for any purpose.
bit 7 - 0 : not used.

5.1.11 PCI POWER MANAGEMENT CAPABILITY REGISTER (PPMC) (47h-44h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
PME_Support
D2_Support
D1_Support
AUX_I
DSI
Auxiliary Power Source
PME Clock
Version
Next Pointer
Capability ID

bit 31- 27 : PME_Support, read only indicates the power states in which the function may assert PMEB pin.
bit 31 ---- PME_D3cold (value=1)
bit 30 ---- PME_D3warm
bit 29 ---- PME_D2
bit 28 ---- PME_D1
bit 27 ---- PME_D0
bit 26 : D2 mode support, read only.
bit 25 : D1 mode support, read only.
bit 24-22 : AUX_I bits, Auxiliary Power Reporting, read only.
bit 21 : DSI, read only.
bit 20 : Auxiliary power source, read only.
bit 19 : PME Clock, read only.
bit 18-16 : Version, read only.
bit 15-8 : Next Pointer, read only.
bit 7-0 : Capability ID, read only, a 1 indicates that the data structure currently being pointed to is the PCI power managment data structure.

5.1.13 PCI POWER MANAGEMENT COMMAND AND STATUS REGISTER (PPMCSR) (4Bh-48h)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0
Data
Bridge Extension Support
PME_Status
Data_Scale
Data_Select
PME_EN
Reserved
Power State

bit 1-0 : Power_State, read/write.
bit7-2 : all 0. Reserved.
bit8 : PME_EN, set 1 to enable PMEB. Set 0 to disable PMEB assertion.
bit 12-9 : Data_Select for report in the Data register located at bit 31:24.
bit 14-13 : Data_Scale, read only.
bit 15 : PME_Status independent of the state of PME_EN.
When set, indicates a assertion of PMEB pin. (support D3 cold).
Write 1 to clear the PMEB signal. Write 0, no effect.
bit 21-16 : Reserved.
bit 22 : B2_B3#, B2_B3 support for D3 hot, meaningful only if BPCC_EN = 1, read only.
bit 23 : BPCC_EN, Bus Power/Clock Control Enable, read only.
bit 31-24 : Data, read only.

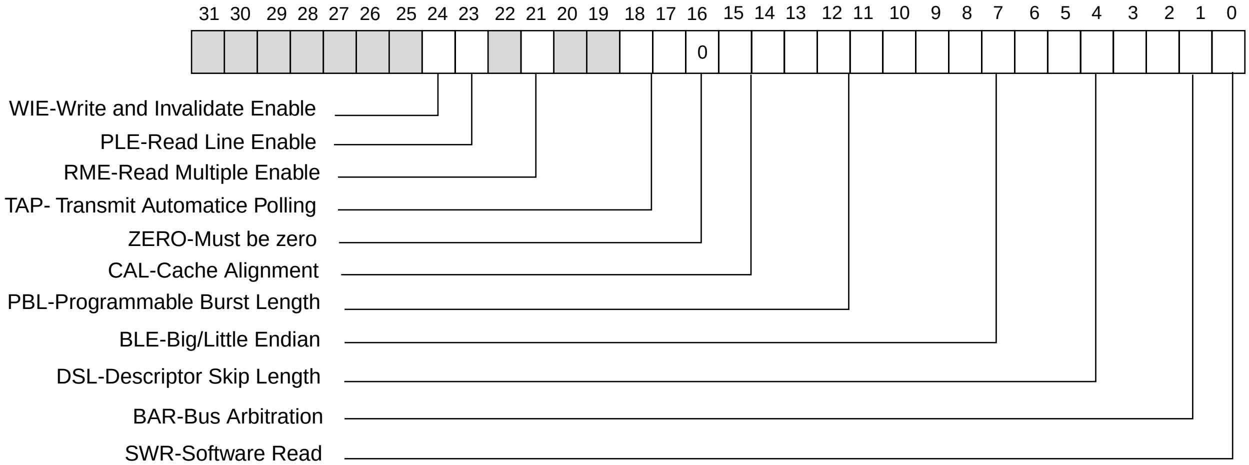
5.2 HOST INTERFACE REGISTERS

MX98725 CSRs are located in the host I/O or memory address space. The CSRs are double word aligned and 32 bits long. Definitions and address for all CSRs are as follows :

CSR Mapping

Register	Meaning	Offset from CSR Base Address (PBIO and PBMA)
CSR0	Bus mode	00h
CSR1	Transmit poll demand	08h
CSR2	Receive poll demand	10h
CSR3	Receive list demand	18h
CSR4	Transmit list base address	20h
CSR5	Interrupt status	28h
CSR6	Operation mode	30h
CSR7	Interrupt enable	38h
CSR8	Missed frame counter	40h
CSR9	Serial ROM and MII management	48h
CSR10	Reserved	50h
CSR11	General Purpose timer	58h
CSR12	10 Base-T status port	60h
CSR13	SIA Reset Register	68h
CSR14	10 Base-T control port	70h
CSR15	Watchdog timer	78h
CSR16	Magic Packet Register	80h
CSR20	NWay Status Register	A0h

5.2.1 BUS MODE REGISTER (CSR0)

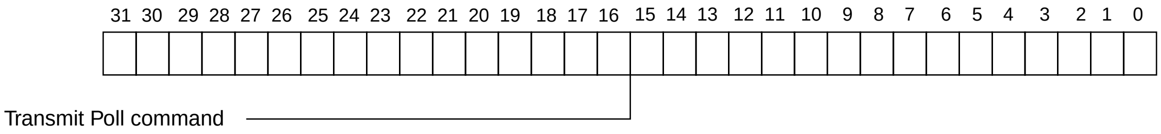

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0
WIE-Write and Invalidate Enable
PLE-Read Line Enable
RME-Read Multiple Enable
TAP- Transmit Automatice Polling
ZERO-Must be zero
CAL-Cache Alignment
PBL-Programmable Burst Length
BLE-Big/Little Endian
DSL-Descriptor Skip Length
BAR-Bus Arbitration
SWR-Software Read

Field	Name	Description
0	SWR	Software Reset, when set, MX98725 resets all internal hardware with the exception of the configuration area and port selection.
1	BAR	Internal bus arbitration scheme between receive and transmit processes. The receive channel usually has higher priority over transmit channel when receive FIFO is partially full to a threshold. This threshold can be selected by programming this bit. Set for lower threshold, reset for normal threshold.
6:2	DSL	Descriptor Skip Length, specifies the number of longwords to skip between two descriptors.
7	BLE	Big/Little Endian, set for big endian byte ordering mode, reset for little endian byte ordering mode, this option only applies to data buffers
13:8	PBL	Programmable Burst Length, specifies the maximum number of longwords to be transferred in one DMA transaction. default is 0 which means unlimited burst length, possible values can be 1,2,4,8,16,32 and unlimited .
15:14	CAL	Cache Alignment, programmable address boundaries of data burst stop, MX98725 can handle non-cache- aligned fragement as well as cache-aligned fragment efficiently.18:17 TAP Transmit Auto-Polling time interval, defines the time interval for MX98725 to performs transmit poll command automatically at transmit suspended state.
21	RME	PCI Memory Read Multiple command enable, indicates bus master may intend to fetch more than one cache lines disconnecting.
23	RLE	PCI Memory Read Line command enable, indicating bus master intends to fetch a complete cache line.
24	WIE	PCI Memory Write and Invalidate command enable, guarantees a minimum transfer of one complete cache line.

TABLE 5.2.0 TRANSMIT AUTO POLLING BITS

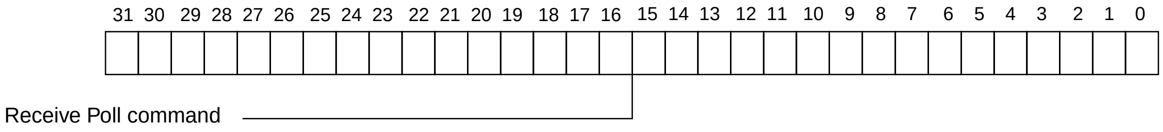
CSR<18:17>	Time Interval
00	No transmit auto-polling, a write to CSR1 is required to poll
01	auto-poll every 200 us
10	auto-poll every 800 us
11	auto-poll every 1.6 ms

5.2.2 TRANSMIT POLL COMMAND (CSR1)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Transmit Poll command

Field	Name	Description
31:0	TPC	Write only, when written with any value, MX98725 read transmit descriptor list in host memory pointed by CSR4 and processes the list.

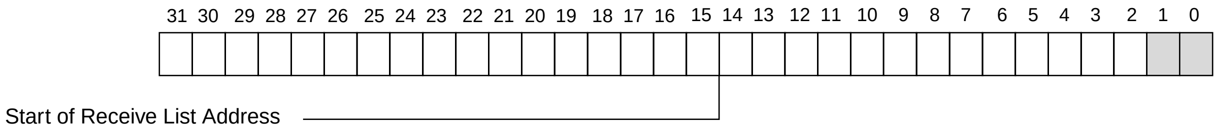
5.2.3 RECEIVE POLL COMMAND (CSR2)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Receive Poll command

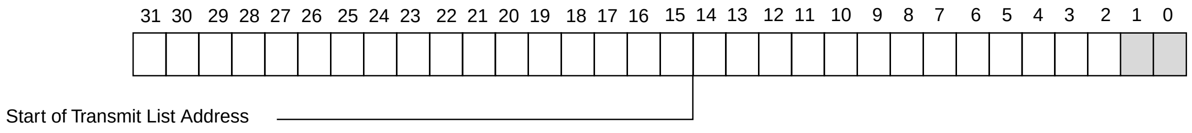
Field	Name	Description
31:0	RPC	Write only, when written with any value, MX98725 read receive descriptor list in host memory pointed by CSR4 and processes the list.

5.2.4 DESCRIPTOR LIST ADDRESS (CSR3, CSR4)

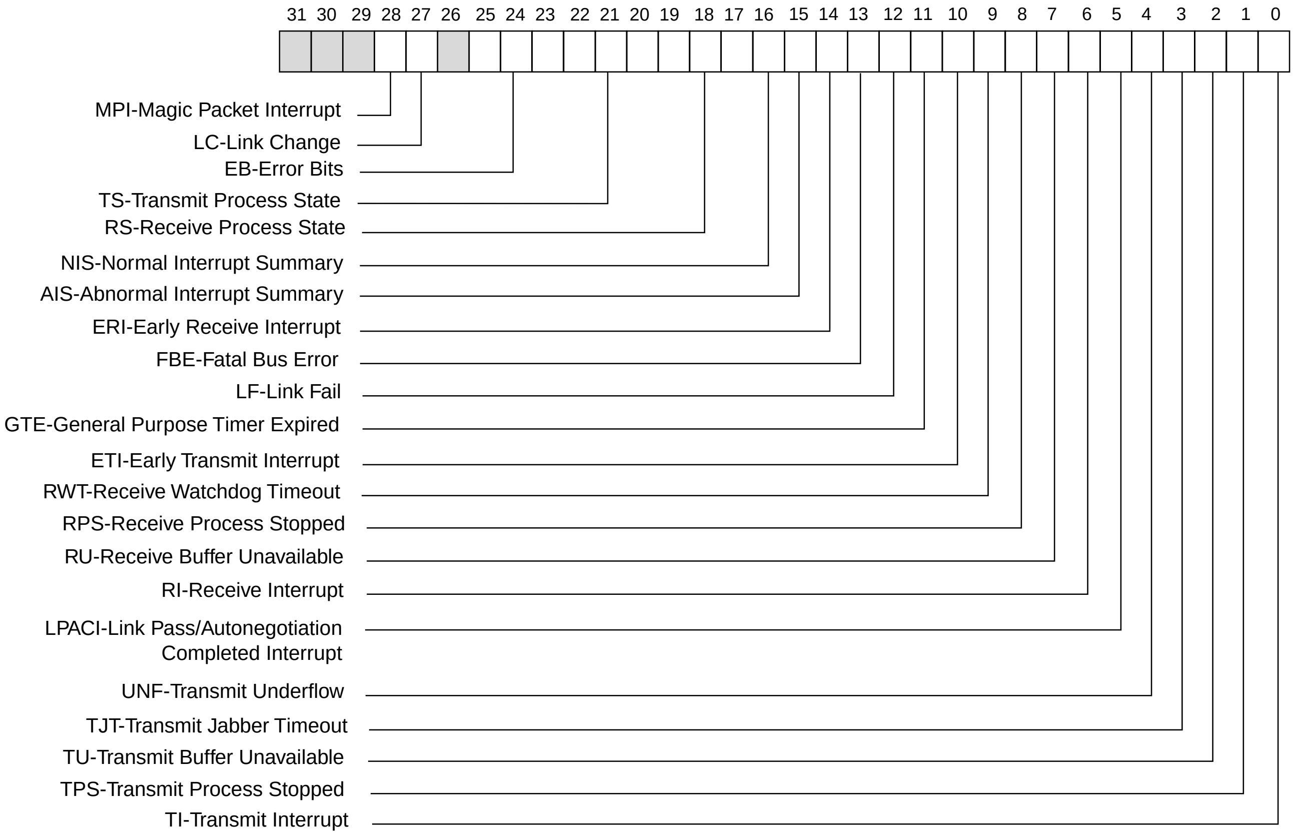
CSR3 Receive List Base Address


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Start of Receive List Address

CSR4 Transmit List Base Address


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Start of Transmit List Address

5.2.5 STATUS REGISTER (CSR5)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MPI-Magic Packet Interrupt
LC-Link Change
EB-Error Bits
TS-Transmit Process State
RS-Receive Process State
NIS-Normal Interrupt Summary
AIS-Abnormal Interrupt Summary
ERI-Early Receive Interrupt
FBE-Fatal Bus Error
LF-Link Fail
GTE-General Purpose Timer Expired
ETI-Early Transmit Interrupt
RWT-Receive Watchdog Timeout
RPS-Receive Process Stopped
RU-Receive Buffer Unavailable
RI-Receive Interrupt
LPACI-Link Pass/Autonegotiation Completed Interrupt
UNF-Transmit Underflow
TJT-Transmit Jabber Timeout
TU-Transmit Buffer Unavailable
TPS-Transmit Process Stopped
TI-Transmit Interrupt

Field	Name	Description
28	MPI	Magic packet received interrupt. Valid only if CSR16<22> bit is set.
27	LC	100 Base-TX link status has changed either from pass to fail or fail to pass. Read CSR12<1> for 100 Base-TX link status.
25:23	EB	Error Bits, read only, indicating the type of error that casued fatal bus error.
22:20	TS	Transmit Process State, read only bits indicating the state of transmit process.
19:17	RS	Receive Process State, read only bits indicating the state of receive process.
16	NIS	Normal Interrupt Summary, is the logical OR of CSR5<0>, CSR5<2> and CSR5<6> and CSR5<28>.
15	AIS	Abnormal Interrupt Summary, is the logical OR of CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CAR5,10>, CSR5<11> and CSR5<13>, CSR5<27>.
14	ERI	Early receive interrupt, indicating the first buffer has been filled in ring mode, or 64 bytes has been received in chain mode.
13	FBE	Fatal Bus Error, indicating a system error occured, MX98725 will disable all bus access.
12	LF	Link Fail, indicates a link fail state in 10 Base-T port. This bit is valid only when CSR6<18>=0, CSR14<8>=1, and CSR13<3>=0.
11	GTE	General Purpose Timer Expired, indicating CSR11 counter has expired.

Field	Name	Description
10	ETI	Early Transmit Interrupt, indicating the packet to be transmitted was fully transferred to internal TX FIFO. CSR5<0> will automatically clears this bit.
9	RWT	Receive Watchdog Timeout, reflects the network line status where receive watchdog timer has expired while the other node is still active on the network.
8	RPS	Write only, when written with any value, MX98725 reads receive descriptor list in host memory pointed by CSR4 and processes the list.
7	RU	Receive Buffer Unavailable, the receive process is suspended due to the next descriptor in the receive list is owned by host. If no receive poll command is issued, the reception process resumes when the next recognized incoming frame is received.
6	RI	Receive Interrupt, indicating the completion of a frame reception.
5	UNF	Transmit Underflow, indicating transmit FIFO has run empty before the completion of a packet transmission.
4	LPANCI	When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10Base-T link integrity test has completed successfully, after the link was down. This bit is also set as as a result of writing 0 to CSR14<12> (Link Test Enable). When Autonegotiation is enabled (CSR14<7> =1) , this bit indicates that the autonegotiation has completed (CSR12<14:12>=5). CSR12 should then be read for a link status report. This bit is only valid when CSR6<18>=0, i.e. 10 Base-T port is selected Link Fail interrupt (CSR5<12>) will automatically clears this bit.
3	TJT	Transmit Jabber Timeout, indicating the MX98725 has been excessively active. The transmit process is aborted and placed in the stopped state. TDES0<1> is also set.
2	TU	Transmit Buffer Unavailable, transmit process is suspended due to the next descriptor in the transmit list is owned by host.
1	TPS	Transmit Process Stopped.
0	TI	Transmit Interrupt. indicating a frame transmission was completed.

TABLE 5.2.1 FATAL BUS ERROR BITS

CSR5<25:23>	Process State
000	parity error for either SERR# or PERR#, cleared by software reset.
001	master abort
010	target abort
011	reserved
1XX	reserved

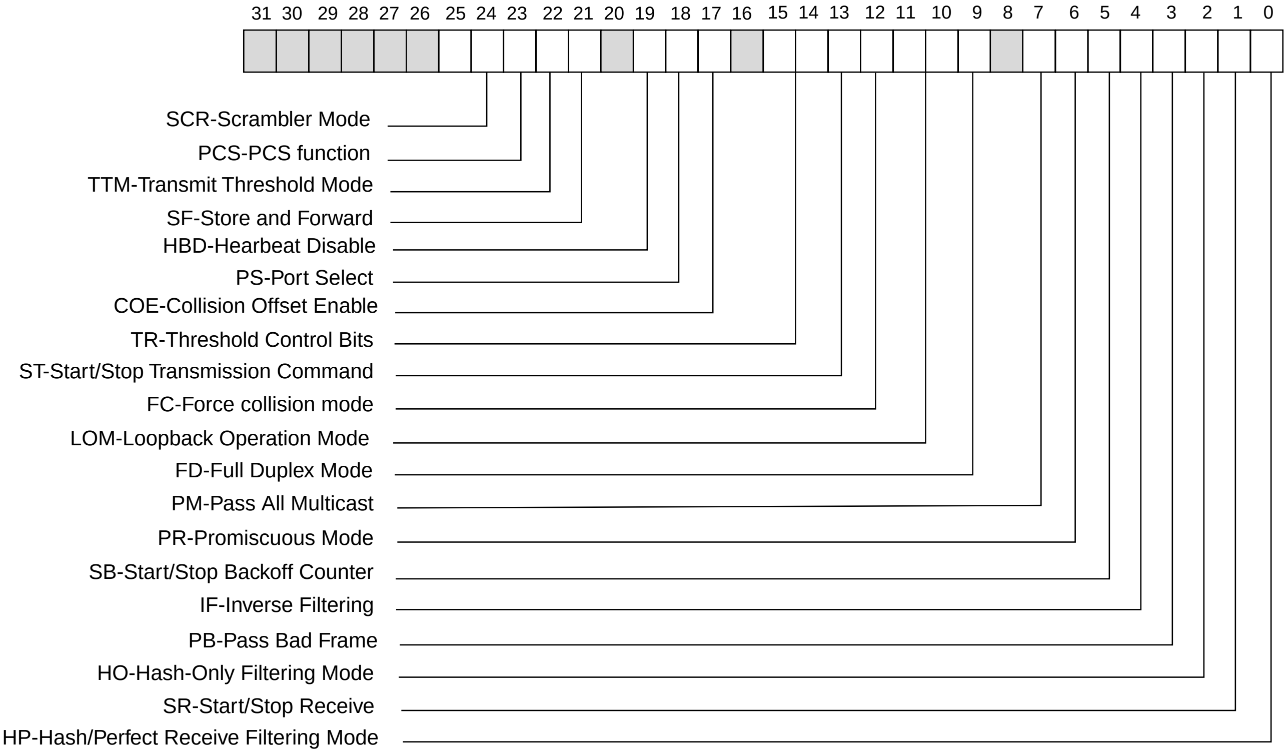
TABLE 5.2.2 TRANASMIT PROCESS STATE

CSR5<22:20>	Process State
000	Stopped- reset or transmit jabber expired.
001	Fetching transmit descriptor
010	Waiting for end of transmission
011	filling transmit FIFO
100	Reserved
101	Setup packet
110	Suspended, either FIFO underflow or unavailable transmit descriptor
111	Closing transmit descriptor

TABLE 5.2.3 RECEIVE PROCESS STATE

CSR5<19:17>	Process State
000	Stopped- reset or stop receive command Fetching receive descriptor
010	Checking for end of receive packet
011	Waiting for receive packet
100	Suspended, receive buffer unavailable
101	Closing receive descriptor
110	Purging the current frame from the receive FIFO due to unavailable receive buffer
111	Queuing the receive frame from the receive FIFO into host receive buffer

5.2.6 OPERATION MODE REGISTER (CSR6)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SCR-Scrambler Mode
PCS-PCS function
TTM-Transmit Threshold Mode
SF-Store and Forward
HBD-Hearbeat Disable
PS-Port Select
COE-Collision Offset Enable
TR-Threshold Control Bits
ST-Start/Stop Transmission Command
FC-Force collision mode
LOM-Loopback Operation Mode
FD-Full Duplex Mode
PM-Pass All Multicast
PR-Promiscuous Mode
SB-Start/Stop Backoff Counter
IF-Inverse Filtering
PB-Pass Bad Frame
HO-Hash-Only Filtering Mode
SR-Start/Stop Receive
HP-Hash/Perfect Receive Filtering Mode

Field	Name	Description
24	SCR	Scrambler Mode, default is set to enable scrambler function. Not affected by software reset.
23	PCS	Default is set to enable PCS functions. CSR6<18> must be set in order to operate in symbol mode.
22	TTM	Transmit Threshold Mode, set for 10 Base-T and reset for 100 Base-TX.
21	SF	Store and Forward, when set, transmission starts only if a full packet is in transmit FIFO. the threshold values defined in CSR6<15:14> are ignored
19	HBD	Heartbeat Disable, set to disable SQE function in 10 Base-T mode.
18	PS	Port Select, deafult is o which is 10 Base-T mode, set for 100 Base-TX mode. A software reset does not affect this bit.
17	COE	Collision Offset Enable, set to enable a modified backoff algorithm during low collision situation, reset for normal backoff algorithm.
15:14	TR	Threshold Control Bits, these bits controls the selected threshold level for MX98725's transmit FIFO, transmission starts when frame size within the transmit FIFO is larger than the selected threshold. Full frames with a length less than the threshold are also transmitted.
13	ST	Start/Stop Transmission Command, set to place transmission process in running state and will try to transmit current descriptor in transmit list. When reset, transmit process is placed in stop state.

Field	Name	Description
12	FC	Force Collision Mode, used in collision logic test in internal loopback mode, set to force collision during next transmission attempt. This can result in excessive collision reported in TDES0<8> if 16 or more collision.
11:10	LOM	Loopback Operation Mode, see table.
9	FD	Full-Duplex Mode, set for simultaneous transmit and receive operation, heartbeat check is disabled, TDES0<7> should be ignored, and internal loopback is not allowed. This bit controls the value of bit 6 of link code word .
7	PM	Pass All Multicast, set to accept all incoming frames with a multicast des tination address are received. Incoming frames with physical address are filtered according to the CSR6<0> bit.
6	PR	Promiscuous Mode, any incoming valid frames are accepted, default is reset and not affected by software reset.
5	SB	Start/Stop Backoff Counter, when reset, the backoff timer is not affected by the network carrier activity. Otherwise, timer will start counting when carrier drops.
4	IF	Inverse Filtering, read only bit, set to operate in inverse filtering mode, only valid during perfect filtering mode.
3	PB	Pass Bad Frames, set to pass bad frame mode, all incoming frames passed the address filtering are accepted including runt frames, collided fragments, truncated frames caused by FIFO overflow.
2	HO	Hash-Only Filtering Mode , read only bit, set to operate in imperfect filtering mode for both physical and multicast addresses.
1	SR	Start/Stop Receive, set to place receive process in running state where descriptor acquisition is attempted from current position in the receive list. Reset to place the receive process in stop state.
0	HP	Hash/Perfect Receive Filtering Mode, read only bit, set to use hash table to filter multicast incoming frames. If CSR6<2> is also set, then the physical adresses are imperfect address filtered too. If CSR6<2> is reset, then physical addresses are perfect address filtered, according to a single physical address as specified in setup frame.

TABLE 5.2.4 TRANSMIT THRESHOLD

CSR6<21>	CSR6<15:14>	CSR6<22>=0	CSR6<22>=1 (Threshold bytes)
		(for 100 Base-TX)	(for 10 Base-T)
0	00	128	72
0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	(Store and Forward)	

TABLE 5.2.5 DATA PORT SELECTION

CSR14<7>	CSR6<18>	CSR6<22>	CSR6<23>	CSR6<24>	Port
1	0	X	X	X	Nway Auto-negociation
0	0	1	X	X	10 Base-T
0	1	0	1	1	100 Base-TX

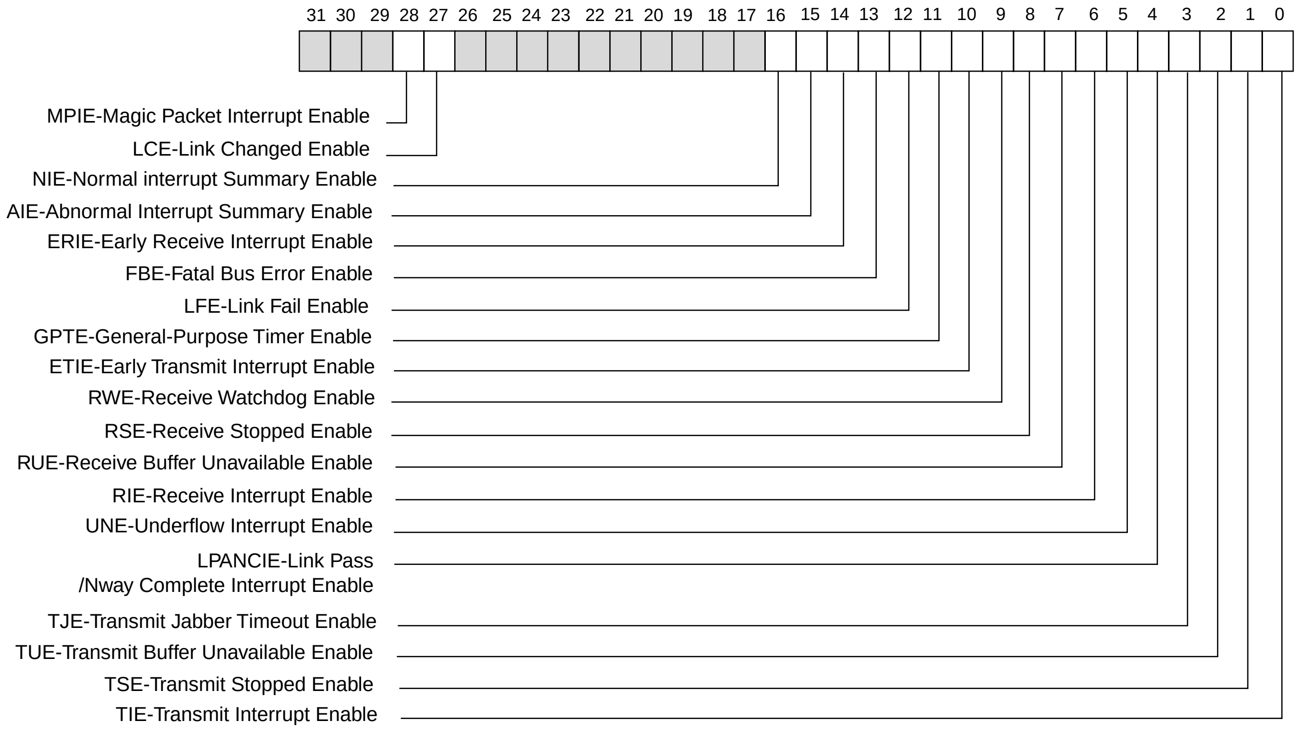
TABLE 5.2.6 LOOPBACK OPERATION MODE

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback at FIFO port
11	Internal loopback at the PHY level
10	External loopback at the PMD level

TABLE 5.2.7 FILTERING MODE

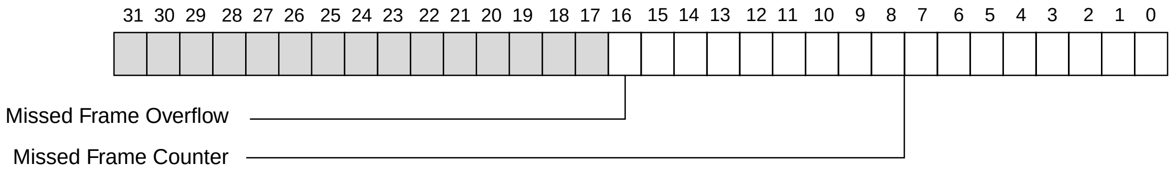
CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering
0	0	0	1	1	512-bit hash for multicast and phyical addresses
0	0	1	0	0	Inverse filtering
X	1	0	X	X	Promiscuous
1	0	0	X	X	Pass All Multicast

5.2.7 INTERRUPT MASK REGISTER (CSR7)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MPIE-Magic Packet Interrupt Enable
LCE-Link Changed Enable
NIE-Normal interrupt Summary Enable
AIE-Abnormal Interrupt Summary Enable
ERIE-Early Receive Interrupt Enable
FBE-Fatal Bus Error Enable
LFE-Link Fail Enable
GPTE-General-Purpose Timer Enable
ETIE-Early Transmit Interrupt Enable
RWE-Receive Watchdog Enable
RSE-Receive Stopped Enable
RUE-Receive Buffer Unavailable Enable
RIE-Receive Interrupt Enable
UNE-Underflow Interrupt Enable
LPANCIE-Link Pass /Nway Complete Interrupt Enable
TJE-Transmit Jabber Timeout Enable
TUE-Transmit Buffer Unavailable Enable
TSE-Transmit Stopped Enable
TIE-Transmit Interrupt Enable

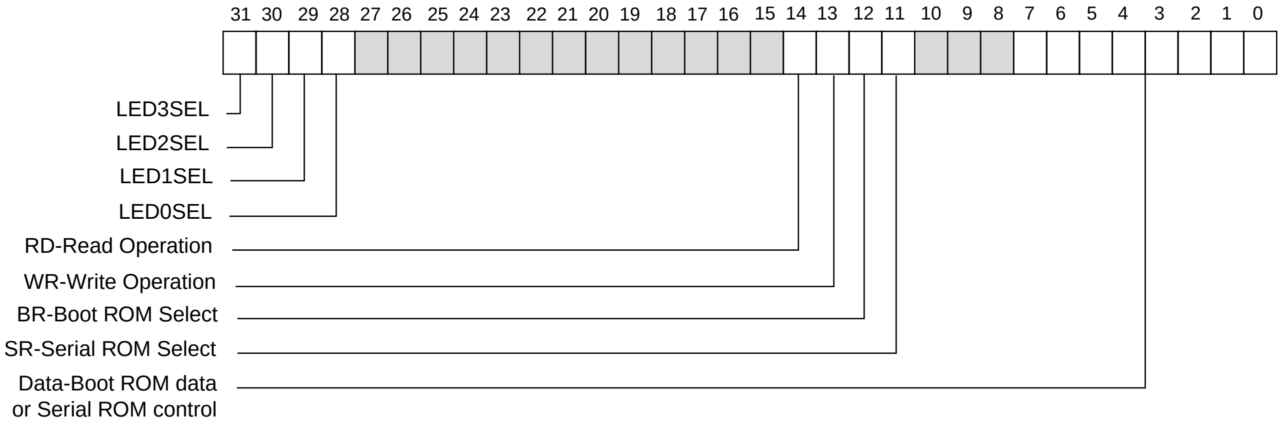
Field	Name	Description
28	MPIE	Magic Packet Interrupt Enable, enables CSR5<28>.
27	LCE	Link Changed Enable, enables CSR5<27>.
16	NIE	Normal Interrupt Summary Enable, set to enable CSR5<0>, CSR5<2>, CSR5<6>.
15	AIE	Abnormal Interrupt Summary enable, set to enbale CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
14	ERIE	Early Receive Interrupt Enable
13	FBE	Fatal Bus Error Enable, set together with with CSR7<15> enables CSR5<13>.
12	LFE	Link Fail Interrupt Enable, enables CSR5<12>
11	GPTE	General_-Purpose Timer Enable, set together with CSr7<15> enables CSR5<11>.
10	ETIE	Early Transmit Interrupt Enable, enables CSR5<10>
9	RWE	Receive Watchdog Timeout Enable, set together with CSR7<15> enables CSR5<9>.
8	RSE	Receive Stopped Enable, set together with CSR7<15> enables CSR5<8>.
7	RUE	Receive Buffer Unavailable Enable, set together with CSR7<15> enables CSR5<7>.
6	RIE	Receive Interrupt Enable, set together with CSR7<16> enables CSR5<6>.
5	UNE	Underflow Interrupt Enable, set together with CSR7<15> enables CSR5<5>.
4	LPANCIE	Link Pass/Autonegotiation Completed Interrupt Enable
3	TJE	Transmit Jabber Timeout Enable, set together with CSR7<15> enables CSR5<3>.
2	TUE	Transmit Buffer Unavailable Enable, set together with CSR7<16> enables CSR5<2>.
1	TSE	Transmit Stop Enable, set together with CSR7<15> enables CSR5<1>.
0	TIE	Transmit Interrupt Enable, set together with CSR7<16> enables CSr5<0>.

5.2.8 MISSED FRAME COUNTER (CSR8)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Missed Frame Overflow
Missed Frame Counter

Field	Name	Description
16	MFO	Missed Frame Overflow, set when missed frame counter overflows, reset when CSR8 is read.
15:0	MFC	Missed Frame Counter, indicates the number of frames discarded because no host receive descriptors were available.

5.2.9 NON-VOLATILE MEMORY CONTROL REGISTER (CSR9)

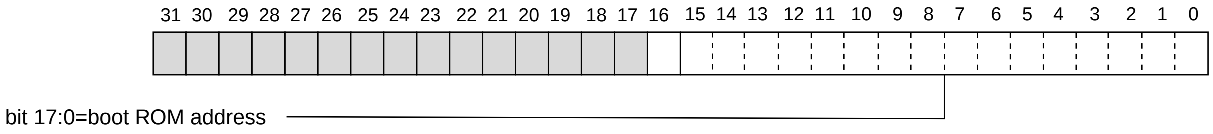

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LED3SEL
LED2SEL
LED1SEL
LED0SEL
RD-Read Operation
WR-Write Operation
BR-Boot ROM Select
SR-Serial ROM Select
Data-Boot ROM data
or Serial ROM control

Field	Name	Description
31	LED3SEL	0:Default value. Set LED3 as RX LED. 1: Set LED3 as Full/Half duplex LED.
30	LED2SEL	0:Default value. Set LED2 as Link Speed (10/100) LED. 1: Set LED2 as Collision LED.
29	LED1SEL	0:Default value. Set LED1 as Good Link LED. 1: Set LED1 as Link/Activity LED.
28	LED0SEL	0:Default value. Set LED0 as Activity LED. 1: Set LED0 as Link Speed (10/100) LED.
14	RD	Boot ROM/EEPROM read operation select bit.

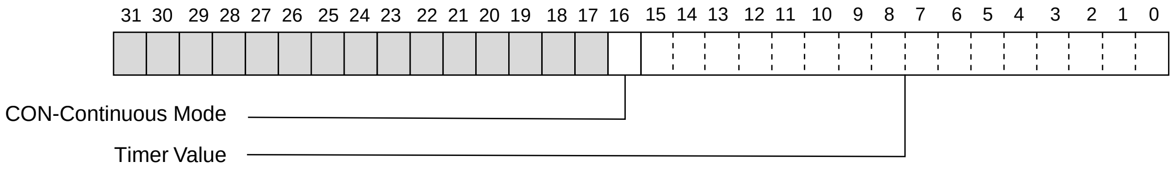
Field	Name	Description
13	WR	Boot ROM/EEPROM write operation select bit. Operation definition: RD WR Operation 1 0 Boot ROM/EEPROM Read 0 1 Boot ROM/EEPROM Write 1 1 EEPROM re-load operation (SR=1) If RD=1 and WR=1, then a EEPROM re-load operation is enabled, the entire content of boot ROM will be reloaded just like the auto-load function after power-up or hardware reset.
12	BR	Boot ROM Select, set to select boot ROM only if CSR9<11>=0.
11	SR	Serial ROM Select, set to select serial ROM for either read or write operation.
7:0	Data	If boot ROM is selected (CSR9<12> is set), this field contains the data to be read from and written to the boot ROM. If serial ROM is selected, CSR9<3:0> are defined as follows: 3 SDO Serial ROM data out from serial ROM into MX98715/MX98725. 2 SDI Serial ROM data input to serial ROM from MX98715/MX98725. 1 SCLK Serial clock output to serial ROM. 0 SCS Chip select output to serial ROM.

Warning : CSR9<11> and CSR9<12> should be mutually exclusive for correct operations.

5.2.10 FLASH MEMORY PROGRAMMING ADDRESS REGISTER (CSR10)

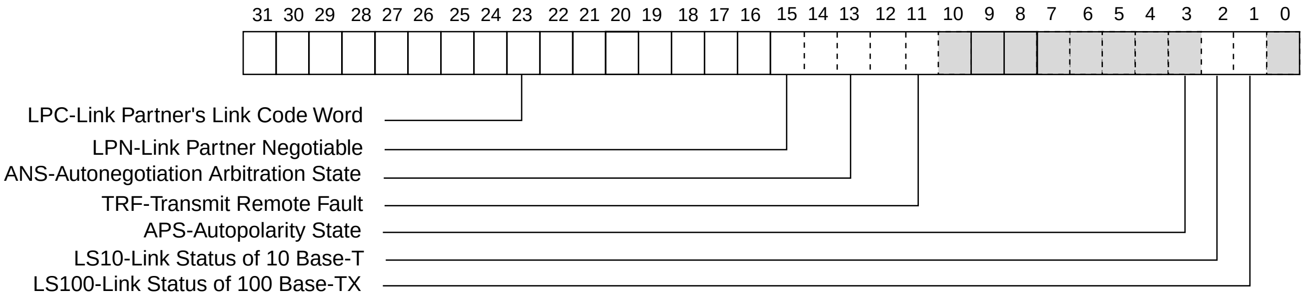

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
bit 17:0=boot ROM address

5.2.11 GENERAL PURPOSE TIMER (CSR11)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
CON-Continuous Mode
Timer Value

Field	Name	Description
16	CON	When set,the general purpose timer is in continuous operating mode. When reset, the timer is in one-shot mode.
15:0	Timer	Value contains the timer value in a cycle time of 204.8us.

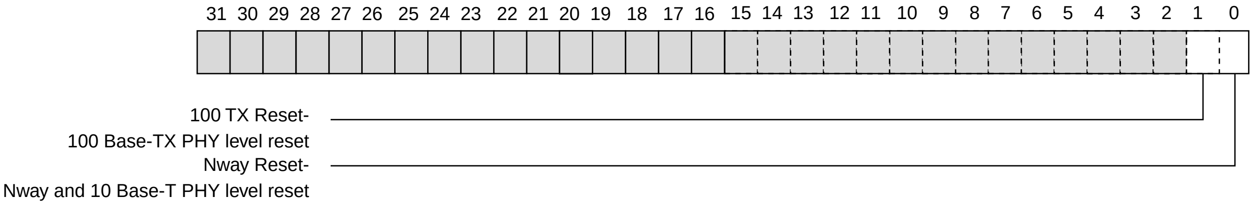
5.2.12 10 BASE-T STATUS PORT (CSR12)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LPC-Link Partner's Link Code Word
LPN-Link Partner Negotiable
ANS-Autonegotiation Arbitration State
TRF-Transmit Remote Fault
APS-Autopolarity State
LS10-Link Status of 10 Base-T
LS100-Link Status of 100 Base-TX

*Software reset has no effect on this register

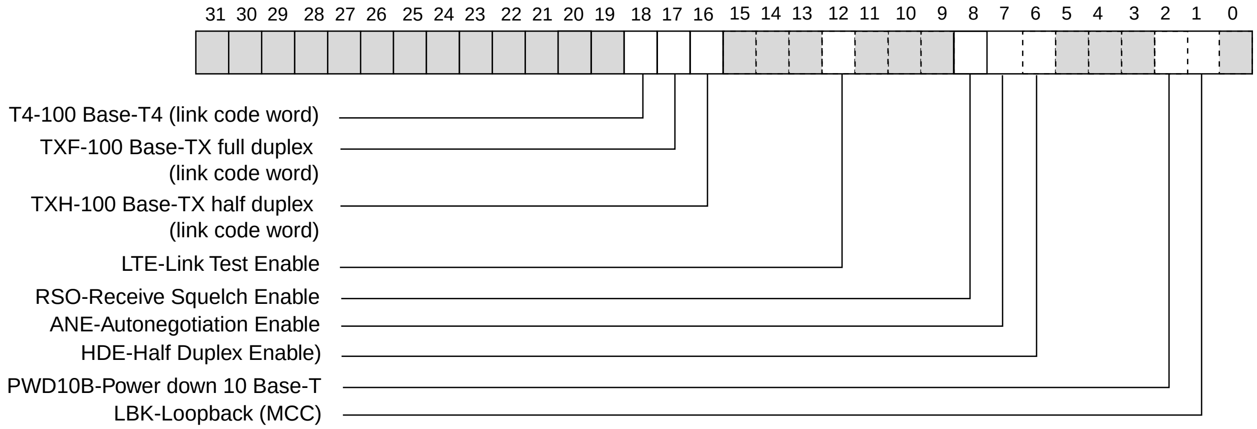
Field	Name	Decription
31:16	LPC	Link Partner's Link Code Word, where bit 16 is S0 (selector field bit 0) and bit 31 is NP (Next Page). Effective only when CSR12<15> is read as a logical 1. the following field.
15	LPN	Link Partner Negotiable, set when link partner support NWAY algorithm and CSR14<7> is set.
14:12	ANS	Autonegotiation Arbitration State, arbitration states are defined 000 = Autonegotiation disable 001 = Transmit disable 010 = ability detect 011 = Acknowledge detect 100 = Complete acknowledge detect 101 = FLP link good; autonegotiation complete 110 = Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated, write 001 into this field can restart the autonegotiation sequence if CSR14<7> is set. Otherwise, these bits should be 0.
11	TRF	Transmit Remote Fault
3	APS	Autopolarity State, set when polarity is positive. When reset, the 10Base-T polarity is negative. The received bit stream is inverted by the receiver.
2	LS10	Set when link status of 10 Base-T port link test fail. Reset when 10 Base-T link test is in pass state.
1	LS100	Link state of 100 Base-TX, this bit reflects the state of SD pin, effective only when CSR6<23>= 1 (PCS is set). Set to indicate a fail condition .i.e. SD=0.

5.2.13 SIA RESET REGISTER (CSR13)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
100 TX Reset-
100 Base-TX PHY level reset
Nway Reset-
Nway and 10 Base-T PHY level reset

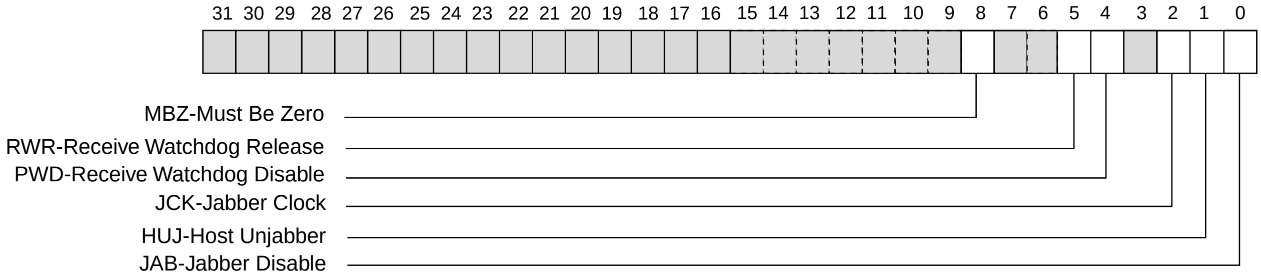
Field	Name	Decription
0	Nway Reset	While writing 0 to this bit, resets the CSR12 & CSR14.
1	100Base-TX	Reset Write a 1 will reset the internal 100 Base-TX PHY module .

5.2.14 10 BASE-T CONTROL PORT (CSR14)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
T4-100 Base-T4 (link code word)
TXF-100 Base-TX full duplex (link code word)
TXH-100 Base-TX half duplex (link code word)
LTE-Link Test Enable
RSO-Receive Squelch Enable
ANE-Autonegotiation Enable
HDE-Half Duplex Enable)
PWD10B-Power down 10 Base-T
LBK-Loopback (MCC)

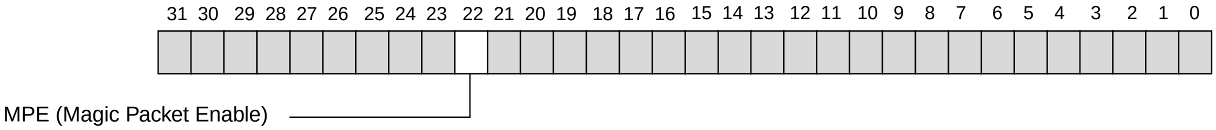
Field	Name	Decription
18	T4	Bit 9 of link code word for T4 mode.
17	TXF	Bit 8 of link code word for 100 Base-TX full duplex mode.
16	TXH	Bit 7 of link code word for 100 Base-TX half duplex mode. Meaningful only when CSR14<7> (ANE) is set.
12	LTE	Link Test Enable, when set the 10 Base-T port link test function is enabled.
8	RSQ	Receive Squelch Enable for 10 Base-T port. Set to enable.
7	ANE	Autonegotiation Enable, .
6	HDE	Half-Duplex Enable, this is the bit 5 of link code word, only meaningful when CSR14<7> is set.
2	PWD10B	Reset to power down 10 Base-T module, this will force both TX and RX port into tri-state and prevent AC current path. Set for normal 10 Base T operation.
1	LBK	Loop back enable for 10 Base-T MCC.

5.2.15 WATCHDOG TIMER (CSR15)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MBZ-Must Be Zero
RWR-Receive Watchdog Release
PWD-Receive Watchdog Disable
JCK-Jabber Clock
HUJ-Host Unjabber
JAB-Jabber Disable

Field	Name	Description
5	RWR	Defines the time interval no carrier from receive watchdog expiration until reenabling the receive channel. When set, the receive watchdog is release 40-48 bit times from the last carrier deassertion. When reset, the receive watchdog is released 16 to 24 bit times from the last carrier deassertion.
4	RWD	When set, the receive watchdog counter is disable. When reset, receive carriers longer than 2560 bytes are guaranted to cause the watchdog counter to time out. Packets horter than 2048 bytes are guaranted to pass.
2	JCK	When set, transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted, When reset, transmission for the 10 Base-T port is cut off after a range of 26 ms to 33ms. When reset, transmission for the 100 Base-TX port is cut off after a range of 2.6ms to 3.3ms.1
1	HUJ	Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the jabber is released 365ms to 420 ms after jabber expiration for 10 Base-T port. When reset, the jabber is released 36.5ms to 42ms after the jabber exporation for 100 Base-TX port.
0	JBD	Jabber Disable, set to disable transmit jabber function.

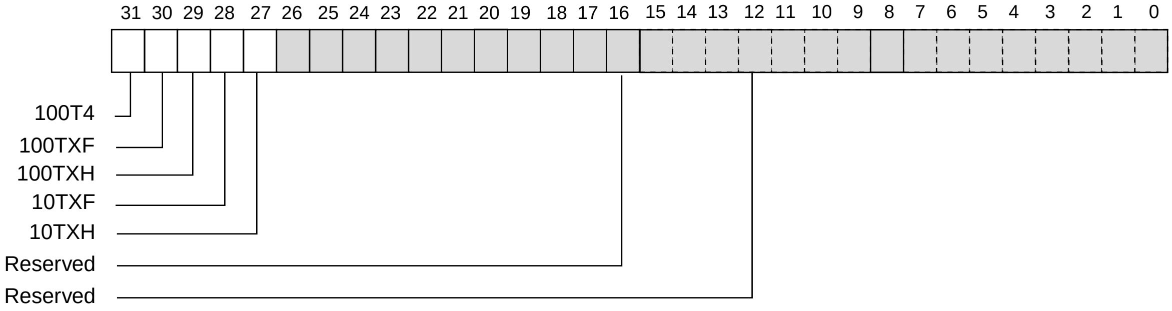
5.2.16 MAGIC PACKET REGISTER (CSR16)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MPE (Magic Packet Enable)

Field	Name	Description
bit 31:23	reserved	
bit 22	MPE	Magic Packet Enable, set to enable Magic Packet Mode
bit 21:0	reserved	

Sleep mode and MPE mode can be used seperately. When Sleep and MPE are both set, the Sleep mode dominate MPE, i.e., no magic packet can be detected since both TX and RX channel are shut off in sleep mode. On the detection of magic packet, a negative pulse will be asserted on PME# pin on PCI bus, LANWAKE pin will be asserted high and EXSTART# pin is driven low and stay low even after PCI reset is asserted. EXSTART# pin can be reset by device driver.

5.2.17 NWAY STATUS REGISTER (CSR20)


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
100T4
100TXF
100TXH
10TXF
10TXH
Reserved
Reserved

Field	Name	Description
31	T4	T4 mode is accepted, read only
30	100TXF	100Base-TX full duplex is accepted, read only
29	100TXH	100Base-TX half duplex is accepted, read only
28	10TXF	10Base-T duplex is accepted, read only
27	10TXH	10Base-T half duplex is accepted, read only
16	Reserved	Reserved for test purpose, must be set 1 for normal operation.
12	Reserved	Reserved for test purpose, must be set 1 for normal operation.

5.3 Power Management Functions :

MX98715A complies to ACPI Version 1.0, supports D3cold state to generate PMEB. There are basically 3 power saving modes supported, namely Remote Power-On, Remote Wake-Up, and Sleep mode. By default, MX98715A will enable ACPI function with the following registers setup :

PFCS<20> (New Capability)= 1
PFCP<7:0> (Capability Pointer) = 44h
PPMC<7:0> (Capability ID) = 1h

Please refer to PCI configuration registers for more details.

5.3.1 Remote Power-On Mode :

When AC power cord of PC is plugged into the wall outlet, MX98715A will load the network ID from EEPROM and enter itself into Remote Power-On mode automatically. The host and PCI bus has no power at this stage. As soon as a Magic packet addressed to this network adaptor, PMEB will be asserted low to power on the PC.

To set up the Remote Power-On (RPO) mode, as long as a 5.0V standby VDD is connected into the adaptor's isolated VDD and MX98715A will set up itself to detect Magic packet. No registers needed to be programmed. Simply turn off the power switch or plug in the AC power cord of the PC that support RPO and everything else is set automatically.

5.3.2 Remote Wake-Up Mode :

When the PC is still turned on regardless of the status of CPU and system's status, a Magic packet can be detected if enabled. As soon as a Magic packet addressed to the network adaptor is detected, both INTA# and PMEB can be asserted low if registers set up as follows :

CSR16<22> (PME) = 1 and
PPMCSR<8> (PME_EN) =1
to enable PMEB assertion.

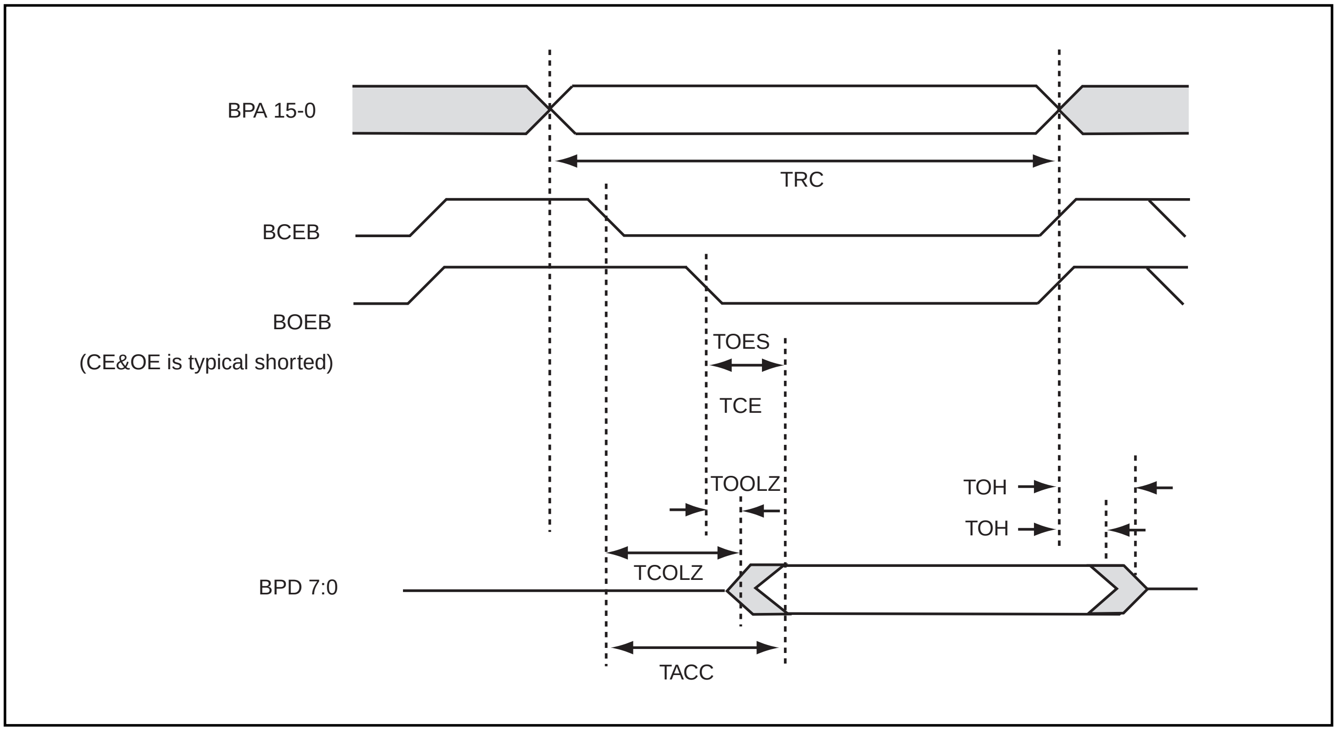
CSR16<22> (PME) = 1 and
CSR7<28> (MPIE) = 1 to enable INTA#
assertion

5.3.3 Sleep Mode :

Set PFDA<31> (Sleep) = 1 will enter the chip into a sleep mode where no TX nor RX activities can be processed. Only PCI configuration can be accessed.

6. AC/DC CHARACTERISTICS

6.1 BOOT ROM TIMING (READ)

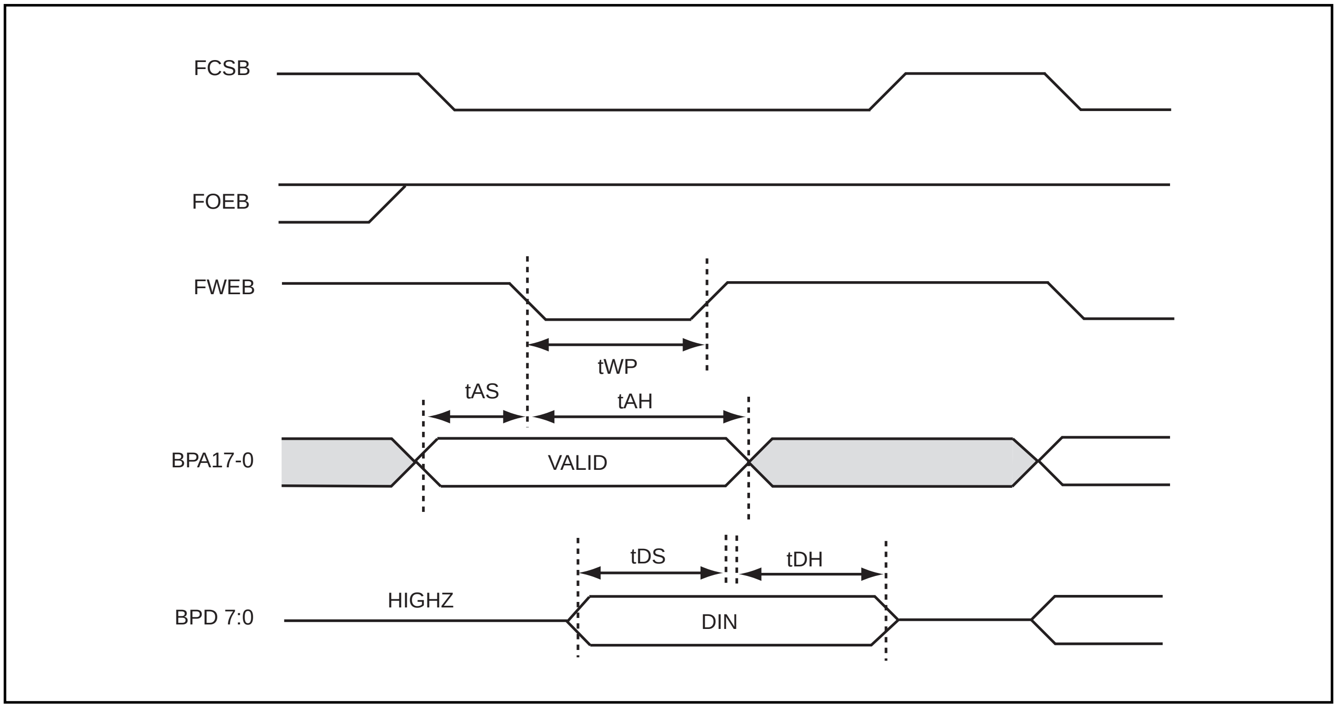

BPA 15-0
TRC
BCEB
BOEB
(CE&OE is typical shorted)
TOES
TCE
TOOLZ
TOH
TOH
TCOLZ
BPD 7:0
TACC

6.2 AC CHARACTERISTICS

SYMBOL	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
TRC	Read Cycle	8	-	-	PCI Cycle
TCE	Chip Enable Access Time	-	-	7	PCI Cycle
TACC	Address Access Time	-	-	7	PCI Cycle
TOES	Output Enable Access Time	-	-	7	PCI Cycl
TOH	Output Hold from Address, CEB, or OEB	0	-	-	ns

PCI cycle range:66ns (16MHz)~25ns (40MHz)

6.3 COMMAND WRITE TIMING WAVEFORMS



SYMBOL	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
tWP	Write Pulse Width	8	-		PCI Cycle
tAS	Address Setup Time	0	-		ns
tAH	Address Hold Time	7	-		PCI Cycle
tDS	Data Setup Time	7	-		PCI Cycl
tDH	Data Hold Time	1	-		PCI Cycle

PCI cycle range:66ns (16MHz)~25ns (40MHz)

6.4 ABSOLUTE OPERATION CONDITION

Supply Voltage (VCC)	-0.5V to +7.0V
DC Input Voltage (Vin)	4.75V to 5.25V
DC Output Voltage (Vout)	-0.5V to VCC +0.5V
Storage Temperature Range (Tstg)	-55℃ to +150℃
Operating Temperature Range	0℃ to 70℃
Power Dissipation (PD)	750mW (Typ)
Lead Temp. (TL) (Soldering, 10 sec)	260℃
ESD Rating (Rzap=1.5K, Czap=100pF)	1.0KV
Clamp Diode Current	±20mA

6.5 DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
TTL/PCI Input/Output					
Voh	Minimum High Level Output Voltage	Ioh = -3mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol = +6mA		0.4	V
Vih	Minimum High Level Input Voltage		2.0		V
Vil	Maximum Low Level Input Voltage			0.8	V
Iin	Input Current	Vi = VCC or GND	- 1.0	+ 1.0	uA
Ioz	Minimum TRI-STATE Output Leakage Current	Vout = VCC or GND	-10	+10	uA
LED output Driver					
Vlol	LED turn on Output Voltage	Iol = 16mA		0.4	V
Supply					
Idd	Average Supply Current	CKREF =25MHz PCICLK = 33MHz	130	170	mA
Vdd	Average Supply Voltage		4.75V	5.25V	V

REVISION HISTORY

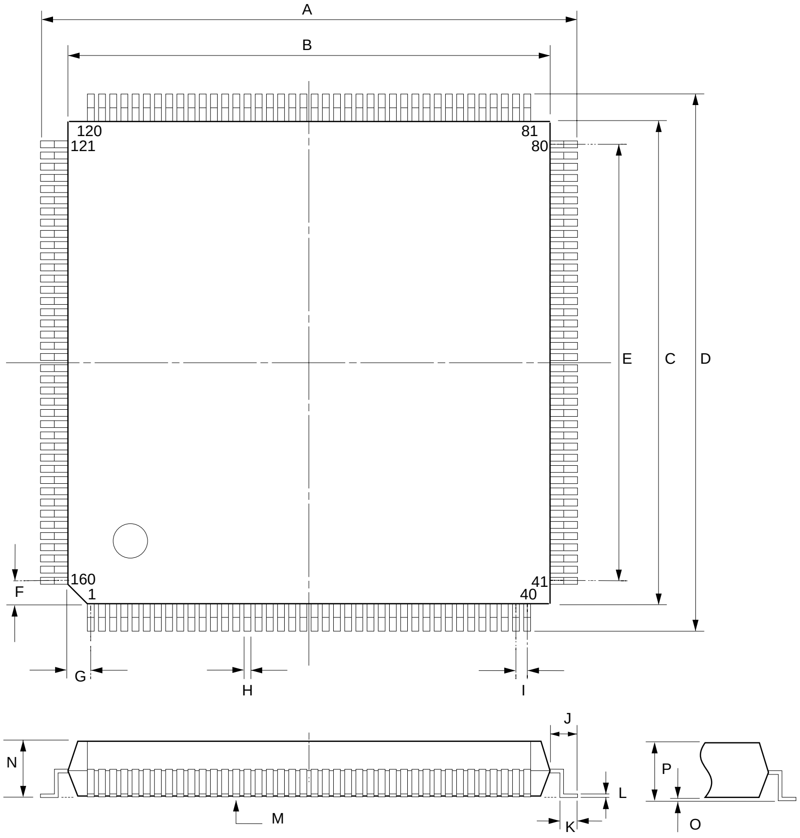
Revision	Destription	Page	Date
1.7	(1) revise PFRV register bit 31-24 to be 2h	7	Sep/15/1998
	(2) exchange description for PFIT register bit 7-0 and bit 15-8	9	
	(3) revise LED2SEL default setting to be Link Speed (10/100)	21	
	(4) revise ESD rating in Section 6.4 from 1.5KV to 1.0KV	29	
	(5) add Power Dissipation in Section 6.4 to be 750mW (typ)	29	
	(6) add Idd value in Section 6.5 to be 130 mA to 170mA	30	

7.0 PACKAGE INFORMATION

160-Pin Plastic Quad Flat Pack

ITEM	MILLIMETERS	INCHES
A	31.20 ±.30	1.228 ±.12
B	28.00 ±.10	1.102 ± .004
C	28.00 ±.10	1.102 ±.004
D	31.20 ±.30	1.228 ±.012
E	25.35	.999
F	1.33 [REF.]	.052 [REF.]
G	1.33 [REF.]	.052 [REF.]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF.]	.063 [REF.]
K	.80 ±.20	.031 ±.008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.
P	3.68 max.	.145 max.

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



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