Signetics

8X320
Bus Interface Register Array

Product Specification

Military
Customer Specific Products

FEATURES

- **16-byte/2-port interface**
- **8- or 16-bit primary port (Host) interface (User selectable)**
- **8-bit secondary port interface**
- **Two 8-bit flag registers (handshake control)**
- **DMA or programmed I/O operation**
- **Two 3-State bidirectional ports**
- **Secondary port is bus compatible with 8X305**
- **Single 5V supply**
- **0.6", 40-pin package**

ARCHITECTURAL OVERVIEW

The Signetics 8X320 Bus Interface Register Array (Figure 1) is a dual-port RAM memory designed for use between a host processor and a peripheral processor. Specifically, the register array provides a convenient and economical interface between the 8X305 Microcontroller (secondary port) and User's Host System (primary port); the host can be almost any bus-oriented device — another processor, a minicomputer, or a mainframe computer. The host has 8-bit (byte) or 16-bit (word) access to the primary port; data can be read-from or written-into any memory location as determined by the primary-port address and control lines. The secondary port (8X305 bus) consists of eight input/output lines and four bus control lines. To implement the secondary-port interface, an 8-bit memory location is addressed during one machine cycle and, during another cycle, data is read or written under control of the secondary (8X305) processor. Both primary and secondary ports feature 3-State outputs and both ports are bidirectional.

BLOCK DIAGRAM

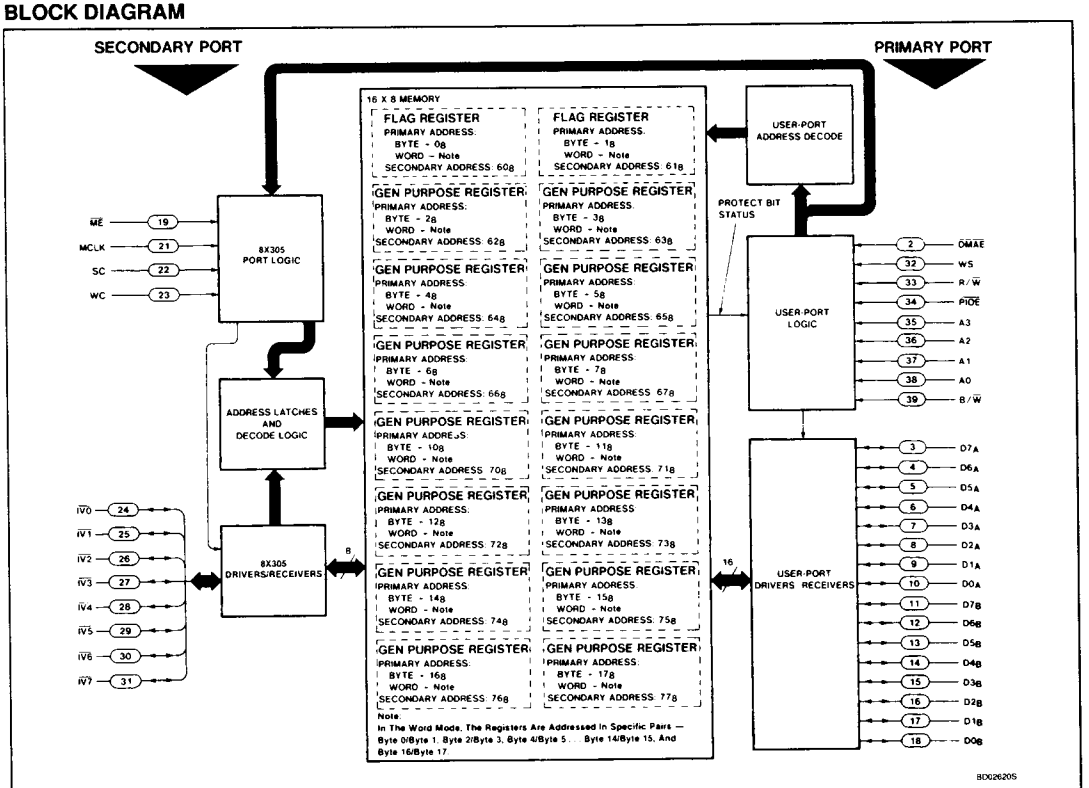
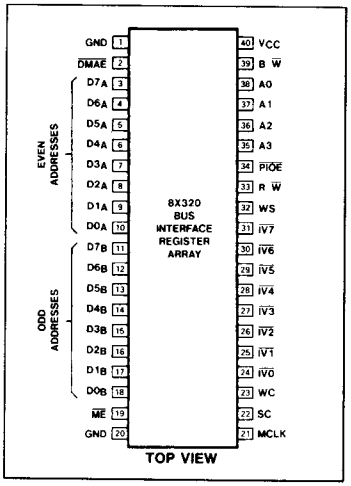


Figure 1. Block Diagram of 8X320 Bus Interface Register Array

Bus Interface Register Array

8X320

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGE	ORDER CODE
40-Pin DIP	8X320/BQA

Besides the convenience and economy of a two-port memory, the array also provides simple handshake control via two 8-bit flag registers, logic to facilitate DMA transfers, and a write-protect feature for the primary port in both byte and word modes of operation.

PIN DESCRIPTION

PIN NO.	IDENTIFIER	FUNCTION
1, 20	GND	**Ground:** Circuit ground.
2	$\overline{DMAE}$	**Direct Memory Access Enable:** Enables primary port to facilitate DMA transfers; does not affect secondary port.
3 – 18	$D0_A - D7_A$/ $D0_B - D7_B$	**Primary Data Port:** Sixteen 3-State lines used for data transfers to-and-from the primary data port; most significant bit is $D0_B$ and least significant bit is $D7_A$.
19	$\overline{ME}$	**Master Enable:** Enables secondary port when active low ($\overline{ME}$).
21	MCLK	**Master Clock:** When MCLK is high, and 8X320 is enabled ($\overline{ME}$ = Low), a register location may be either selected or written-into under control of SC and WC.
22	SC	**Select Command:** With SC high, WC low, MCLK high and $\overline{ME}$ low, data on $\overline{IV0}$ through $\overline{IV7}$ is interpreted as an address. If any one of the 16 register addresses ($60_8 - 77_8$) matches that on the I/O (IV) bus, that particular register is selected and remains selected until another address on the same bank (i.e. $\overline{ME}$ = low) is output on the I/O bus — at which time, the old register is deselected and a new register may or may not be selected.
23	WC	**Write Command:** With WC high, SC low, MCLK high, and $\overline{ME}$ low, the selected register stores contents of $\overline{IV0} - \overline{IV7}$ as data.
24 – 31	$\overline{IV0} - \overline{IV7}$	**Secondary Data Port:** Eight 3-State lines used to transfer data or I/O address to-and-from the secondary data port; most significant bit is $\overline{IV0}$ and least significant bit is $\overline{IV7}$.
32	WS	**Write Strobe:** When active high, data appearing at the primary port ($D0_A$ - $D7_A$/$D0_B$ - $D7_B$) is stored in the register array if the primary port is in the *write* mode.
33	R/$\overline{W}$	**Read/Write Control:** When this signal is high, primary port is in *read* mode; when signal is low, primary port is in *write* mode.
34	$\overline{PIOE}$	**Programmed I/O Enable:** When active low, primary port operates in programmed input/output mode with register to be read-from or written-into selected by A0 – A3.
35–38	A0 –A3	**Primary Port Address Select:** Select register or register-pair that primary port is read-from or write-into. Most significant bit is A3; least significant bit is A0.
39	B/$\overline{W}$	**Byte/Word:** When signal is high, the primary port operates in the byte (8-bit) mode; when signal is low, the primary port operates in the word (16-bit) mode.
40	V_{CC}	**Power:** +5V.

NOTE:
All barred symbols ($\overline{DMAE}$, etc.) denote signals that are asserted (or active) when low (logical 0); signals that are not barred are asserted in the high state (logical 1).

OPERATING CHARACTERISTICS

Memory Organization

Memory and address correlation for the 16-register array is shown in Figure 2. From the primary port, the sixteen 8-bit registers can be addressed in either (8-bit) or word (16-bit) format; in the word mode, the registers are addressed in pairs — $0_8/1_8$, $2_8/3_8$, $4_8/5_8$,... $14_8/15_8$, and $16_8/17_8$. From the secondary port, all registers are addressed in byte format — 60_8 through 77_8. The memory consists of two 8-bit flag registers and fourteen 8-bit general-purpose registers. The flag registers facilitate information transfers between the two ports and, in addition, they protect certain registers from being written into from the primary port.

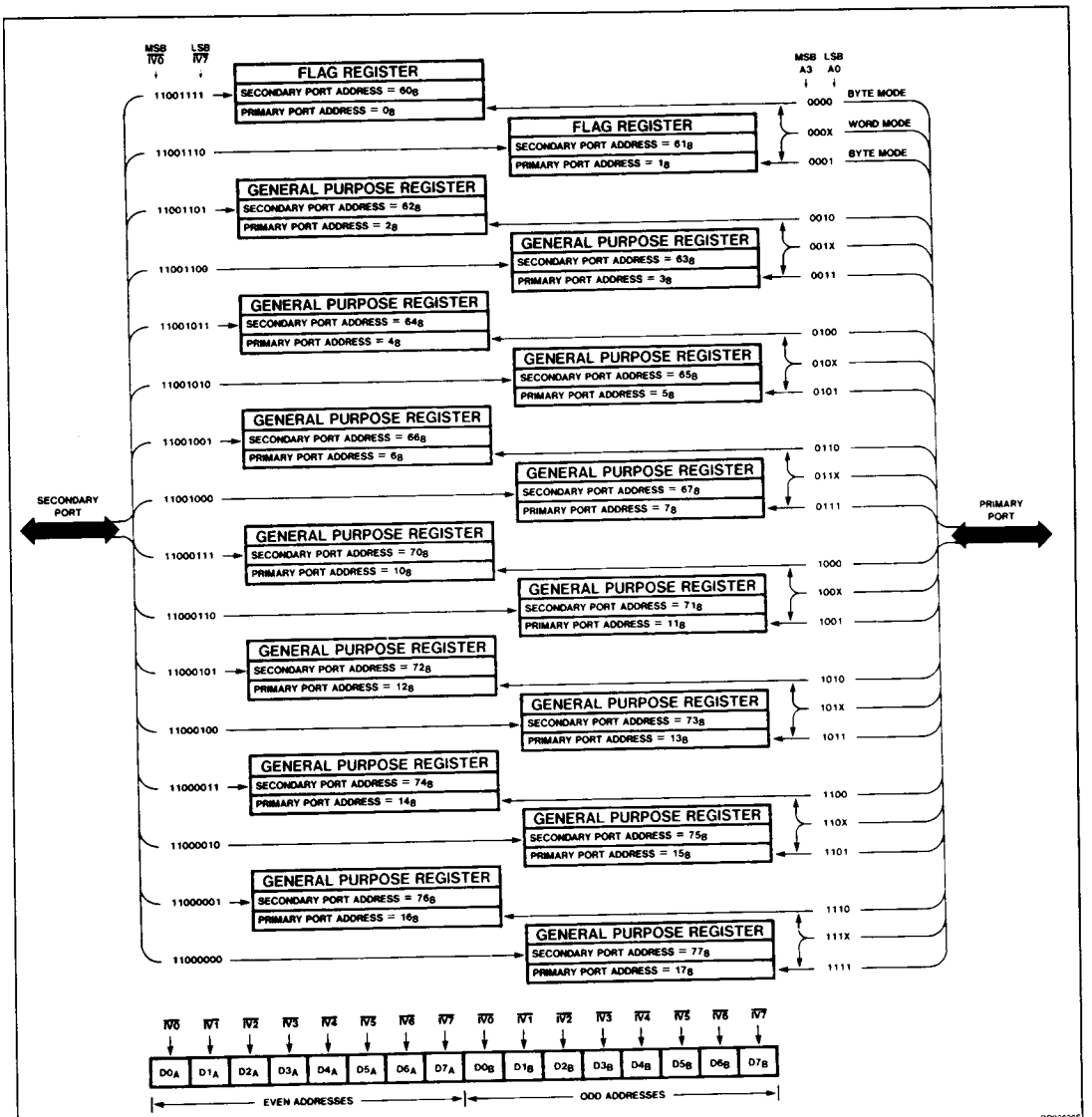


Figure 2. Memory and Address Organization for the 8X320

Table 1. Control Of The Two Flag Register

FLAG	60_8 (0_8)	F2	F3	F4	F5	F6	F7								
REGISTERS	61_8 (1_8)							F0	F1	F2	F3	F4	F5	F6	F7
OCTAL ADDRESS OF	Primary	2	3	4	5	6	7	10	11	12	13	14	15	16	17
CONTROLLING BYTE	Secondary	62	63	64	65	66	67	70	71	72	73	74	75	76	77

Table 2. Relationship Between Flag Register Bits And Those Of Primary And Secondary Ports

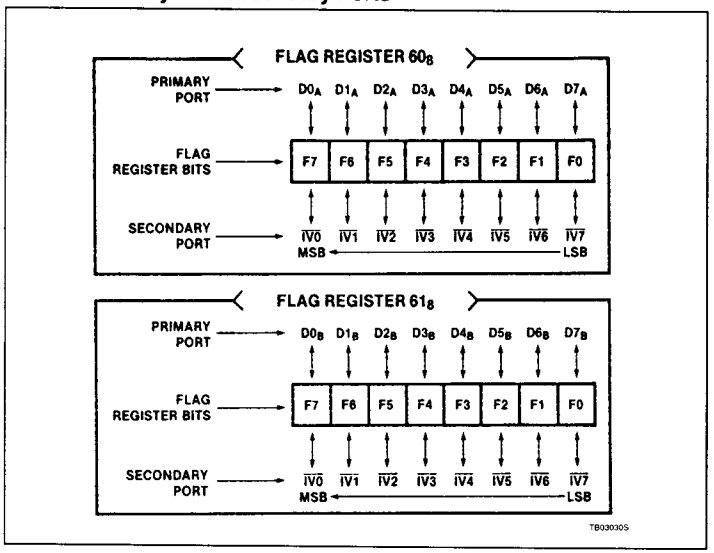


Table 3. Mode Control Of Primary Port

MODE	$\overline{PIOE}$	$\overline{DMAE}$
Disabled (output)	1	1
Programmed I/O	0	1
DMA	X	0

NOTE:
X = Don't Care

Table 4. Primary Port Operating In Programmed I/O Mode

MODE	B/$\overline{W}$	A0	$D0_A - D7_A$ (EVEN ADDRESSES)	$D0_B - D7_B$ (ODD ADDRESSES)
Read	0 (Word)	X	Stored Data	Stored Data
Read	1 (Byte)	0	Stored Data	Hi-Z
Read	1 (Byte)	1	Hi-Z	Stored Data
Write	0 (Word)	X	Write	Write
Write	1 (Byte)	0	Write	No Change
Write	1 (Byte)	1	No Change	Write

NOTE:
X = Don't Care

In either byte or word mode, the write-protect logic, implemented by bits F0 and F1 of register 60_8, inhibits the primary port from writing into addresses 16_8 and 17_8, respectively. Both write-protect bits (F0 and F1) can be read or written from the secondary port; the bits are read-only from the primary port.

As shown in Table 1, flag bits F2 through F7 of 60_8 and F0 through F7 of 61_8 are controlled by the fourteen general-purpose registers. When any one of these registers is written into by either port, the corresponding flag bit for that register is automatically set by internal logic of the 8X320. When information is read from any register, the corresponding flag bit must be reset by user software Except for the write-protect bits, all other flag bits can be read or reset from the primary or the secondary port.

Table 2 shows the relationship between bits of the flag registers and bits of the primary and secondary ports.

FUNCTION AND CONTROL OF PRIMARY PORT

The primary port provides an 8-bit (byte) or 16-bit (word) interface between the 16-byte memory and the user's host system. If the host is an 8-bit system (or 16-bit system operating in Byte mode), the sixteen bidirectional I/O lines must be tied together ($D0_A$ to $D0_B$, $D1_A$ to $D1_B$, ... and $D7_A$ to $D7_B$); when data is input or output on $D0_A$ to $D7_A$, the remaining eight lines ($D0_B$ through $D7_B$) are Hi-Z and vice-versa.

Other than the Byte/$\overline{Word}$ control line, specific operating characteristics of the primary port are controlled by two signals — $\overline{PIOE}$ (Programmed I/O Enable) and $\overline{DMAE}$ (Direct Memory Access Enable). When $\overline{PIOE}$ is active (low) and $\overline{DMAE}$ is inactive (high), the primary port operates in the programmed I/O mode — refer to table 3; in this mode of operation, the register to be read-from or written-into is determined by four address lines (A0 through A3) and the Byte/$\overline{Word}$ control line — see Figure 2 and Table 4. In the DMA mode of operation, A1, A2, and A3 are not used; data is read-from or written-into preassigned registers: bytes 16_8 (76_8) and 17_8 (yy_8) for the byte mode of operation and bytes 14_8 (74_8)/15_8 (75_8) and 16_8 (76_8)/17_8 (77_8) for the word mode of operation. In both cases, switching between bytes 16_8 and 17_8 in the byte mode and 14_8/15_8 and 16_8/17_8 in the word mode is controlled by A0 (the least significant address bit). Refer to Table 5.

Table 4 defines programmed I/O operation of the primary port in terms of read/write functions and Byte/Word control. In the byte mode, data is read-from or written-into the even addresses (p_8, 2_8, 4_8, 6_8, 10_8, 12_8, 14_8, and 16_8) via data lines $D0_A$ through $D7_A$; data is read-from or written-into odd addresses (1_8, 3_8, 5_8, 7_8, 11_8, 13_8, 15_8, and 17_8) via data lines $D0_B$ through $D7_B$. When A0 is low (logical 0), even addresses are selected and when A0 is high (logical 1), odd addresses are selected; thus, A0 is the LSB of a 4-bit address. In the word mode, the state of A0 is irrelevant, since both the odd and even bytes are, simultaneously, read-from or written-into; thus, a register pair is selected by a 3-bit address, A1 being the LSB.

In the DMA mode of operation with $\overline{DMAE}$ set to 0 and other conditions satisfied, data is directly transferred to-or-from specified memory locations under control of Byte/$\overline{Word}$, R/$\overline{W}$, and A0. The state of the Byte/$\overline{Word}$ control line determines whether the data word is 8 bits or 16 bits. The A0 address line correlates eight of the sixteen data lines ($D0_A$ - $D7_A$ or $D0_B$ - $D7_B$) with the proper byte/word location. Thus, in the word mode, the exchange of data between the memory and the primary port occurs via $D0_A$ – $D7_A$ for bytes 14_8 and 16_8 and via $D0_B$ – $D7_B$ for bytes 15_8 and 17_8. The byte mode of operation is similar, except that the unused eight lines are 3-Stated.

Table 5. DMA Operation Of The Primary Port

MODE	BYTE/WORD	A0	$D0_A - D7_A$	$D0_B - D7_B$
Read	0 (Word)	0	Data stored in byte 14_8	Data stored in byte 15_8
Read	0 (Word)	1	Data stored in byte 16_8	Data stored in byte 17_8
Read	1 (Byte)	0	Data stored in byte 16_8	Hi-Z
Read	1 (Byte)	1	Hi-Z	Data stored in byte 17_8
Write	0 (Word)	0	Write to byte 14_8	Write to byte 15_8
Write	0 (Word)	1	Write to byte 16_8	Write to byte 17_8
Write	1 (Byte)	0	Write to byte 16_8	Hi-Z
Write	1 (Byte)	1	Hi-Z	Write to byte 17_8

FUNCTION AND CONTROL OF SECONDARY PORT

The secondary port provides an 8-bit interface between the sixteen memory registers and the 8X305 (or other processor). As shown in Table 6, the secondary-port interface is controlled by five input signals and a status latch. The status latch is set when SC is high (MCLK high/$\overline{ME}$ low) and a valid memory address (60_8 – 77_8) is presented to the 8X320 via the secondary data port ($\overline{IV0}$/$\overline{IV7}$). The latch is cleared by internal logic when an invalid memory address is presented at the secondary port. In all read/write operations from the secondary port, the status latch acts like a master enable; data can be transferred only if the status latch is set.

Table 6. Functional Control of Secondary Port

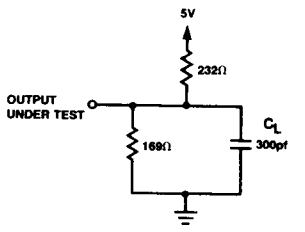
$\overline{ME}$	SC[1]	WC[1]	MCLK	R/$\overline{W}$	STATUS LATCH	FUNCTION OF SECONDARY BUS
L	L	L	X	X	Set	Output data from 8X320 memory to 8X305.
L	L	H	H	H	Set	Data from 8X305 is input and written-into a previously-selected memory location of the 8X320 (Note 2).
L	L	H	H	L	Set	With the primary port in the write mode (R/$\overline{W}$ = 0), the secondary port is overridden and cannot write to the same register addressed by the primary port; however, the register addressed by the primary port can be read and any other register can be read-from or written-into from the secondary port (Note 2).
L	H	L	H	X	X	Data transmitted to the secondary port via the $\overline{IV}$ bus is interpreted as an address; if address is within range of 60_8 - 77_8 the memory status latch is subsequently set.
L	L	H	L	X	X	Inactive
L	H	L	L	X	X	Inactive
L	L	X	X	X	Not set	Inactive
H	X	X	X	X	X	Inactive

NOTES:
1. The SC and WC lines should never both be high at the same time; the 8X305 processor never generates this condition.
2. During read or write operations, the same register can be simultaneously addressed from either port. For any write operation by both ports on the same register, the primary port has priority; other than this, the 8X320 does not indicate error conditions or resolve conflicts.
3. X = Don't Care.

DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq 125°C$

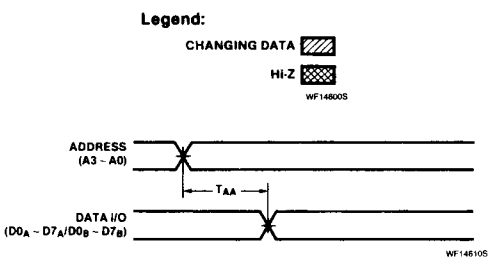
SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]		LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{IL}	Low level input voltage					0.80	V
V_{IH}	High level input voltage			2.0			V
V_{OL}	Low level output voltage	$V_{CC} = 4.5V$; $I_{OL} = 16mA$				0.5	V
V_{OH}	High level output voltage	$V_{CC} = 4.5V$; $I_{OH} = -3mA$		2.5			V
V_{IK}	Input clamp voltage	$V_{CC} = 4.5V$; $I_I = -18mA$				-1.5	V
I_{CC}	Supply current	$V_{CC} = 5.5V$	$T_A = 125°C$			210	mA
			$T_A = 25°C$			260	mA
			$T_A = -55°C$			300	mA
I_{OS}	Short circuit output current[3]	$V_{CC} = 5.5V$		-20		-100	mA
I_{IL}	WC, MCLK, SC, & $\overline{ME}$	$V_{CC} = 5.5V$; $V_{IL} = 0.50V$				-1.0	mA
I_{IL}	B/$\overline{W}$	$V_{CC} = 5.5V$; $V_{IL} = 0.50V$				-1.6	mA
I_{IL}	A0 – A3	$V_{CC} = 5.5V$; $V_{IL} = 0.50V$				-1.0	mA
I_{IL}	$\overline{DMAE}$	$V_{CC} = 5.5V$; $V_{IL} = 0.5V$				-800	µA
I_{IL}	WS, $\overline{PIOE}$, & R/$\overline{W}$	$V_{CC} = 5.5V$; $V_{IL} = 0.5V$				-400	µA
I_{IL}	$\overline{IV0} - \overline{IV7}$	$V_{CC} = 5.5V$; $V_{IL} - 0.5V$				-400 each line	µA
I_{IL}	$D0_A - D7_A/D0_B - D7_B$	$V_{CC} = 5.5V$; $V_{IL} = 0.5V$				-400 each line	µA
I_{IH}	WC, SC, MCLK, & $\overline{ME}$	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				100	µA
I_{IH}	B/$\overline{W}$	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				240	µA
I_{IH}	A0	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				120	µA
I_{IH}	A1 – A3	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				60	µA
I_{IH}	$\overline{DMAE}$	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				120	µA
I_{IH}	WS, $\overline{PIOE}$, & R/$\overline{W}$	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				60	µA
I_{IH}	$\overline{IV0} - \overline{IV7}$ and $D0_A - D7_A/D0_B - D7_B$	$V_{CC} = 5.5V$; $V_{IH} = 5.5V$				100	µA

AC TEST CIRCUIT

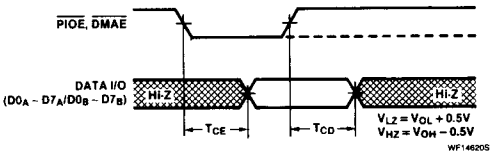


NOTE:
C_L includes jig and probe capacitance.

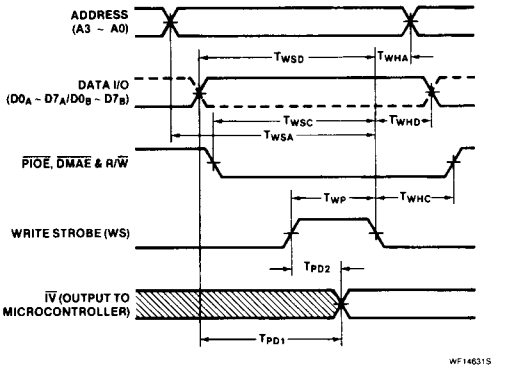
AC CHARACTERISTICS OF PRIMARY PORT



Address Access Time



Primary Port Enable/Disable Times

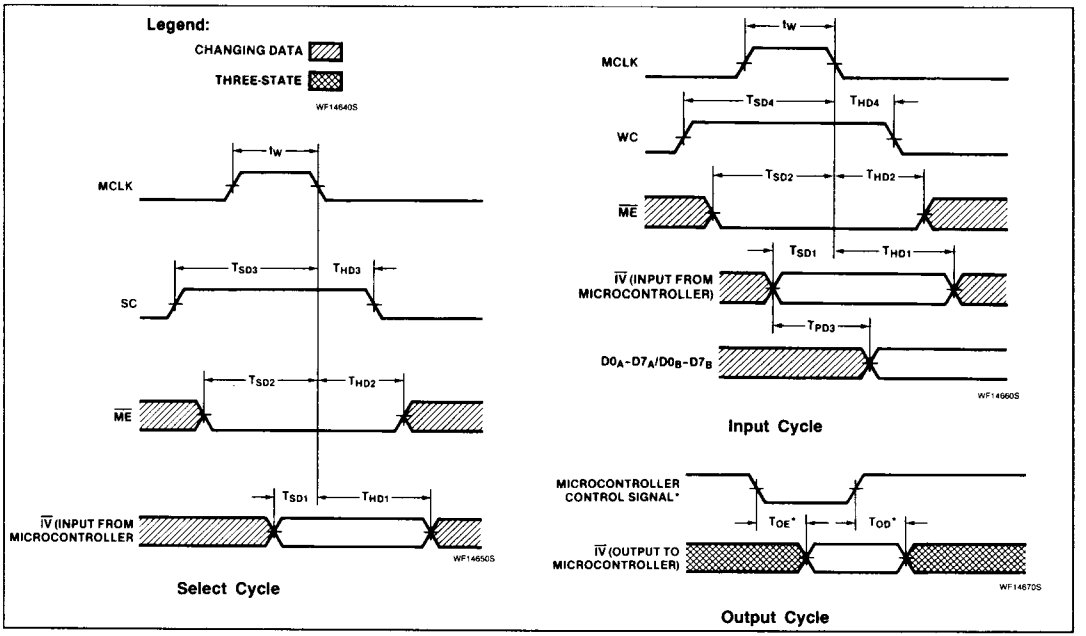


Write Cycle

AC ELECTRICAL CHARACTERISTICS OF PRIMARY PORT $4.5V \le V_{CC} \le 5.5V, -55°C \le T_C \le 125°C$

SYMBOL	PARAMETER	FROM	TO	LIMITS			UNIT
				Min	Typ	Max	
T_{AA}	Address Access Time	A3 – A0	$D0_A – D7_A/D0_B – D7_B$			65	ns
T_{CE}	Primary port enable time	↓PIOE ↓DMAE	$D0_A – D7_A/D0_B – D7_B$			30	ns
T_{CD}	Primary port disable time	↑PIOE ↑DMAE	$D0_A – D7_A/D0_B – D7_B$			35	ns
T_{WSA}	Address setup time	A3 – A0	↓WS	60			ns
T_{WHA}	Address hold time	↓WS	A3 – A0			0	ns
T_{WSD}	Primary port data setup time	$D0_A – D7_A/D0_B – D7_B$	↓WS	30			ns
T_{WHD}	Primary port data hold time	↓WS	$D0_A – D7_A/D0_B – D7_B$			5	ns
T_{WSC}	Write mode control setup time	PIOE DMAE R/W	↓WS ↓WS ↓WS	35 45 55			ns ns ns
T_{WHC}	Write mode control hold time	↓WS	PIOE DMAE R/W			15 10 10	ns nsns
T_{WP}	Write strobe pulse width			25			ns
T_{PD1}[4]	Primary port data delay	$D0_A – D7_A/D0_B – D7_B$	IV0 – IV7			90	ns
T_{PD2}[5]	Primary port data delay from WS	↑WS	IV0 – IV7			90	ns

AC CHARACTERISTICS OF SECONDARY PORT



AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq 125°C$

SYMBOL	PARAMETER[1]	FROM	TO	LIMITS			UNIT
				Min	Typ	Max	
T_W	MCLK pulse width			30			ns
T_{SD1}	Data setup time	$\overline{IV0} - \overline{IV7}$	↓MCLK	35			ns
T_{SD2}	$\overline{ME}$ setup time	$\overline{ME}$	↓MCLK	40			ns
T_{SD3}	SC setup time	SC	↓MCLK	40			ns
T_{SD4}	WC setup time	WC	↓MCLK	40			ns
T_{HD1}	Data hold time	↓MCLK	$\overline{IV0} - \overline{IV7}$			5	ns
T_{HD2}	$\overline{ME}$ hold time	↓MCLK	$\overline{ME}$			0	ns
T_{HD3}	SC hold time	↓MCLK	SC			0	ns
T_{HD4}	WC hold time	↓MCLK	WC			0	ns
T_{PD3}[6]	$\overline{IV}$ propagation time	$\overline{IV}$	$D0_A - D7_A/D0_B - D7_B$			65	ns
T_{OE}	Output enable	$\overline{ME}$, SC, or WC	$\overline{IV0} - \overline{IV7}$			30	ns
T_{OD}	Output disable	$\overline{ME}$, SC, or WC	$\overline{IV0} - \overline{IV7}$			35	ns

NOTE:
1. Operating temperature ranges are guaranteed after terminal equilibrium has been reached.
2. All voltages are measured with respect to ground terminal.
3. Short only one output at a time.
4. Measurement with Write Strobe set High and the control signals of the secondary port set for output data from the same register.
5. Measurement with primary port data stable and control signals of secondary port set for output data from the same register.
6. Measured with MCLK = High and control signals of the primary port set for output data from the same register.

Signetics

Packaging Information

T-90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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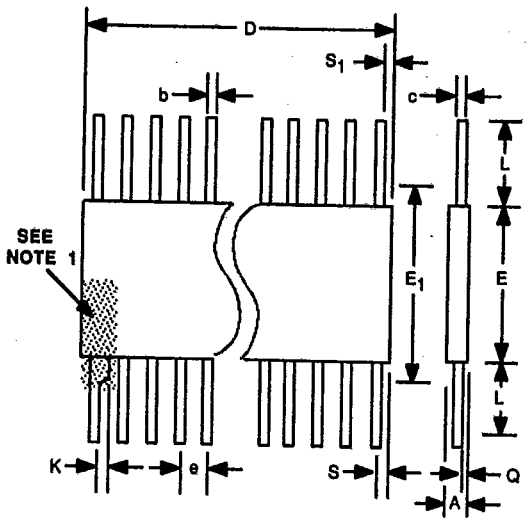
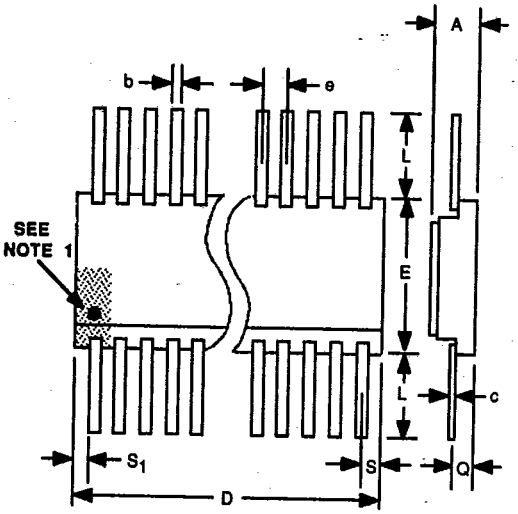
Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

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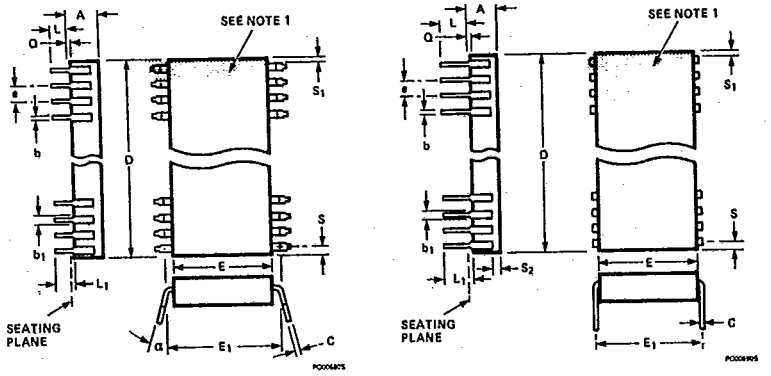
Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1 Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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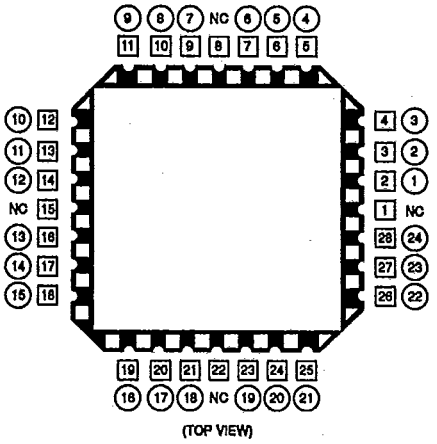
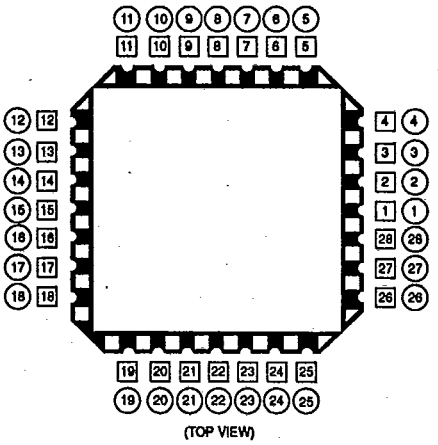
Packaging Information

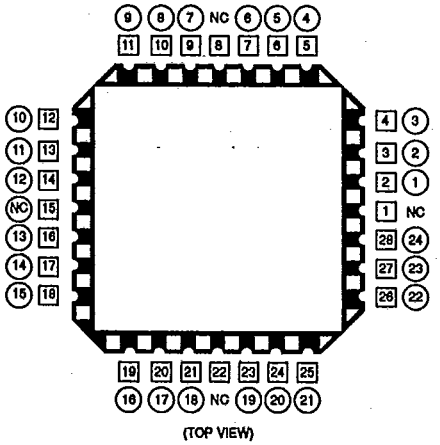
LEADLESS CHIP CARRIER (LLCC) PINOUTS



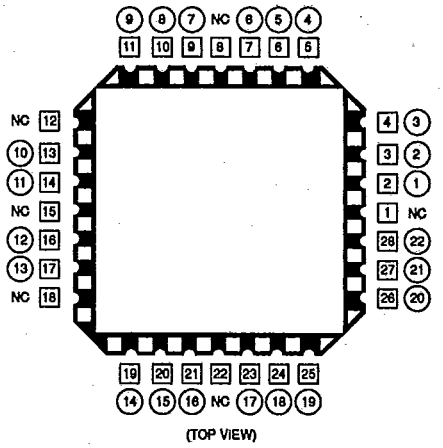
24–Lead Logic Pinout for 28 Terminal Chip Carrier



26–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect