National Semiconductor

ADVANCE INFORMATION
March 1994

NM28F040
4,194,304-Bit (512k × 8) CMOS FLASH

General Description

The NM28F040 is a 4,194,304-bit FLASH Electrically Erasable and Programmable Non-volatile Memory device. The NM28F040 features a single command for Read, Auto Chip Erase, Auto Block Erase, and Auto Program/Verify to allow ease of use for on-board programming.

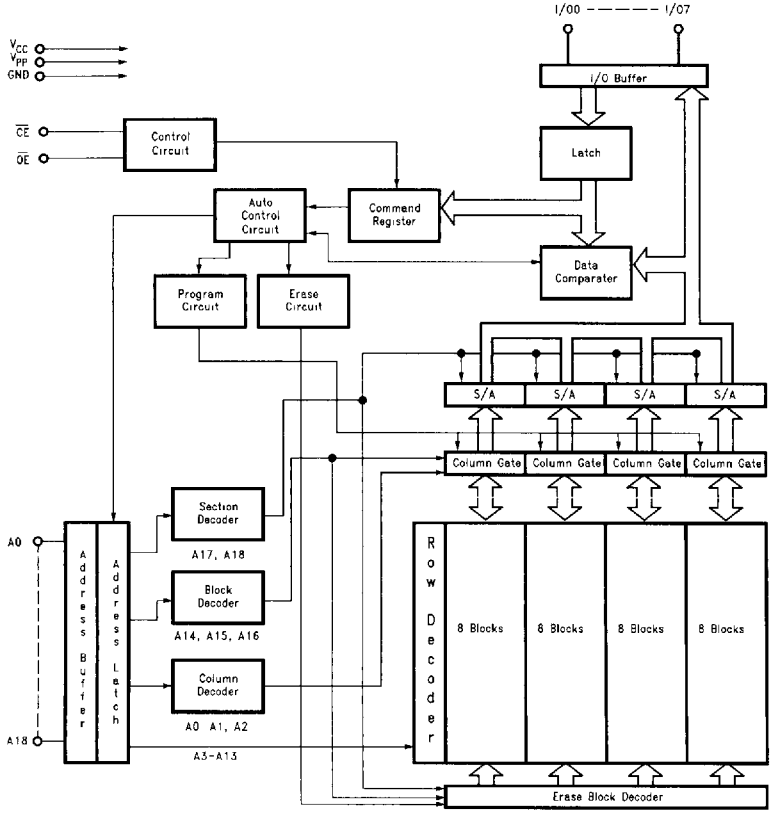
The NM28F040 is ideally suited for applications such as firmware storage, BIOS, engine control modes, and wireless communication where EPROM has been used in the past. The 16 kbyte sector size allows for easier management of code blocks.

The NM28F040 is available in either a 32-pin plastic DIP, SOP, or forward and reverse bend TSOP packages to suit a variety of design applications.

Features

- Power supply: V_{PP} = 12V ±0.6V, V_{CC} = 5V ±0.25V
- Mode: Read/Reset, Auto Program (byte unit), Auto Chip Erase, Auto Block Erase (16 kbyte x 32 blocks), Status polling
- Mode Control: Command input
- W/E cycle: 10,000 cycles (target)
- Access time: 120ns/150ns
- Power dissipation: Operating 30mA, Standby 100μA
- Pin compatible with NM27C040 EPROM
- Packages available: 32-pin DIP, SOP, TSOP, Reversed TSOP

Functional Diagram



TL/D/11873–4

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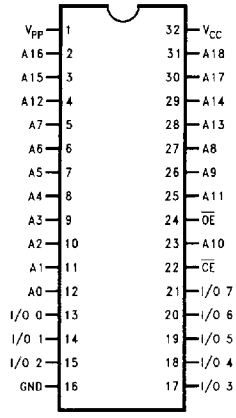
Connection Diagrams

Dual-In-Line Package (N)
Small Outline Package (M)



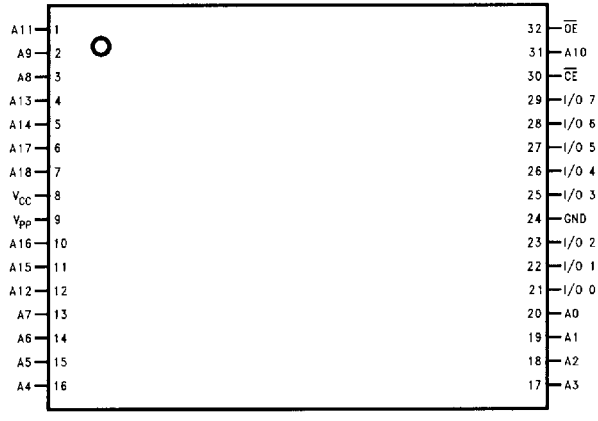
TL/D/11873-1

Top View

Pin Names

A0–A18	Address Input
I/O_0–I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program/Erase Supply
V_{CC}	Supply (5V)
GND	Ground

TSOP Package (T)



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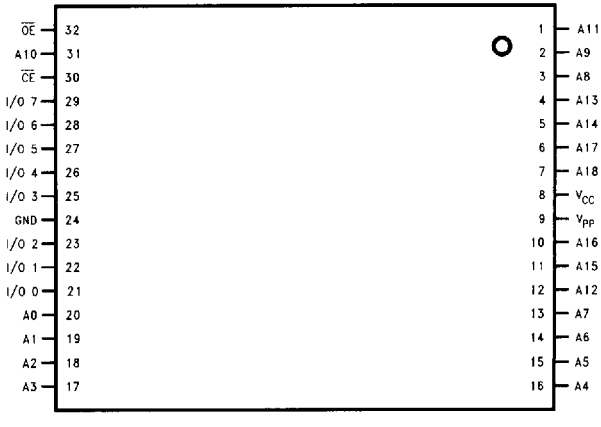
Reversed TSOP Package (TR)



TL/D/11873-3

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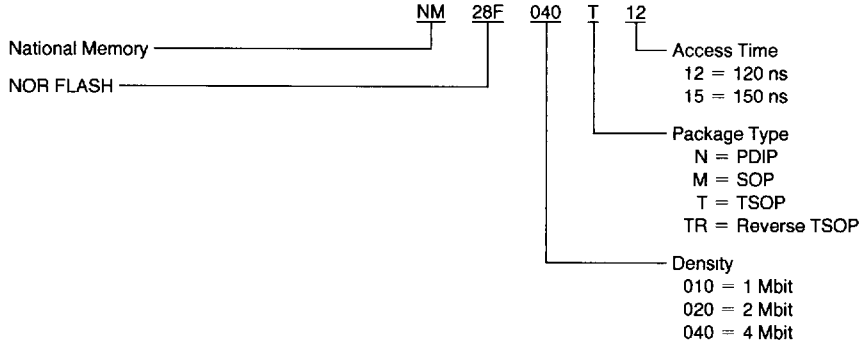
Ordering Information

COMMERCIAL TEMPERATURE RANGE (0°C to +70°C)
V_{CC} = 5.0V ±5%

Parameter/Order Number	Access Time (ns)
NM28F040 N, M, T, TR 12	120
NM28F040 N, M, T, TR 15	150



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.6V to +7.0V
Program/Erase Supply Voltage (V_{PP})	−0.6V to +14.0V
Input Voltage (V_{IN})	−0.6V to +7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to +7.0V
Power Dissipation (P_D)	1.0W
Lead Temp. (Soldering, 10 seconds)	260°C
Storage Temperature Range (T_{STG})	−55°C to +150°C
Operating Temperture Range (T_{OPR})	0°C to +70°C
Erase/Program Cycling Capability (N_{EW})	10,000 Cycle
Input Voltage (A9) (V_{ID})	−0.6V to +13.5V

DC and Operating Characteristics T_A = 0°C to +70°C

Symbol	Parameter	Min	Max	Units
V_{CC}	V_{CC} Supply Voltage	4.75	5.25	V
V_{ID}	A9 Input High Voltage (during ID Read)	11.4	12.6	V
V_{PPL}	V_{PP} Supply Voltage (during Read Operation)	0	6.5	V
V_{PPH}	V_{PP} Supply Voltage (during Erase/Program Operations)	11.4	12.6	V

DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	μA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		−0.5	0.8	
V_{OH}	Output High Voltage	I_{OH} = −0.40 mA	2.4		
V_{OL}	Output Low Voltage	I_{OL} = +2.10 mA		0.4	
I_{CCO1}	V_{CC} Read Average Current (Read/Signature Read)	$V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0 mA, $t_{CYCLE} = t_{RC}$ (min) Cycle		30	mA
I_{CCO2}	V_{CC} Programming Average Current	$V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 9 μs		30	
I_{CCO3}	V_{CC} Erase Average Current	$V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0 mA		30	
I_{CCS1}	V_{CC} Standby Current (Read)	$\overline{CE} = V_{IH}$		1	mA
I_{CCS2}	V_{PP} Standby Current	$\overline{CE} = V_{CC} - 0.2V$		100	μA
I_{PPS}		$0V \le V_{PP} \le 6.5V$		±10	
		$11.4V \le V_{PP} \le 12.6V$		200	
I_{PP1}	V_{PP} Read Average Current (Except Program and Erase)	$0V \le V_{PP} \le 6.5V$, $V_{IN} = V_{IH}/V_{IL}$		±10	
		$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		200	
I_{PP2}	V_{PP} Programming Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		30	mA
I_{PP3}	V_{PP} Erase Average Current	$11.4V \le V_{PP} \le 12.6V$, $V_{IN} = V_{IH}/V_{IL}$		30	
I_{ID}	A9 Pin High Voltage Input Current	$11.4V \le V_{ID} \le 12.6V$		200	μA

6501126 0069954 135

AC Electrical Characteristics

READ OPERATION

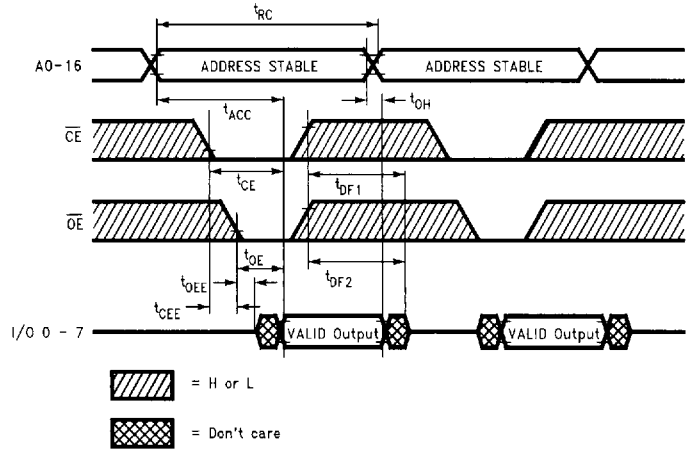
T_A = 0° to +70°C, V_{CC} = 5V ±5%, V_{PP} = 0V to V_{CC} or 12.0V ±5%

Symbol	Parameter	NM28F040						Units
		-120			-150			
		Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	120			150			ns
t_{ACC}	Address Access Time			120			150	
t_{CE}	$\overline{CE}$ Access Time			120			150	
t_{OE}	$\overline{OE}$ Access Time			50			70	
t_{CEE}	$\overline{CE}$ to Output Low Z	0			0			
t_{OEE}	$\overline{OE}$ to Output Low Z	0			0			
t_{OH}	Output Data Hold Time	0			0			
t_{DF1}	$\overline{CE}$ to Output High Z			30			30	
t_{DF2}	$\overline{OE}$ to Output High Z			30			30	

AC TEST CONDITIONS

- Output Load — TTL Gate and C_L = 100 pF
- Input Pulse Rise and Fall Time (10%–90%) — 5 ns max
- Input Pulse Level — 0.6V/2.4V
- Timing Measurement Reference Level — Input 0.8V/2.0V, Output 0.8V/2.0V

Waveform for Read Operations



TL/D/11873-5

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AC Electrical Characteristics (Continued)

COMMAND CONTROL OPERATION

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{PP} = 12.5V ±5%

Symbol	Parameter	120			150			Units
		Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Setup Time	0			0			ns
t_{AH}	Address Hold time	50			60			
t_{OES}	$\overline{OE}$ Setup Time	0			0			
t_{DS}	Data Setup Time	50			60			
t_{DH}	Data Hold Time	0			0			
t_{CEHL}	$\overline{CE}$ Low Level Hold Time	50			60			
t_{CEHH}	$\overline{CE}$ High Level Hold Time	20			30			
t_{CMC}	Command Cycle Time	120			150			
t_{OEPS}	Status Polling $\overline{OE}$ Setup Time	20			30			
t_{PPW}	Auto Program Time	16			16			µs
t_{PCEW}	Auto Chip Erase Time	10			10			s
t_{PBEW}	Auto Block Erase Time	0.5			0.5			
t_{ACC}	Address Access Time			120			150	ns
t_{CE}	$\overline{CE}$ Access Time			120			150	
t_{OE}	$\overline{OE}$ Access Time			50			60	
t_{CEE}	$\overline{CE}$ to Output Low Z	0			0			
t_{OEE}	$\overline{OE}$ to Output Low Z	0			0			
t_{OH}	Output Data Hold Time	0			0			
t_{DF1}	$\overline{CE}$ to Output High Z			30			30	
t_{DF2}	$\overline{OE}$ to Output High Z			30			30	
t_{RC}	Read Cycle Time	120			150			

Capacitance* T_A = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		10	12	pF

*This parameter is periodically sampled and is not 100% tested

6501126 0069956 T08

Mode Selection

Mode		Pin						
		$\overline{CE}$	$\overline{OE}$	Address	I/O	V_{CC}	V_{PP}	Power
Read	Read	L	L	Read Address	Data Input	5V	0–V_{CC} or 12V	Active
	Output Deselect	L	H	*	High Impedance			
	Standby	H	*	*				Standby
Command Input		⊓	H	(Note 1)	Command Data	5V	12V	Active
Program/Erase		*	*	*				
Program/Erase Status Polling		L	L	*	I/O ~ 3,5,6: HZ I/O4: Fail/$\overline{Pass}$ I/O7: Ready/$\overline{Busy}$			
ID Read		L	L	"0"/"1"	Code Output			

*H or L

Note 1: Shown as Command Definition Table and Operation Timing Chart

Command Definition Table

Function	Bus Cycle	1st Bus Cycle			2nd Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	X	00H			
ID Read	2	WRITE	X	90H	READ	0000/1H	Mfg/Dev ID
Auto Byte Program	2	WRITE	X	10H	WRITE	Byte Address	Data
Auto Chip Erase	2	WRITE	X	30H	WRITE	X	30H
Auto Block Erase	2	WRITE	X	20H	WRITE	Block Address	D0H
Reset	2	WRITE	X	FFH	WRITE	X	FFH

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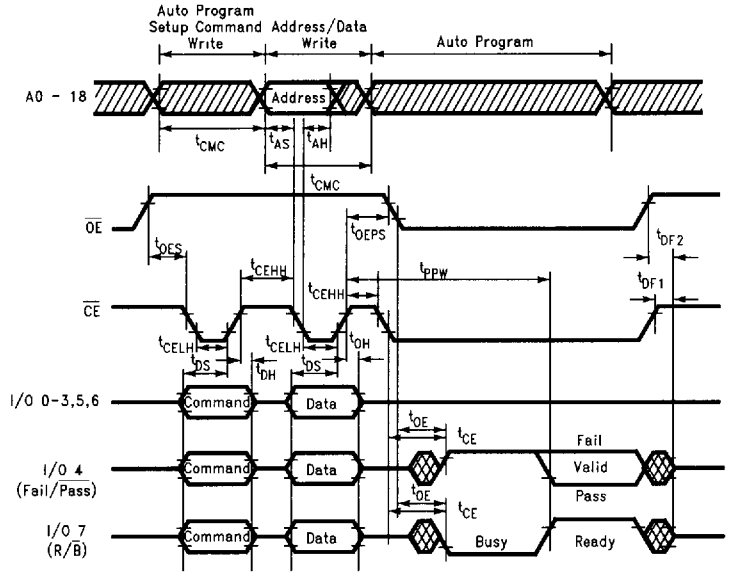
Auto Program Operation Timing Chart



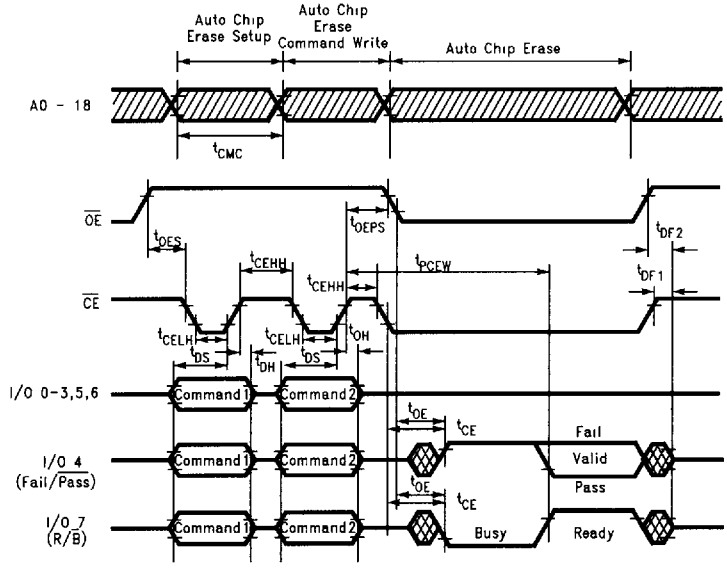
Command = '10H'

= H or L

= Don't care

TL/D/11873-6

Auto Chip Erase



Command 1 = '30H, Command 2 = '30H'

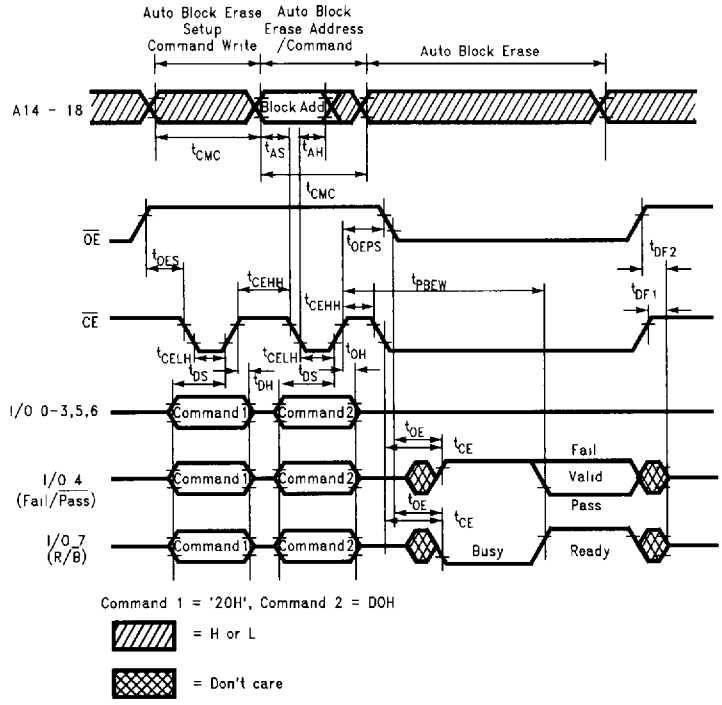
= H or L

= Don't care

TL/D/11873-7

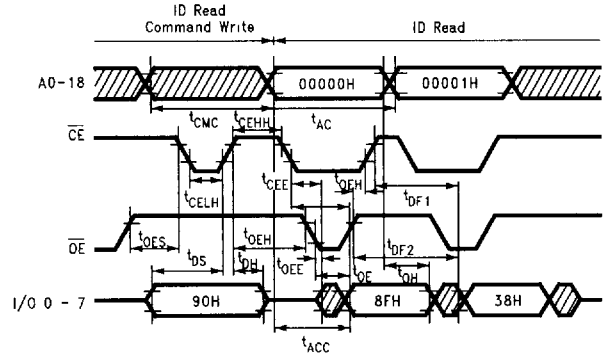
6501126 0069958 880

Auto Block Erase Operation



TL/D/11873-8

ID Read Operation



TL/D/11873-9

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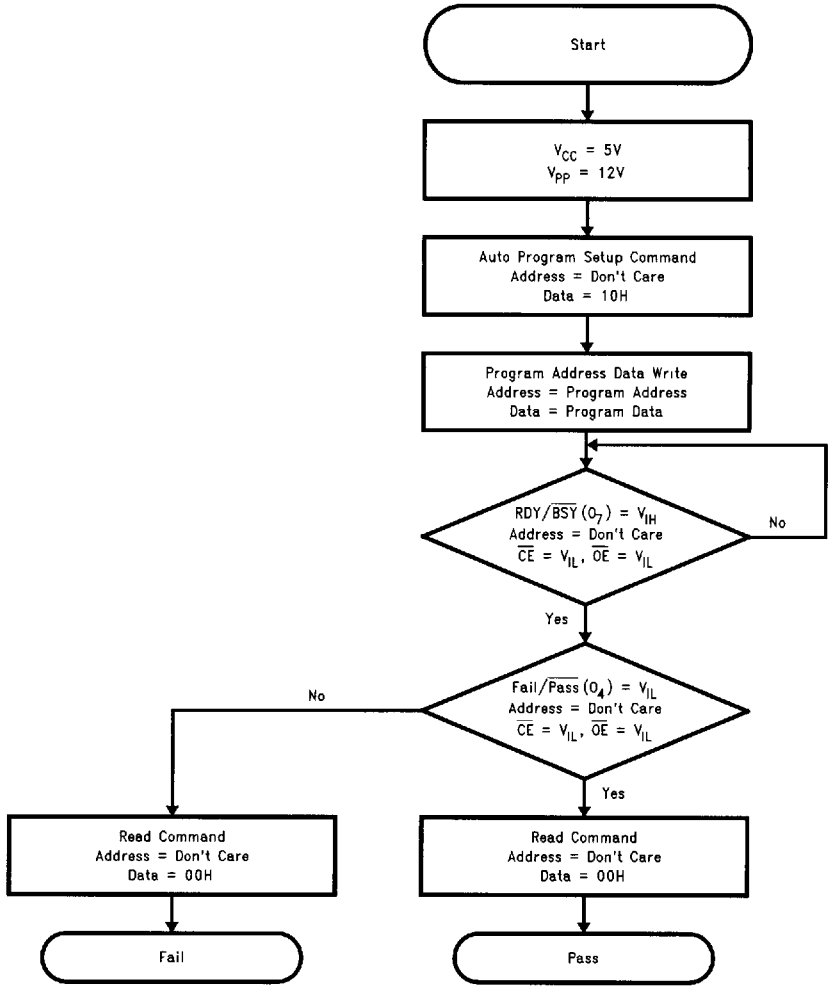
Auto Program Flow Chart



TL/D/11873–10

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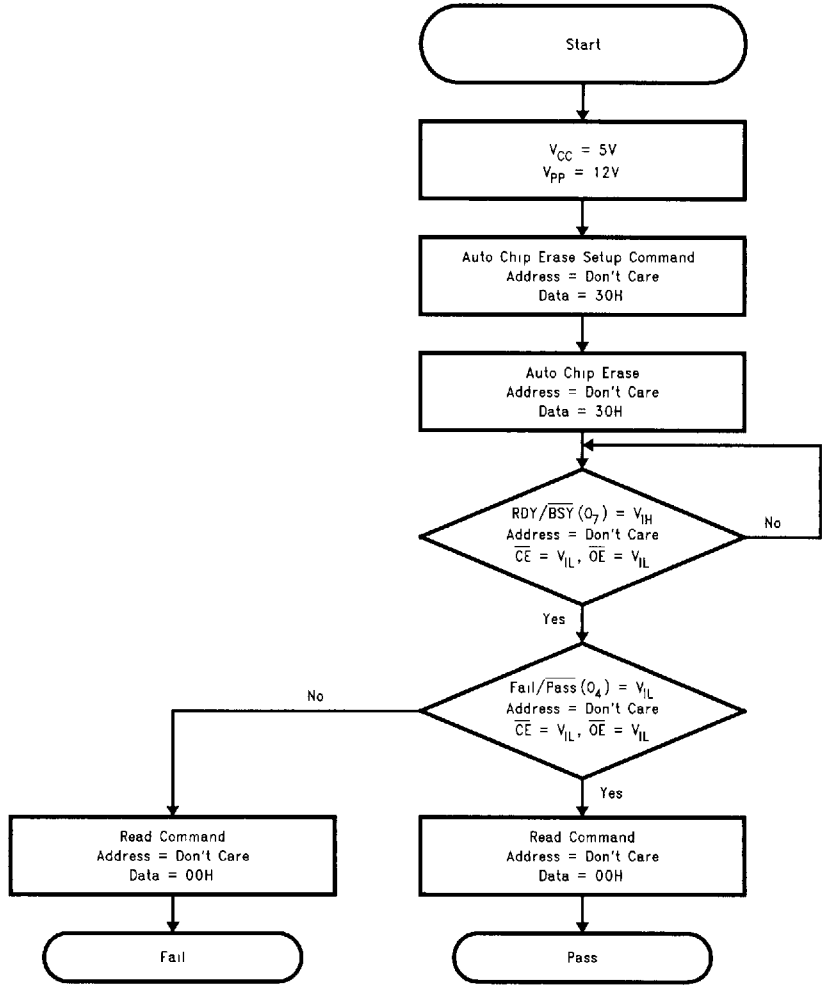
Auto Chip Erase Flow Chart



TL/D/11873–11

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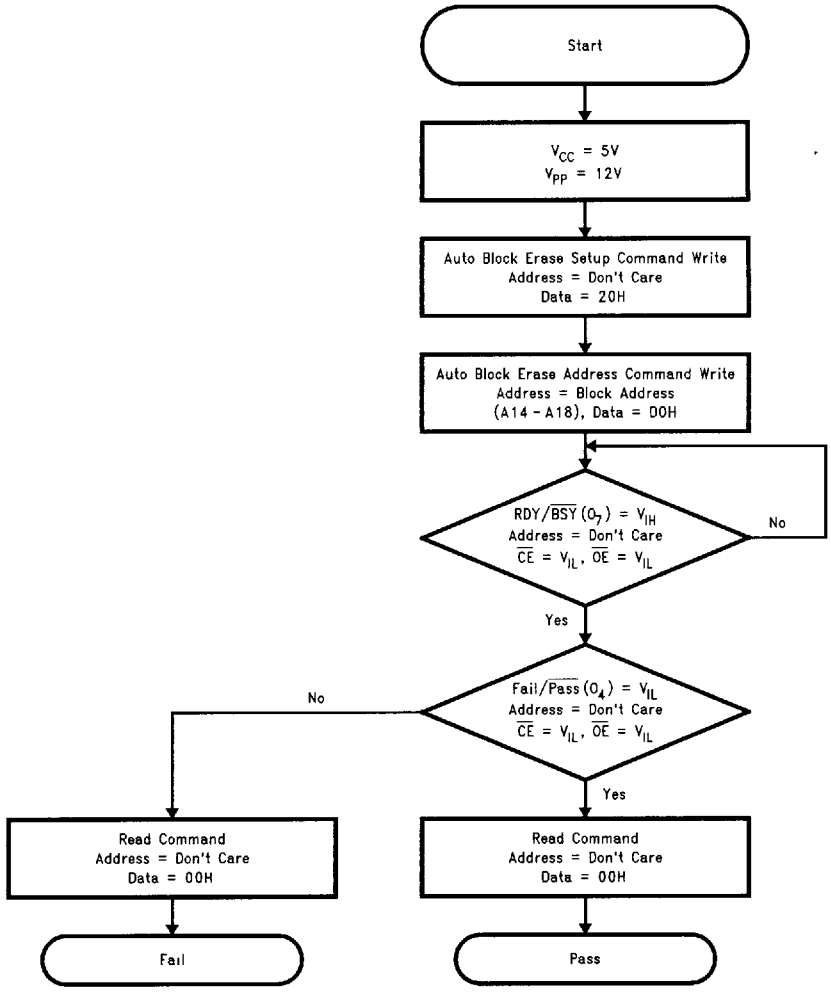
Auto Block Erase Flow Chart



TL/D/11873-12

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Functional Description

OPERATING MODE

The NM28F040 features six modes of operation: Read, ID Read, Auto Byte Program/Program-Verify, Auto Chip Erase/Erase-Verify, Auto Block Erase/Erase Verify, and Reset. Each mode is selected by a command input through the I/O pins.

READ MODE: When the device is set to read mode, it acts as an asynchronous ROM with the access time of 120 ns/150 ns. The device enters read mode regardless of a read command input in the case of V_{PP} = 0 to V_{CC}. The read command (00H) is required to set the read mode in the case of V_{PP} = 12V. The device is automatically set to read mode after V_{PP} changes from 0 ~ V_{CC} to 12V.

ID READ MODE: The ID read mode is utilized for recognizing the device type. There are two ways to read the device ID. Method (A) is normally used for in-circuit erase and reprogramming while method (B), which is the same method used to identify EPROMs, is used by automated EPROM programmers. These programmers match the program algorithm to be used based on the ID.

A. The ID read mode is set by a "90H" command input with V_{PP} = 12V. The "00000H" address location indicates the manufacturer code (8FH) while the "00001H" address location indicates the device code (38H). The access time of the ID read is the same as a normal read operation. (Refer to ID Read Operation Timing Chart for details.)

B. The ID mode can also be set by applying V_{ID} to the A9 pin with V_{PP} = 0 ~ V_{CC}. The manufacturer code is read out of the I/Os while A10–A18 = V_{IL} and A0–A8 = 000H. The device code is read out while A10–A18 = V_{IL} and A0–A8 = 001H.

AUTO PROGRAM MODE: The program mode is set by entering a "10H" command input at V_{PP} = 12V. The next bus cycle will latch the input data and target address. The program operation is enabled at the end of this second bus cycle. The Program and program-verify are automatically executed inside the device until complete. The status of the device is output from I/O7 for Ready/Busy and I/O4 for Pass/Fail. The reset command (FFH) can be used to terminate the program operation.

AUTO CHIP ERASE MODE: The auto chip erase mode is set by a "30H" command input. The device executes the auto erase operation by a succeeding "30H" command input at the next cycle. After programming all memory cells to a "0" data state, the chip erase and erase-verify operation is automatically executed inside the device. The status of the device is output from I/O7 for Ready/$\overline{\text{Busy}}$ and I/O4 for Pass/$\overline{\text{Fail}}$. The reset command (FFH) can be used to terminate the erase operation.

AUTO BLOCK ERASE MODE: The auto block erase mode is set by a "20H" command input. The next bus cycle will latch the block address (A14–A18) and the command data (D0H) and automatically execute the block erase operation. After programming all memory cells to a "0" data state, the block erase and erase-verify operation is automatically executed inside the device. The status of the device is output from I/O7 for Ready/$\overline{\text{Busy}}$ and I/O4 for Pass/$\overline{\text{Fail}}$. The reset command (FFH) can be used to terminate the erase operation.

RESET MODE: The reset mode is used to abort a program or erase operation and return the device to a known state. The reset operation is activated after two successive "FFH" command inputs. The device returns to the read mode after 6 μs of recovery time.

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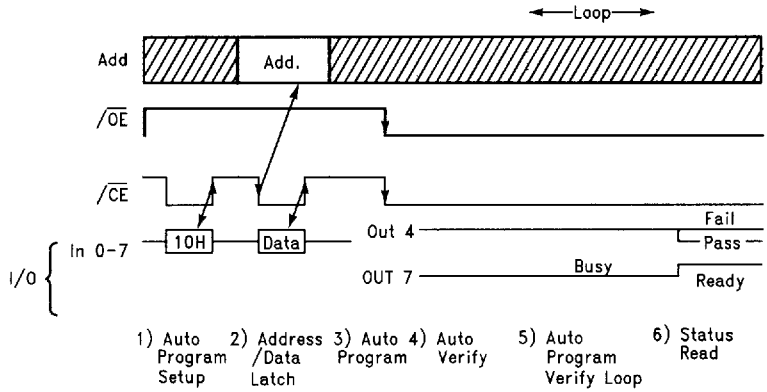
Auto Program, Auto Erase Operations

AUTO PROGRAM OPERATION



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The details of the auto program operation can be broken down to the following steps:

1. **AUTO PROGRAM SET-UP CYCLE:** This cycle sets up the device for a program operation by latching a "10H" command at the rising edge of $\overline{CE}$.
2. **ADDRESS/DATA LATCH CYCLE:** The address location is latched at the falling edge of $\overline{CE}$ while the data is latched at the rising edge of $\overline{CE}$. The program operation starts at the rising edge of $\overline{CE}$ in this second cycle.
3. **AUTO PROGRAM CYCLE:** The latched input data is automatically programmed into the selected address location.
4. **AUTO VERIFY CYCLE:** After the program cycle is completed, the data is automatically verified to see that it was written correctly.
5. **AUTO PROGRAM AND VERIFY LOOP CYCLE:** The program and verify cycles explained above automatically repeat until the written data is verified correct.
6. **STATUS READ CYCLE:** The status of the device is output on I/O4 and I/O7 when $\overline{CE}$ and $\overline{OE}$ are low during the program, verify or program/verify loop cycles. The verify result is output through I/O4 ("L" for "Pass" or "H" for "Fail"). The device status is output through I/O7 ("H" for "Ready" or "L" for "Busy"). "Ready" means that the operation has completed and the device can accept a new command. "Busy" means the device is still executing the last command and cannot be accessed except to Reset the device. This cycle must be kept active ($\overline{CE}$, $\overline{OE}$ = "L") for a minimum of 30 ns.

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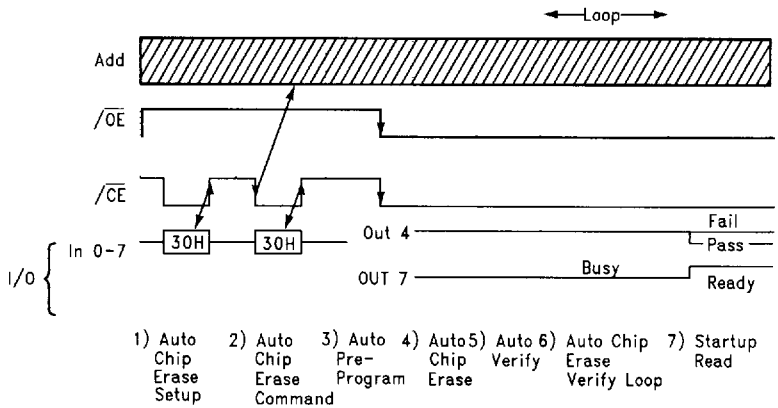
Auto Program, Auto Erase Operations (Continued)

AUTO CHIP ERASE OPERATION



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The details of the auto chip erase operation can be broken down to the following steps:

1. **AUTO CHIP ERASE SET-UP CYCLE:** This cycle sets up the device for a chip erase operation by latching a "30H" command at the rising edge of $\overline{CE}$.
2. **AUTO CHIP ERASE COMMAND CYCLE:** This cycle verifies that an auto chip erase operation is to be carried out by latching a second "30H" at the rising edge of $\overline{CE}$. This second latching cycle is needed to prevent accidental erasure of data due to possible external noise issues. The set-up command will be reset if any other command except the second "30H" is input. The following internal operations start at the rising edge of $\overline{CE}$.
3. **AUTO PRE-PROGRAM CYCLE:** Data "0" is automatically programmed into all memory cells of the device before the erase operation can be carried out. The pre-programming is executed in a similar manner to the auto program operation inside the device. The address is incremented by an internal address counter. This pre-program operation is needed to prevent over erasing of cells that originally contained "1" data.
4. **AUTO CHIP ERASE CYCLE:** The chip erase operation is executed automatically after pre-programming is complete.
5. **AUTO VERIFY CYCLE:** The verify operation is automatically executed after the chip erase has completed. The address is again incremented by the internal counter until all address locations are verified. The internal counter will stop at a failed address location.
6. **AUTO CHIP ERASE/VERIFY LOOP CYCLE:** The auto chip erase and verify cycles above will automatically repeat when the verify cycle fails.
7. **STATUS READ CYCLE:** The auto chip erase operation finishes when the verify operation for all memory cells successfully completes. The status read cycle operation is the same as outlined for a program operation.

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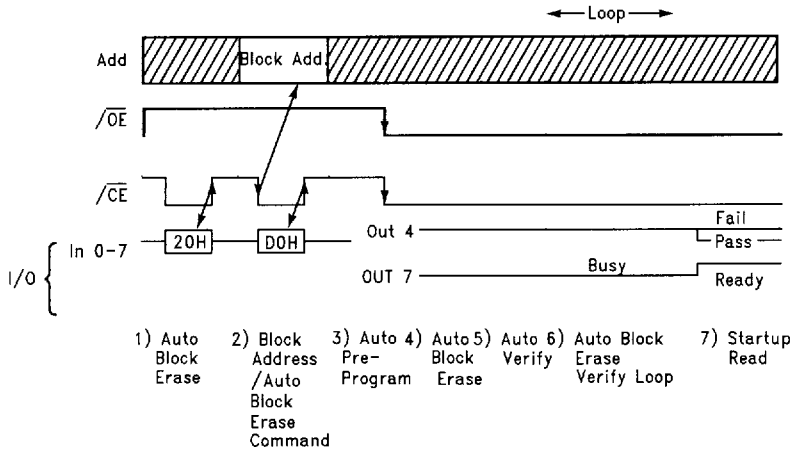
Auto Program, Auto Erase Operations (Continued)

AUTO BLOCK ERASE OPERATION



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The details of the auto block erase operation can be broken down to the following steps:

1. **AUTO BLOCK ERASE SET-UP CYCLE:** This cycle sets up the device for a block erase operation by latching a "20H" command at the rising edge of $\overline{CE}$.
2. **BLOCK ADDRESS/AUTO BLOCK ERASE COMMAND CYCLE:** The block address (A14–A18; other addresses are "H" or "L") for the block to be erased is latched at the falling edge of $\overline{CE}$. This cycle also verifies that an auto chip erase operation is to be carried out by requiring that "D0H" be latched at the subsequent rising edge of $\overline{CE}$. This second latching cycle is needed to prevent accidental erasure of data due to possible external noise issues. The set-up command will be reset if any other command except "D0H" is input in this second cycle. The following internal operations start at the rising edge of $\overline{CE}$.
3. **AUTO PRE-PROGRAM CYCLE:** Data "0" is automatically programmed into all memory cells of the selected block before the erase operation can be carried out. The pre-programming is executed in a similar manner to the auto program operation inside the device. The address is incremented by an internal address counter up to the last address of the selected block. This pre-program is needed to prevent over erasing of cells that originally contained "1" data.
4. **AUTO BLOCK ERASE CYCLE:** The block erase operation automatically after pre-programming is complete.
5. **AUTO VERIFY CYCLE:** The verify operation is automatically executed after the block erase has completed. The address is again incremented by the internal counter until all address locations within the block are verified. The internal counter will stop at a failed address location.
6. **AUTO BLOCK ERASE/VERIFY LOOP CYCLE:** The auto block erase and verify cycles above will automatically repeat when the verify cycle fails.
7. **STATUS READ CYCLE:** The auto block erase operation finishes when the verify operation for all memory cells within the selected block successfully completes. The status read cycle operation is the same as outlined for a program operation.

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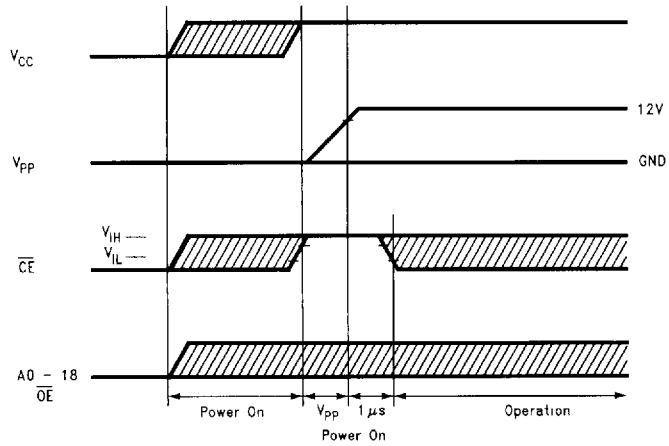
POWER ON/OFF SEQUENCE

The following sequences are needed to protect against data corruption during power on and power off conditions:

POWER ON: V_{PP} must be applied only after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high.

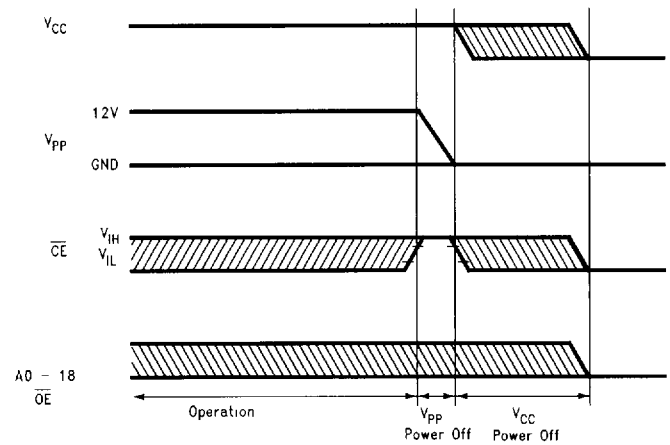
POWER OFF: V_{PP} must be turned off after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high. V_{CC} can only be turned off after V_{PP} has reached 0V.

(1) Power ON Sequence



TL/D/11873–16

(2) Power OFF Sequence



TL/D/11873–17

6501126 0069967 893

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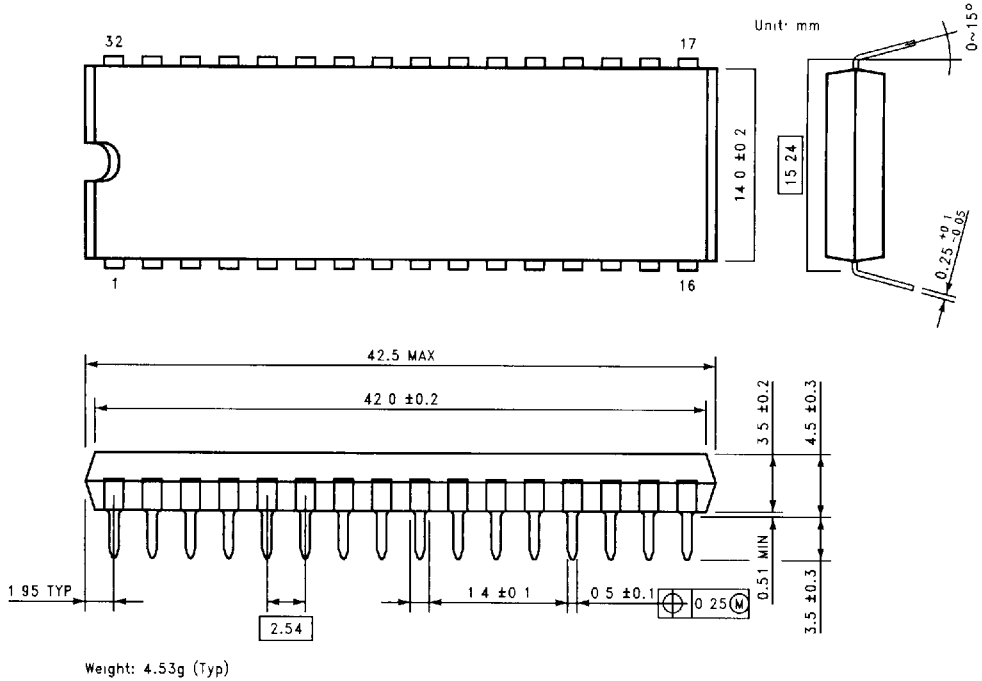
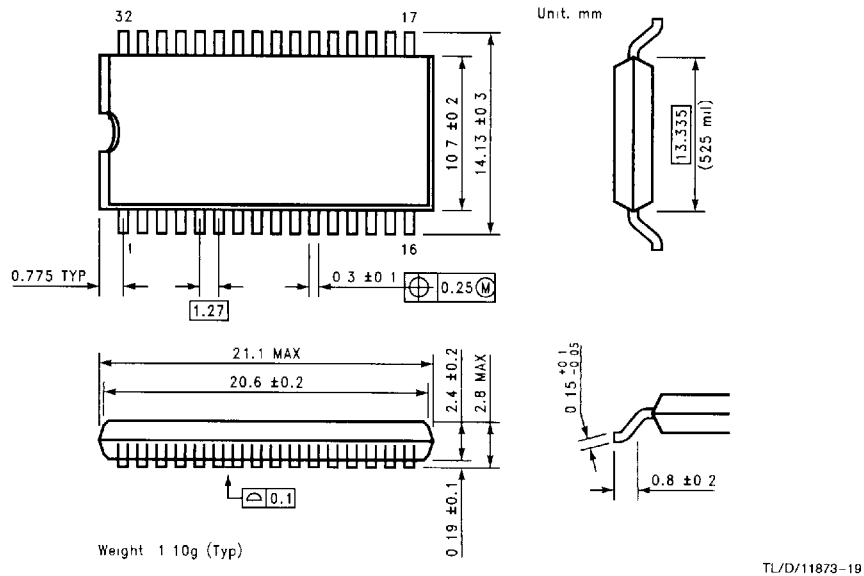
6501126 0069968 72T

Physical Dimensions millimeters



TL/D/11873–18

32-Pin Dual-In-Line Package (N)
Order Number NM28F040NXXX

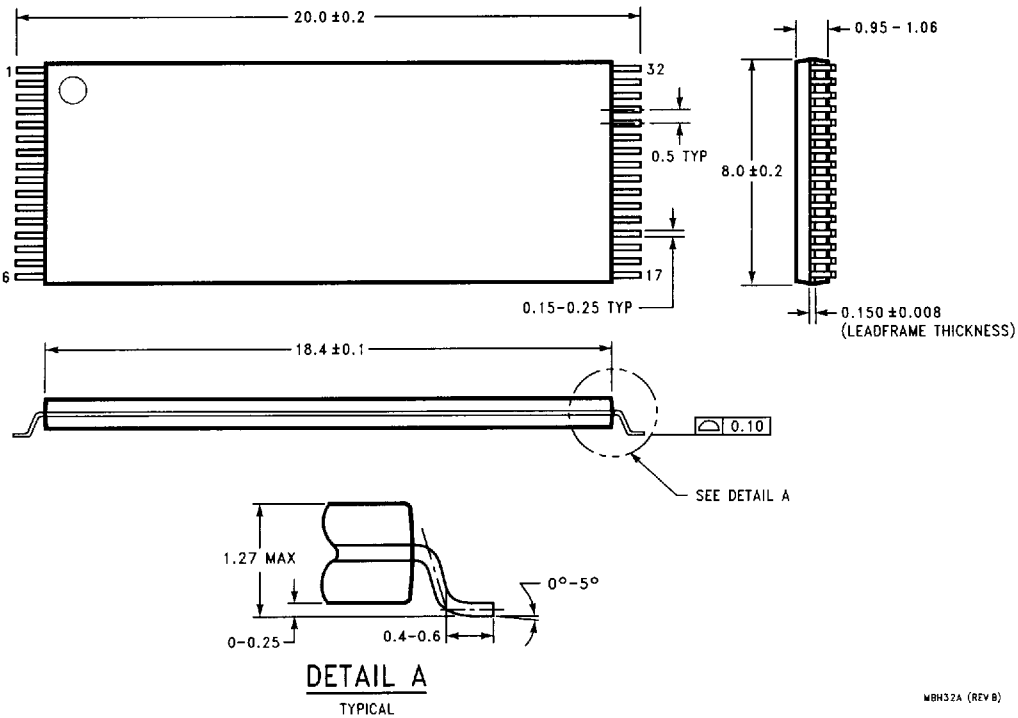


TL/D/11873–19

32-Pin Plastic Small Outline Package (M)
Order Number NM28F040MXXX

6501126 0069969 666

Physical Dimensions millimeters (Continued)



32-Pin Thin Small Outline Package (T)
Order Number NM28F040TXXX

32-Pin Reverse Thin Small Outline Package (TR)
Order Number NM28F040TRXXX
Package Number MBH32A

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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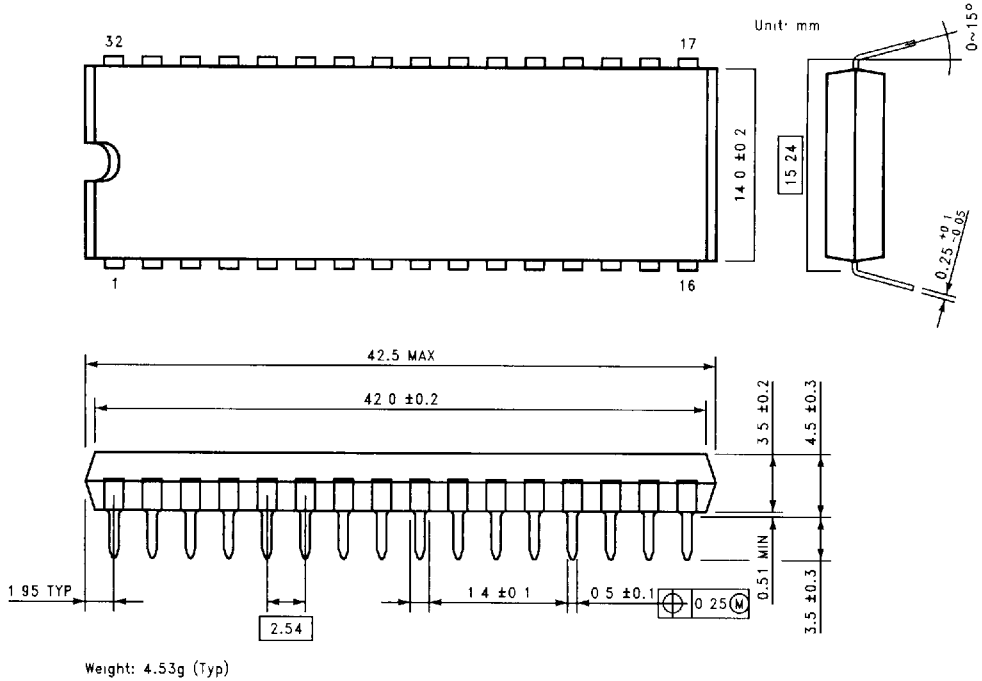
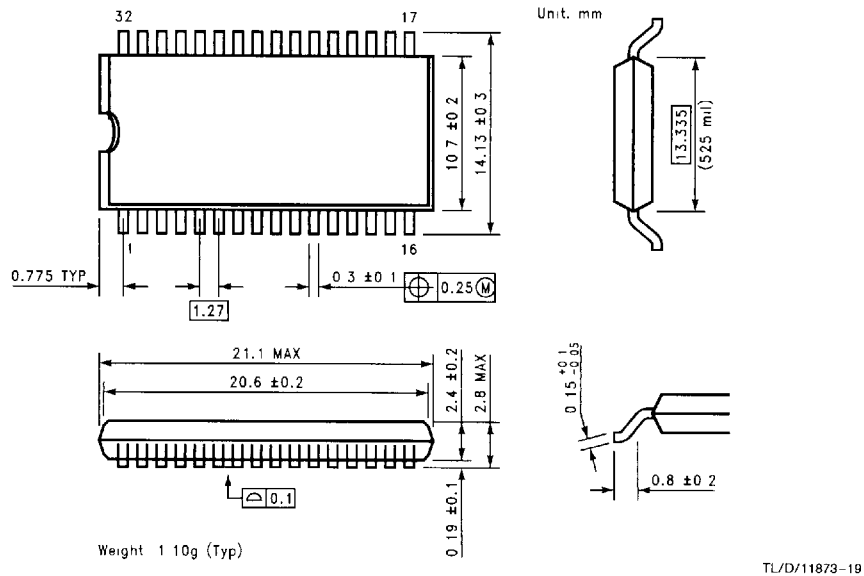
6501126 0069970 388

Physical Dimensions millimeters



TL/D/11873–18

32-Pin Dual-In-Line Package (N)
Order Number NM28F040NXXX

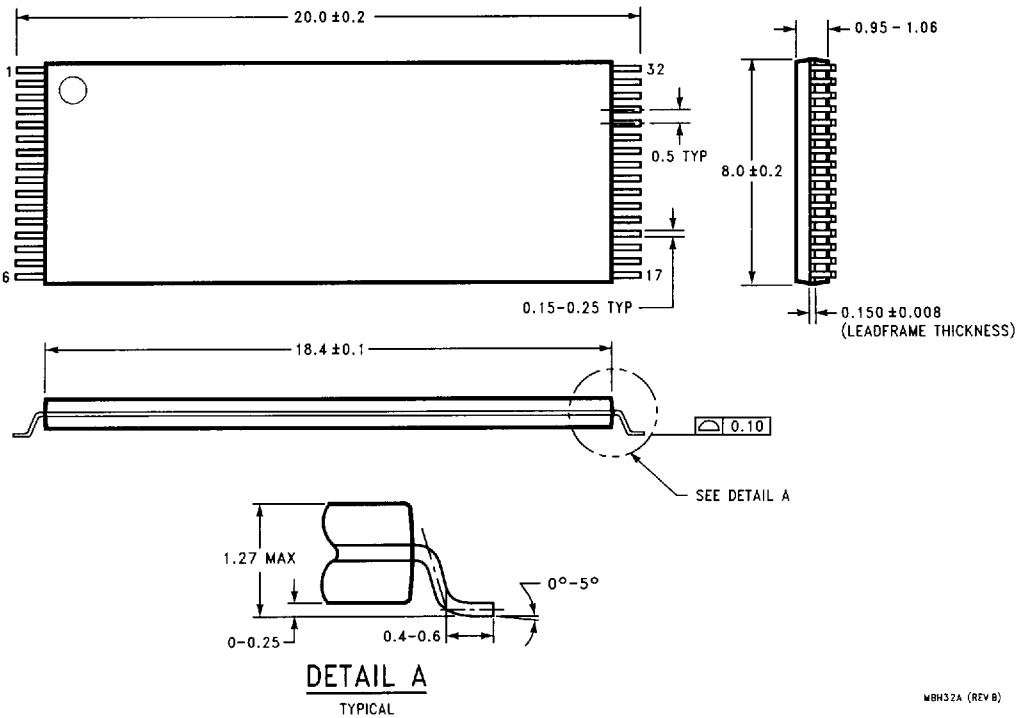


TL/D/11873–19

32-Pin Plastic Small Outline Package (M)
Order Number NM28F040MXXX

6501126 0069969 666

Physical Dimensions millimeters (Continued)



32-Pin Thin Small Outline Package (T)
Order Number NM28F040TXXX

32-Pin Reverse Thin Small Outline Package (TR)
Order Number NM28F040TRXXX
Package Number MBH32A

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